WAVETEK®

OPERATION AND MAINTENANCE MANUAL

MODELS 51, 52, 52A

Data Multimeters
Maintenance Manual

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OVERVIEW OF THE TABLE OF CONTENTS

SECTION 1 **HOW TO USE THIS MANUAL**

1.1 INTRODUCTION 1-1
1.2 WHAT IS IN THIS MANUAL 1-1
1.3 HOW TO USE THIS MANUAL 1-1
1.4 THE OPERATOR'S MANUAL 1-1
1.5 CONVENTIONS USED IN THIS MANUAL 1-1

SECTION 2 **ROUTINE MAINTENANCE**

2.1 CALIBRATION 2-1
2.2 FUSE REPLACEMENT 2-1
2.3 BATTERY REPLACEMENT 2-2
2.4 OPTION REPLACEMENT 2-4
2.5 PROM REPLACEMENT 2-4
2.6 MEASUREMENT MODULE REPLACEMENT 2-5

SECTION 3 **VERIFICATION PROCEDURES**

3.1 THE VERIFICATION PROCEDURE 3-1
3.2 REQUIRED TEST EQUIPMENT 3-1
3.3 INITIAL CHECKS 3-2
3.4 INITIAL SETUP 3-2
3.5 MEASUREMENT MODULE CHECKS 3-2
3.6 RS-232-C CHECK 3-6
3.7 IEEE-488 CHECK 3-6
3.8 DIGITAL I/O CHECK 3-7
3.9 MEMORY EXPANSION CHECK 3-7
3.10 PRIMARY AND RECHARGEABLE BATTERY CHECK 3-8
3.11 MULTIPLEXER CHECK 3-8
3.12 VERIFICATION RECORD 3-9

SECTION 4 **CALIBRATION PROCEDURE**

4.1 FACTORY REPAIR 4-1
4.2 REQUIRED TEST EQUIPMENT 4-1

SECTION 5 **MODEL 52 CIRCUIT DESCRIPTION**

5.1 INTRODUCTION 5-1
5.2 MOTHERBOARD 5-2
5.3 MEASUREMENT MODULES 5-19
5.4 MEASUREMENT CONTROL 5-36
5.5 MODEL 52 KEYPAD CIRCUITRY 5-67
5.6 MODEL 52 DISPLAY ASSEMBLY 5-67
5.7 50-14 DIGITAL I/O OPTION 5-68
5.8 EXPANSION RAM BOARDS 5-76
5.9 50-13 GPIB BOARD 5-80
5.10 MULTIPLEXERS 5-89
5.11 RECHARGEABLE BATTERY ASSEMBLY 5-98

SECTION 6 **TROUBLESHOOTING**

SECTION 7 **DRAWING PACKAGE**

APPENDICES

LIST OF TABLES AND FIGURES

TABLE OF CONTENTS

SECTION 1 HOW TO USE THIS MANUAL

1.1 INTRODUCTION 1-1
1.2 WHAT IS IN THIS MANUAL 1-1
1.3 HOW TO USE THIS MANUAL 1-1
1.4 THE OPERATOR'S MANUAL 1-1
1.5 CONVENTIONS USED IN THIS MANUAL 1-1

SECTION 2 ROUTINE MAINTENANCE

2.1 CALIBRATION 2-1
2.2 FUSE REPLACEMENT 2-1
2.2.1 Power Fuse 2-1
2.2.2 Current Overload Fuse 2-1
2.2.3 Battery Charger Fuse 2-1
2.3 BATTERY REPLACEMENT 2-2
2.3.1 Primary Power Battery 2-2
2.3.2 RAM Backup Battery 2-3
2.4 OPTION REPLACEMENT 2-4
2.5 PROM REPLACEMENT 2-4
2.6 MEASUREMENT MODULE REPLACEMENT 2-5
2.6.1 Preparation 2-5
2.6.2 To Remove The Measurement Module 2-5
2.6.3 To Install The Measurement Module 2-5
2.6.4 Closing Up 2-5

SECTION 3 VERIFICATION PROCEDURES

3.1 THE VERIFICATION PROCEDURE 3-1
3.2 REQUIRED TEST EQUIPMENT 3-1
3.3 INITIAL CHECKS 3-2
3.4 INITIAL SETUP 3-2
3.5 MEASUREMENT MODULE CHECKS 3-2
3.5.1 DC Voltage Checks (Models 50-1 and 50-2) 3-2
3.5.2 Cold Junction Temperature (Models 50-1 and 50-2) 3-2
3.5.3 AC Voltage Check (Model 50-1 only) 3-3
3.5.4 Zero Resistance Check (Model 50-1 only) 3-3
3.5.5 Resistance (>1kΩ) Check (Model 50-1 only) 3-3
3.5.6 Resistance (<100kΩ Check (Model 50-1 only) 3-4
3.5.7 DC Current (mA) Check (Model 50-1 only) 3-4
3.5.8 DC Current (A) Check (Model 50-1 only) 3-4
3.5.9 AC Current (mA) Check (Model 50-1 only) 3-5
3.5.10 AC Current (A) Check (Model 50-1 only) 3-5
3.5.11 Frequency Check (Model 50-1 only) 3-5
3.5.12 Input Sensitivity Check (Model 50-1 only) 3-6
3.5.13 Input Sensitivity (TTL) Check (Model 50-1 only) 3-6
3.5.14 Input Sensitivity (CMOS) Check (Model 50-1 only) 3-6
3.6 RS-232-C CHECK 3-6
3.7 IEEE-488 CHECK 3-6
3.8 DIGITAL I/O CHECK 3-7
3.9 MEMORY EXPANSION CHECK 3-7

CONTENTS (Continued)

3.10 PRIMARY AND RECHARGEABLE BATTERY CHECK 3-8
3.11 MULTIPLEXER CHECK 3-8
3.12 VERIFICATION RECORD 3-9

SECTION 4 **CALIBRATION PROCEDURE**

4.1 FACTORY REPAIR 4-1
4.2 REQUIRED TEST EQUIPMENT 4-1
4.2.1 Calibrating the Models 51 and 52 4-1

SECTION 5 **MODEL 52 CIRCUIT DESCRIPTION**

5.1 INTRODUCTION 5-1
5.2 MOTHERBOARD 5-2
5.2.1 Overview 5-2
5.2.2 Logic And Logic Levels Used 5-2
5.2.3 The Motherboard Power Supplies 5-3
5.2.3.1 The Power Supplies Overviewed 5-3
5.2.3.2 Power Down Feature Vs. Power Save Feature 5-3
5.2.3.3 Battery Pack Pin 4 Signals: 50-11 Vs. 50-10 5-4
5.2.3.4 IEEE-488 Power Control 5-4
5.2.3.5 Raw B+ For V++ and V+ Regulators 5-5
5.2.3.6 In Case Of Power Loss 5-6
5.2.3.7 Too-low-to-operate Vs. "LOW BAT" 5-6
5.2.3.8 U12 Regulation Of V++ Voltage 5-7
5.2.3.9 Generation Of V+ Voltage 5-7
5.2.4 Power On-off Control 5-8
5.2.4.1 Overview 5-8
5.2.4.2 Detailed Turn On Explanations 5-9
5.2.4.3 Detailed Turn Off Explanations 5-10
5.2.5 MPU Bus Overhead Lines 5-11
5.2.5.1 MPU Clock And E Generation 5-11
5.2.5.2 $R/\overline{W}$ 5-11
5.2.5.3 A0-A7 Address Latching 5-11
5.2.5.4 Data Latching 5-13
5.2.6 Other MPU Lines 5-13
5.2.6.1 $\underline{\text{STBY}}$ Line 5-13
5.2.6.2 $\overline{\text{RESET}}$ Line 5-13
5.2.6.3 P20-P24 Lines 5-13
5.2.6.4 RS-232 5-13
5.2.6.5 P10-P17 Lines 5-14
5.2.6.6 $\overline{\text{NMI}}$ Line 5-14
5.2.7 Addresses Above 32K: ROM 5-14
5.2.8 Addresses Less Than 32K 5-15
5.2.8.1 Memory Map And Sheet 2 Address Decoding 5-15
5.2.8.2 8-16K: CALRAM and User Storage 5-15
5.2.8.3 16-24K: User Standard RAM 5-15
5.2.8.4 24-32K: Expansion RAM 5-15
5.2.8.5 0-8K 5-15
5.2.8.5.1 0-8K Overview 5-15
5.2.8.5.2 MPU Internal Registers ($00\text{-}1F_H$) 5-15

CONTENTS (Continued)

5.2.8.5.3 U27 Gate Array (20_H-$3F_H$) 5-16
5.2.8.5.4 Unassigned 40_H-$7F_H$ 5-16
5.2.8.5.5 MPU Internal RAM (80_H-FF_H) 5-16
5.2.8.5.6 Clock And Beeper ($100+_H$) 5-16
5.2.8.5.7 Local Display (200_H-$5FF_H$) 5-16
5.2.8.5.8 Keyboard ($600+_H$) 5-17
5.2.8.5.9 Plug-in Option Board Address Decoding ($72X_H$-$7AX_H$) 5-17
5.2.8.5.10 Plug-in Slot Address Line Buffering 5-17
5.2.8.5.11 Power Off (7E0-7FF) 5-19
5.3 MEASUREMENT MODULES 5-19
5.3.1 50-1 and 50-2 Overview 5-19
5.3.1.1 Measured-quantity Signal Flow 5-19
5.3.1.2 Software-controlled Lines And Relays 5-21
5.3.2 Measurement Module Detailed Circuit Description 5-23
5.3.2.1 Power Supply 5-23
5.3.2.2 A/D Converter 5-24
5.3.2.3 True RMS Converter 5-26
5.3.2.4 AC Converter 5-27
5.3.2.5 Programmable Schmitt Trigger 5-30
5.3.2.6 Prescaler And Frequency Divider Circuitry 5-30
5.3.2.7 A/D Gain 5-31
5.3.2.8 A/D Input MUX 5-31
5.3.2.9 Precision Current Source 5-33
5.3.2.10 Input Terminal Arrangements; Grounds 5-36
5.4 MEASUREMENT CONTROL 5-36
5.4.1 Introduction 5-36
5.4.2 MPU to Measurement Module Communications 5-38
5.4.2.1 U27 — The Parallel To Serial Converter 5-38
5.4.2.2 Three-line Serial Shift Format 5-38
5.4.2.3 How Three-line Serial Turns Into Parallel 5-38
5.4.2.3.1 Overview 5-38
5.4.2.3.2 8-bit Shifts 5-39
5.4.2.3.3 "32-bit" Shifts 5-39
5.4.3 Module Type Checking During A Power-on 5-41
5.4.4 Sending Measurements To The Motherboard 5-44
5.4.4.1 Introduction 5-44
5.4.4.2 Review Of The Basics 5-46
5.4.4.3 A/D Functions 5-47
5.4.4.4 Vdc Example 5-47
5.4.4.5 Counter Type Functions 5-47
5.4.5 The Measurement Control Patterns 5-50
5.4.5.1 How To Read The Control Patterns Below 5-50
5.4.5.2 Default Control Patterns, By Function 5-51
5.4.5.3 Vdc 5-52
5.4.5.4 dBdc 5-56
5.4.5.5 CJTEMP 5-56
5.4.5.6 TEMP 5-57
5.4.5.7 OHMS, CONT, ▶|CHK 5-57
5.4.5.8 Vac 5-58
5.4.5.9 Vac + dc 5-59
5.4.5.10 dB 5-59

CONTENTS (Continued)

5.4.5.11 Adc 5-59
5.4.5.12 Aac 5-60
5.4.5.13 Aac + dc 5-60
5.4.5.14 Wdc 5-61
5.4.5.15 VAac 5-62
5.4.5.16 VAac + dc 5-63
5.4.5.17 Counter Functions 5-63
5.4.5.17.1 General 5-63
5.4.5.17.2 EVENTS 5-65
5.4.5.17.3 FREQ 5-65
5.4.5.17.4 PERIOD 5-66
5.4.5.17.5 T-INT, T-INT..1SHOT 5-66
5.4.5.17.6 P-WTH, P-WTH..1SHOT 5-66
5.4.5.18 LOGIC 5-66
5.5 MODEL 52 KEYPAD CIRCUITRY 5-67
5.6 MODEL 52 DISPLAY ASSEMBLY 5-67
5.7 50-14 DIGITAL I/O OPTION 5-68
5.7.1 General Description 5-68
5.7.2 Control Block 5-69
5.7.3 Digital Output Block 5-70
5.7.4 Analog Output Block 5-71
5.7.5 Digital Input Block 5-73
5.7.6 Board Identification Block 5-75
5.8 EXPANSION RAM BOARDS 5-76
5.8.1 Expansion RAM Overview 5-76
5.8.2 50-12 Board 5-76
5.8.2.1 Bank Selection For The MPU 24-32K Window 5-76
5.8.2.2 Byte-level Decoding 5-77
5.8.2.3 Expansion RAM Reading And Writing 5-78
5.8.2.4 Summary Of 5.8.2 5-78
5.8.3 50-12A Board 5-78
5.8.3.1 Bank Selection For The MPU 24-32K Window 5-78
5.8.3.2 Byte-level Decoding 5-79
5.8.3.3 Expansion RAM Reading And Writing 5-79
5.8.3.4 Summary Of 5.8.3 5-79
5.9 50-13 GPIB BOARD 5-80
5.9.1 The Bus 5-80
5.9.1.1 The Bus Lines 5-80
5.9.1.2 The Models 51 and 52 as a Talker 5-80
5.9.1.3 The Models 51 and 52 as a Listener 5-81
5.9.1.4 The Service Request and the Models 51 and 52 5-82
5.9.2 The GPIB Board 5-82
5.9.2.1 The GPIA 5-83
5.9.2.2 The Bus Transceivers 5-84
5.9.2.3 GPIB Address Switch and Board Identification 5-85
5.9.2.4 GPIA Transceiver 5-85
5.9.2.5 Buffer 5-88
5.9.2.6 GPIB Initialization 5-88
5.10 MULTIPLEXERS 5-89
5.10.1 Introduction 5-89
5.10.2 Option 50-20 5-89

CONTENTS (Continued

5.10.2.1 Multiplexer Switching 5-90
5.10.2.2 Switch Matrix 5-91
5.10.2.3 Switch Control 5-93
5.10.2.4 Cold Junction Temperature 5-95
5.10.3 Option 53-1 5-96
5.10.3.1 Multiplexer Switching 5-96
5.10.3.2 Bank Control 5-96
5.10.3.3 Cold Junction Temperature 5-96
5.10.3.4 Current Source 5-96
5.10.4 Option 53-2 5-96
5.10.4.1 Multiplexer Switching 5-97
5.10.4.2 Switch Matrix 5-97
5.10.4.3 Switch Control 5-97
5.10.4.4 Cold Junction Temperature 5-97
5.10.4.5 Current Source 5-97
5.11 RECHARGEABLE BATTERY ASSEMBLY 5-98
5.11.1 Battery 5-98
5.11.2 Battery Charger 5-98
5.11.3 Power Detector 5-98

SECTION 6 TROUBLESHOOTING

6.1 INTRODUCTION 6-1
6.2 FACTORY REPAIR 6-1
6.3 BEFORE YOU START 6-2
6.4 TROUBLESHOOTING THE MODELS 51 AND 52 6-2
6.4.1 Troubleshooting Overview 6-2
6.4.2 Narrowing Down The Fault Possibilities 6-2
6.4.3 Isolating A Problem To A Board 6-2
6.4.3.1 Overview 6-2
6.4.3.2 Motherboard Vs. Measurement Module 6-3
6.4.3.2.1 Operating Vs. Board Swapping 6-3
6.4.3.2.2 One-measurement-module Approaches 6-3
6.4.3.2.3 Two-module Approaches (Preferred) 6-3
6.4.3.2.4 Signature Analysis Of Motherboard Signals 6-4
6.4.3.3 Motherboard Vs. Keypad 6-4
6.4.3.4 Motherboard Vs. Display 6-4
6.4.3.5 Motherboard Vs. Digital I/O 6-4
6.4.3.6 Motherboard Vs. RAM Board 6-5
6.4.3.7 Motherboard Vs. GPIB Board 6-5
6.4.3.8 Measurement Module Vs. Multiplexer 6-5
6.4.3.9 Batteries 6-5
6.4.4 Isolating Bad Circuits Within A Board 6-5
6.4.4.1 Overview 6-5
6.4.4.2 Motherboard Troubleshooting 6-6
6.4.4.3 Measurement Module Troubleshooting 6-9
6.4.4.4 Keypad Troubleshooting 6-14
6.4.4.5 Display Troubleshooting 6-15
6.4.4.6 Digital I/O Board Troubleshooting 6-15
6.4.4.7 Expansion RAM Board Troubleshooting 6-16
6.4.4.8 GPIB Board Troubleshooting 6-16

CONTENTS (Continued)

6.4.4.9 Multiplexer Troubleshooting 6-17
6.4.4.10 Rechargeable Battery Assembly Troubleshooting 6-18

SECTION 7 DRAWING PACKAGE

7.1 DRAWINGS 7-1
7.2 ORDERING PARTS 7-1
7.3 ERRATA 7-1

APPENDIX A AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII) A-1

APPENDIX B RECOMMENDED SPARE PARTS B-1

APPENDIX C MOTHERBOARD VS. OPTION BOARD FAULT ISOLATION C-1

APPENDIX D DECIMAL/HEXADECIMAL/BINARY NUMBER EQUIVALENTS D-1

APPENDIX E REMOVING OR REPLACING CHIP RESISTORS AND CAPACITORS E-1

APPENDIX F REPLACING SMALL OUTLINE IC'S F-1

APPENDIX G MOTHERBOARD POWER LINE DESTINATIONS G-1

LIST OF TABLES

Table 2-1 Possible Location For The Option 2-4
Table 3-1 Required Test Equipment 3-1
Table 4-1 Required Test Equipment 4-1
Table 4-2 Calibration Procedure 4-1
Table 5-1 0-32K Memory Map 5-15
Table 5-2 Some Internal MPU Registers 5-16
Table 5-3 U24 Decoder Outputs 5-17
Table 5-4 Latching Relay Usage 5-22
Table 5-5 Deintegrate Times 5-26
Table 5-6 Comparator Output Pin States 5-26
Table 5-7 AC CONVERTER Gain Switching 5-28
Table 5-8 U15C and U15B Gain Switching 5-29
Table 5-9 U5 Gain Derivation 5-31
Table 5-10 Control Line States for Measuring DC Current 5-32
Table 5-11 Constant Currents Generated by Function 5-34
Table 5-12 Measurement Module Default Control Patterns 5-51
Table 5-13 Keypad Stimulation Pattern 5-67
Table 5-14 Display Module Initialization Sequence 5-67
Table 5-15 Control 5-69
Table 5-16 Decoder 5-71
Table 5-17 Digital Output Logic 5-71
Table 5-18 Analog Output Examples 5-74
Table 5-19 DAV, NRFD, NDAC Control 5-84
Table 5-20 Multiplexer Switching 5-92
Table 5-21 Switch Matrix 5-92
Table 5-22 Row Decoder Logic 5-93
Table 5-23 Column Decoder 5-94
Table 5-24 Channel Enable 5-95
Table 5-25 Cold Junction Temperature 5-96
Table 6-1 Suggested Test Equipment 6-1
Table 6-2 Circuit Board Supporting Paragraphs 6-2
Table 6-3 Measurement Module Function References 6-10
Table 6-4 Function Vs. Circuit Blocks Matrix 6-11

LIST OF ILLUSTRATIONS

Figure 2-1 Power Fuse 2-1
Figure 2-2 Overload Fuse 2-2
Figure 2-3 Top Cover Removal 2-2
Figure 2-4 Model 51 or 52 Internal Locator 2-3
Figure 2-5 Battery Charger Fuse 2-3
Figure 2-6 Battery Housing 2-3
Figure 3-1 Four-Wire Resistance 3-4
Figure 3-2 Digital I/O Check Interconnections 3-8
Figure 5-1 Busses Internal To The Model 52 5-0
Figure 5-2 Power Down Vs. Power Save 5-4
Figure 5-3 Battery Board Identification/IEEE Power Control 5-5

ILLUSTRATIONS (Continued)

Figure 5-4 B+ Dropout/brownout Turn Off-Request Circuitry 5-6
Figure 5-5 LT1020 Regulation Circuitry 5-7
Figure 5-6 Simplified Switcher 5-8
Figure 5-7 Switcher Voltage Waveforms 5-9
Figure 5-8 Y1 Crystal and E Waveforms 5-12
Figure 5-9 AD0-AD7 Address/Data Multiplexing 5-12
Figure 5-10 Devices Using Address Decoding 5-18
Figure 5-11 Block Diagram, Measured-quantity Signal Flow 5-19
Figure 5-12 Input Terminal Arrangements, Measurement Module 5-20
Figure 5-13 SIPO Control Registers 5-21
Figure 5-14 Latching Relay Pinout 5-22
Figure 5-15 ICL7660 Operation 5-23
Figure 5-16 Simplified Integrator 5-24
Figure 5-17 Integrator Ramps 5-24
Figure 5-18 Simplified Converter Operation 5-25
Figure 5-19 AD637 Block Diagram 5-27
Figure 5-20 AD637 Two-pole Filter 5-28
Figure 5-21 U15D at X1 Gain 5-29
Figure 5-22 Schmitt Trigger Noise Immunity 5-30
Figure 5-23 U5 Gain Configuration 5-31
Figure 5-24 Thermocouple Wires-to-Copper Thermocouples 5-33
Figure 5-25 Setting U3-2 Input Currents/Simplified Feedback Loop 5-35
Figure 5-26 Making the I_{out} Go Through $R_{unknown}$ 5-35
Figure 5-27 Measurement Control 5-37
Figure 5-28 Counter Function Shift 5-39
Figure 5-29 32 And 8 Bit Shifts For FREQuency, Front Panel Input 5-40
Figure 5-30 32 Bit Shift For FREQuency, Back Panel Input 5-41
Figure 5-31 Type Checking 5-42
Figure 5-31a Complete Type Checking Routine 5-42
Figure 5-31b First Two Bursts 5-42
Figure 5-31c First Burst 5-43
Figure 5-31d First Part Of First Burst 5-43
Figure 5-31e Last Part Of First Burst 5-43
Figure 5-31f Burst #2 Intensified 5-43
Figure 5-31g Burst #2 Intensified (intermediate setup) 5-44
Figure 5-31h Burst #2 Shown On Delayed Time Base 5-44
Figure 5-31i Burst #3 Intensified 5-44
Figure 5-31j Burst #3 5-44
Figure 5-31k Burst #4 Intensified 5-45
Figure 5-31l Burst #4 5-45
Figure 5-31m Burst #5 5-45
Figure 5-31n Burst #6 5-45
Figure 5-31o Burst #7 5-46
Figure 5-31p Burst #7, First part (U10) 5-46
Figure 5-31q Burst #7, Last part (U30) 5-46
Figure 5-31r Burst #8 5-46
Figure 5-32 The Timing Of The OUT Signal 5-48
Figure 5-33 The 8 Bursts For Vdc 5-49
Figure 5-34 Vdc, 3V Range, All Bursts 5-53
Figure 5-35 Vdc, 3V Range, Burst #1 5-53
Figure 5-36 Vdc, 3V Range, Burst #2 5-53

ILLUSTRATIONS (Continued)

Figure 5-37 Vdc, 3V Range, Burst #3 5-53
Figure 5-38 Vdc, 3V Range, Burst #4 5-54
Figure 5-39 Vdc, 3V Range, Burst #5 Overall 5-54
Figure 5-40 Vdc, 3V Range, First Part Of Burst #5 5-54
Figure 5-41 Vdc, 3V Range, Last Part Of Burst #5 5-54
Figure 5-42 Vdc, 3V Range, Burst #6 5-55
Figure 5-43 Vdc, 3V Range, Burst #7 5-55
Figure 5-44 Vdc, 3V Range, Burst #8 5-55
Figure 5-45 Display Addresses 5-68
Figure 5-46 Digital I/O Board Block Diagram 5-69
Figure 5-47 Control Block Diagram 5-70
Figure 5-48 Latch Timing 5-70
Figure 5-49 Decoder Timing 5-71
Figure 5-50 Digital Output 5-72
Figure 5-50a Digital Output II 5-73
Figure 5-51 Analog Output Block Diagram 5-73
Figure 5-52 Analog Output Timing 5-73
Figure 5-53 Digital Input 5-74
Figure 5-54 Digital Input Timing 5-75
Figure 5-55 Digital Input Logic Levels 5-75
Figure 5-56 External Trigger Input 5-75
Figure 5-57 Board Identification Block 5-76
Figure 5-58 Board Identification Timing 5-76
Figure 5-59 Talker/Listener 5-80
Figure 5-60 GPIB Bus Lines 5-80
Figure 5-61 Talker Timing 5-81
Figure 5-62 Listener Timing 5-82
Figure 5-63 GPIB Board Block Diagram 5-83
Figure 5-64 General Purpose Interface Adapter 5-84
Figure 5-65 GPIB Transceiver 5-85
Figure 5-66 GPIB Address/Identification 5-86
Figure 5-67 GPIA Transceiver 5-87
Figure 5-68 Buffer 5-87
Figure 5-69 GPIB Initializer 5-88
Figure 5-70 Multiplexer Block Diagram 5-89
Figure 5-71 Multiplexer Switching 5-90
Figure 5-72 Single Ended Switching 5-91
Figure 5-73 Differential Switching 5-91
Figure 5-74 Switch Matrix 5-93
Figure 5-75 Switch Control 5-94
Figure 5-76 Cold Junction Temperature 5-95
Figure 5-77 Battery Charger 5-99
Figure 5-78 Battery Charger 5-99
Figure 5-79 Battery Charger Timing 5-100
Figure 5-80 Power Detector 5-100
Figure 6-1 J12-J15 Pinout 6-3

SAFETY

WARNING

The case of the unit is not connected to earth ground through the AC Adapter. The case may inductively or electrostatically float to a high voltage if used in a strong electromagnetic or electrostatic field. This presents the potential for a nasty shock. To prevent this, the case may be connected to earth ground using the uninsulated banana jack (⏚◎) on the rear panel.

Grounds for the Digital I/O, IEEE-488, and RS-232-C cards are connected internally to the case. If one of these grounds in external equipment is connected to earth ground, this will make unnecessary the precautionary connection of the paragraph above, when the unit would have floated electrostatically.

Measurement modules ''float'' to approximately the input common mode voltage. The measurement modules have a shield over their midsection. This shield is connected to analog ground (measurement module input LO). With the case cover off, this shield is exposed. This shield is at input LO potential.

SECTION 1
HOW TO USE THIS MANUAL

1.1 INTRODUCTION

This manual contains information relating to the testing, calibration, and servicing of the Wavetek Models 51 and 52 Data Multimeters.

1.2 WHAT IS IN THIS MANUAL

This manual contains the following information:

Section 2 Routine preventive maintenance. Removal and replacement of options, accessories, and upgrades.
Section 3 Verification Procedure.
Section 4 Calibration Procedure.
Section 5 Circuit Description — multimeter circuits and their operation.
Section 6 Troubleshooting — tips and details about the various circuits in the multimeter.
Section 7 The drawing package — schematics, parts location drawings, and parts lists.

1.3 HOW TO USE THIS MANUAL

The purpose of the maintenance manual is to support you in keeping your Model 51 or 52 functioning correctly. How the material in this manual is used depends on your needs.

Spare And Replacement Parts

Users who plan on servicing the unit themselves may choose to order spare parts from Wavetek. Appendix E is a list of recommended spare parts.

For each electronic assembly there is also parts list in the drawing package, Section 7. Any part may be ordered from Wavetek.

Suspected Malfunctions

If the malfunction is known, turn to the appropriate section and correct the fault. Use the Calibration Procedure when the problem is calibration (the entire Calibration Procedure does not need to be performed, only the portions needed to correct the error). Remember, the Calibration Procedure only affects Measurement Modules. Use the Troubleshooting to locate and correct any outright failues.

When the problem is not so obvious, use the Verification Procedure to check out the multimeter. If a step in the first part (paragraph 3.5) of the Verification Procedure is out of limits, use the Calibration Procedure to correct the error. If the multimeter can not be calibrated, you should refer to the Troubleshooting section. The second part of the Verification Procedure (paragraphs 3.6 through 3.11) checks out the options to the Model 51 or 52.

The Circuit Description, schematics, and assembly drawings all support the Troubleshooting.

Once again, if the Model 51 or 52 does not operate correctly, check your set up in the *Models 51 and 52 Operator's Manual* before proceeding to the troubleshooting procedures.

1.4 THE OPERATOR'S MANUAL

This manual does not cover the operation of the Model 51 or 52. The *Models 51 and 52 Operator's Manual* contains that information which is summarized below:

Multimeter specifications.
Preparation for use and installation.
Operational overview.
Local operation (Model 52 only).
Remote operation (Models 51 and 52).

1.5 CONVENTIONS USED IN THIS MANUAL

In this manual the Models 51 and 52 is often refered to as the "multimeter" or "unit".

Digital Logic — Throughout this manual, with the exception of RS-232, positive digital logic notation is used. That is, a "0" or low in a table or in the text means that the signal is close to ground, and a "1" or high means that the signal is close to the positive rail. The context of the text shows if the signal of interest is steady state or dynamic: the latter meaning that a 1 or 0 is being specified only in a particular time frame.

SECTION 2
ROUTINE MAINTENANCE

This section covers various items related to the routine maintenance of the Model 51 or 52.

2.1 CALIBRATION

To maintain the accuracy of the Model 51 or 52, the multimeter should calibrated at least once a year using the Calibration Procedure, Section 4. The Models 50-1 and 50-2 Measurement Modules are the only components that require calibration.

Once the Calibration Procedure has been performed, the multimeter will hold calibration "adjustments" as long as the internal RAM battery maintains the memory.

2.2 FUSE REPLACEMENT

The multimeter contain from 1 to 6 fuses, which throughout normal use may need replacement.

Power fuse
Current overload fuse (Model 50-1 Measurement Module)
Battery charger fuse (Option 50-11 Rechargeable Battery)

2.2.1 Power Fuse

The power fuse, located on the rear panel, is a 1A, 3AG type fuse. Figure 2-1 illustrates the replacement of the power fuse.

2.2.2 Current Overload Fuse

The 320 mA inputs to the Option 50-1 Measurement Modules are protected by 1A, 3AG type fuses. These fuses are accessible from the bottom of the multimeter. Figure 2-2 illustrates replacement of one of the overload fuses.

2.2.3 Battery Charger Fuse

The battery charger for option 50-11 Rechargeable Battery is protected by 1A, 3AG type fuse. Option 50-11 Rechargeable Battery is attached to the inside top cover of the multimeter. The following procedure describes battery charger fuse replacement.

1. Disconnect the multimeter from the power source.
2. Remove the top cover; see figure 2-3.
3. Disconnect the battery cable from the circuit board; see figure 2-4.
4. Remove the battery charger fuse cover; see figure 2-5.
5. Replace the fuse with a 1A, 3AG type fuse.
6. Replace the battery charger fuse cover, connect the battery cable to the circuit board (figure 2-4), and replace the top cover (figure 2-3).

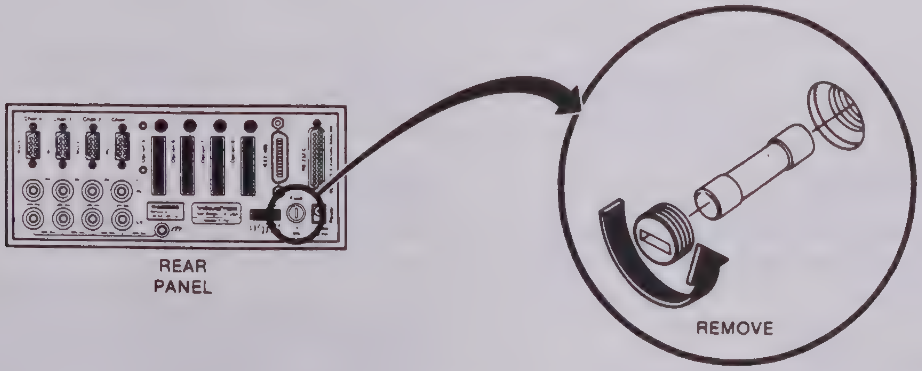


Figure 2-1. Power Fuse

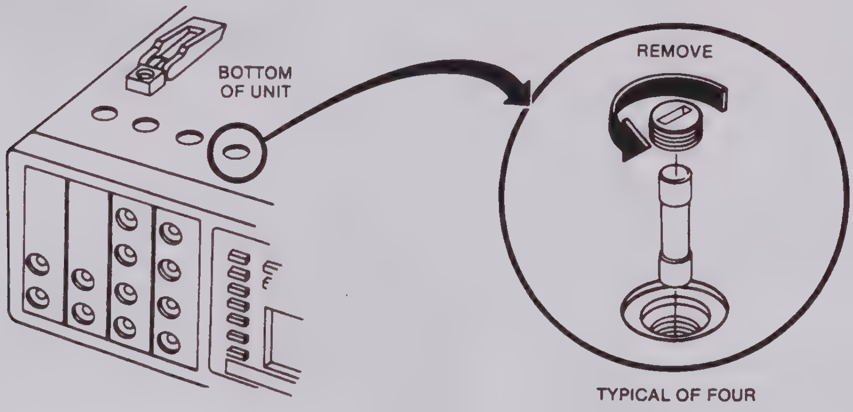


Figure 2-2. Overload Fuse

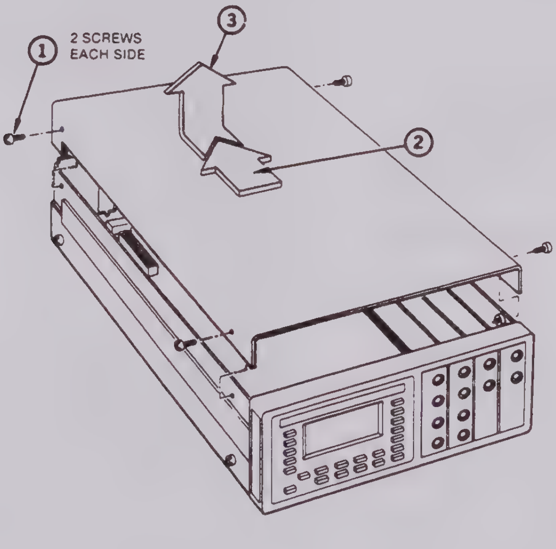


Figure 2-3. Top Cover Removal

2.3 BATTERY REPLACEMENT

The Model 51 or 52 can contain two batteries (Primary power Option 50-10 and RAM backup) that will occasionally need replacement.

2.3.1 Primary Power Battery

The following procedure describes the installation or replacement of Option 50-10 alkaline cells.

1. Remove the top cover; see figure 2-3.
2. Disconnect the battery cable from the circuit board; see figure 2-4.
3. Open the top cover's battery housing cover (see figure 2-6) and remove the battery holder.
4. Install the eight alkaline "C" cells into the battery holder. Ensure the cells are installed in the correct polarity as illustrated on the holder.

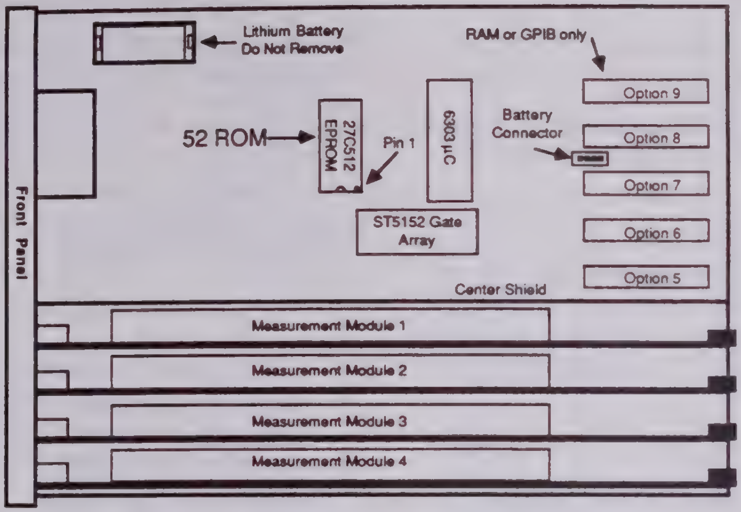

Lithium Battery
Do Not Remove
RAM or GPIB only
Option 9
52 ROM
27C512
EPROM
Pin 1
6303 µC
Battery
Connector
Option 8
Option 7
ST5152 Gate
Array
Option 6
Front Panel
Center Shield
Option 5
Measurement Module 1
Measurement Module 2
Measurement Module 3
Measurement Module 4

Figure 2-4. Model 51 or 52 Internal Locator

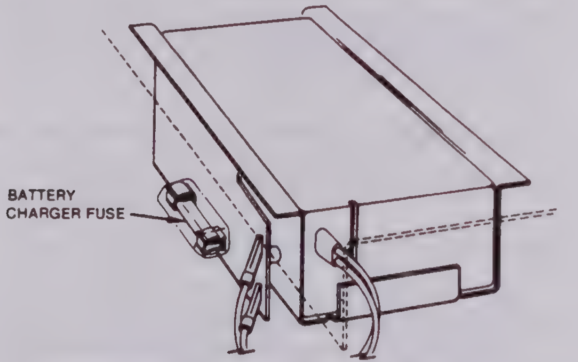

BATTERY
CHARGER FUSE

Figure 2-5. Battery Charger Fuse

5. Rotate each cell inside the holder ½ turn to ensure all contacts are seated and making good connection.
6. Replace the battery holder in the housing and close the housing cover; see figure 2-6.
7. Connect the battery cable to the circuit board; see figure 2-4.
8. Replace the top cover by reversing the steps shown in figure 2-3.

2.3.2 RAM Backup Battery

Whenever a calibration is performed on the unit, the lithium RAM backup battery should be tested.; see figure 2-4. In addition, 50-12A expansion RAM boards, if installed, have a flat lithium battery that should be tested; see drawing 1100-00-2947 located in the rear of this manual.

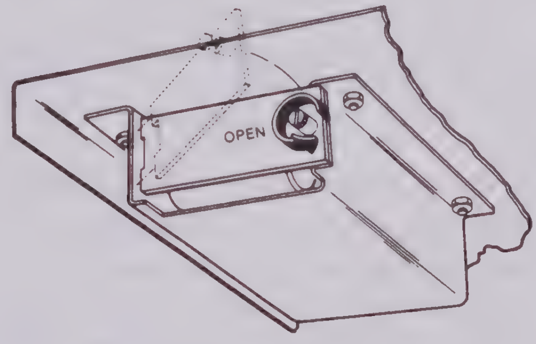


Figure 2-6. Battery Housing

To check the RAM backup batteries, use the following procedure.

1. Remove the top cover; see figure 2-3.
2. With the batteries in their holders, measure each battery voltage. Replace the batteries if they measure less than 2.75V, or replace the them every five years, whether they were used for backup or not. Replace the battery on the motherboard with a 2/3A lithium battery, and replace the battery on the 50-12A expansion RAM board with a "coin cell" lithium battery.

NOTE

To avoid losing the calibration settings, programs or data, replace the lithium battery with the wall transformer plugged in and the multimeter turned off.

3. Replace the top cover by reversing the steps shown in figure 2-3.

2.4 OPTION REPLACEMENT

The following procedure describes the installation and replacement of the RAM Board (Option 50-12)
IEEE-488 Board (Option 50-13)
Digital I/O Board (Option 50-14)

1. Disconnect the power source as follows. If using external power, unplug the power source at the rear panel. If using internal power, remove the top cover (figure 2-3) and disconnect the Battery Connector J6 (figure 2-4).

CAUTION

After power is removed, allow greater than 1 minute for power supply discharge, otherwise the option board could be damaged when plugged into the connector.

2. After the top cover has been removed (figure 2-3), remove, install, or replace the option board. Figure 2-4 illustrates the connector locations, and table 2-1 shows the possible locations of the option boards.
3. If applicable, connect the battery (see figure 2-4).
4. Replace the top cover (see figure 2-3).
5. If applicable, connect the external power source.
6. If a RAM Board (Option 50-12) has been installed, the memory must be cleared by holding down the *Clear* key while pressing *Power* on.

2.5 PROM REPLACEMENT

The following procedure describes how to replace the Programmable Read Only Memory (PROM).

1. Disconnect the power source as follows. If using external power, unplug the Power connector from the rear panel. If using internal power, remove the top cover (figure 2-3) and disconnect the Battery Connector J6 (figure 2-4).

CAUTION

After power is removed, allow greater than 1 minute for power supply discharge, otherwise the option board could be damaged when plugged into the connector.

2. After the top cover has been removed (figure 2-3), locate and remove the PROM U5; see figure 2-4. Gently pry loose the PROM and remove it.
3. Plug in the replacement PROM making sure it is placed correctly in the socket. Note the location of pin 1 in figure 2-4.
4. If applicable, connect the battery (see figure 2-4).
5. Replace the top cover (see figure 2-3).
6. If applicable, connect the power source.
7. Verify the PROM is installed correctly by turning on the power and locating and selecting CONFIG in the main menu. The configuration screen should show the new software revision on the display.

Table 2-1. Possible Location For The Option

	Option Position				
Option Board	**Option Position 9**	**Option Position 8**	**Option Position 7**	**Option Position 6**	**Option Position 5**
RAM (50-12)	X	X	X	X	X
Digital I/O (50-13)		X	X	X	X
GPIB (50-14)	X	X			

X = Boards can be installed in this position.
[BLANK] = Boards *cannot* be installed in this position.

2.6 MEASUREMENT MODULE REPLACEMENT

The following procedures describe how to replace the Measurement Modules. Refer to assembly drawings 1100-00-0464 and 1100-00-0465 which are located in the rear of this manual.

2.6.1 Preparation

1. Disconnect the power source as follows. If using external power, unplug the Power connector from the rear panel.

CAUTION

After power is removed, allow greater than 1 minute for power supply discharge, otherwise the Measurement Module could be damaged when plugged into the connector.

2. If using internal power, remove the top cover (figure 2-3) and disconnect the Battery Connector J6 (figure 2-4).
3. Remove the bottom cover, which is similar to removing the top cover (figure 2-3).

2.6.2 To remove the Measurement Module

1. Disconnect the Measurement Module cable at the motherboard.
2. Disconnect the two wires from the rear panel input connectors.
3. Remove the Measurement Module's two jack screws from the rear panel.
4. Push the Measurement Module out through the front panel.

2.6.3 To install the Measurement Module

1. Slide the Measurement Module in through the front panel.
2. Attach the Measurement Module at the rear panel with two jack screws.
3. Connect the two wires to the rear panel input connectors.

   Red wire to red connector.
   Black wire to the black connector.
4. Connect the Measurement Module cable to the motherboard. Make sure the cable is connected to the correct socket; for example, the cable for a Measurement Module in channel 1's slot must connect to the Chan 1 socket on the motherboard.
5. When connecting the cable to the motherboard, make sure the LED is installed in the correct location.
   - a. For a single channel install the LED in the DS5 position.
   - b. For three channels install the LED in the DS7 position.
   - c. For two or four channels remove the LED entirely.

2.6.4 Closing Up

1. Replace the bottom cover which is similar to replacing the top cover (figure 2-3).
2. Replace the top cover (figure 2-3). Remember to connect the internal batteries if Option 50-10 or 50-11 is installed.

SECTION 3
VERIFICATION PROCEDURES

3.1 THE VERIFICATION PROCEDURE

This procedure checks out the operation of the following parts of the Models 51 and 52.

Paragraph 3.5 — Model 50-1 Measurement Module
Paragraph 3.5 — Model 50-2 Measurement Module
Paragraph 3.6 — RS-232 Interface
Paragraph 3.7 — Model 50-13 IEEE-488 Interface
Paragraph 3.8 — Model 50-14 Digital I/O Board
Paragraph 3.9 — Model 50-12 Memory Expansion Board
Paragraph 3.10 — Option 50-10 Primary Battery
Option 50-11 Rechargeable Battery
Paragraph 3.11 — Option 50-20 Multiplexer

Following the verification procedure is a verification record (paragraph 3.12) which can be copied and used to enter the data from the procedure.

If a check fails to meet the limits, the unit may need calibration. Reference to items that can be calibrated are designated by “”IF NOT — ...”. If the item can not be calibrated or does not work at all, refer to Section 6, Troubleshooting.

3.2 REQUIRED TEST EQUIPMENT

The equipment required to perform the verification procedures are listed in table 3-1.

Table 3-1. Required Test Equipment

Equipment	Manufacturer	Specification
Precision Calibrator	Datron 4700 (recommended)	
Precision Calibrator	Fluke 5100 (alternate)	With wideband option
Precision Thermometer		±0.1°C Accuracy
Precision Frequency		2ppm or better, 1MHz WWV down converter or equivalent.
Short		<1mΩ
RS-232	Terminals: ADDS Viewpoint, DEC VT52, or VT220. Tandy 100 or 200. Programs: TERM, VTERM, RED RYDER, or MIRROR	Dumb Terminal or Computer with a terminal mode or program.
IEEE-488 Controller	Commodore 8032. Commodore 64 with IEEE-488 adapter. IBM PC AT or XT with National Instruments or Data Translation IEEE-488 plug-in card.	
Digital I/O Test Connector	Wavetek Accessory 50-32	Wavetek Option 50-14 must be installed in the Model 51 or 52.

3.3 INITIAL CHECKS

1. Connect the Model 52 to external power.
2. Power on the multimeter; main menu is displayed.
3. Press Range.

   Select CAL STATUS.
   Verify that the "LAST CAL'D" date within a year of today's date.
   Verify that the line frequency is correct — 50 Hz or 60 Hz.

IF NOT — recalibrate using table 4-2.

3.4 INITIAL SETUP

1. Set up a test channnel list which includes all measurement modules. Refer to paragraph 4.6 of the *Models 51 and 52 Operator's Manual.*
2. For example: Set up a channel list named TEST.

   Locate and select "Channel List" from the main menu.
   Enter the channel list's name: "TEST".
   Press Enter.
   Press 1, 2, 3, or 4 to select a measurement module, or press 1, ±, 4 to select all four measurement modules.
   Press Range and select "Auto".
   Press Enter twice.
   Note: the default function is Vdc.

3.5 MEASUREMENT MODULE CHECKS

The following steps verify the calibration of the Models 50-1 and 50-2 measurement modules.

3.5.1 DC Voltage Checks (Models 50-1 and 50-2)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) Func: Vdc and Range: Auto. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Short each Hi to Lo measurement module input connector.

VERIFY AND RECORD

Measurements should read <6 counts on the display.

IF NOT — rezero the measurement module; refer to table 4.2, steps 8, 9, and 10.

4. Remove the short from input connector. Connect all Hi and Lo input connectors to the precision dc voltage calibrator and apply the input voltage.

VERIFY AND RECORD

Read all measurement modules at once.

	Input Voltage	Min Reading	Max Reading
1.	+2.000mV	+1.994mV	+2.006mV
2.	−2.000mV	−1.994mV	−2.006mV
3.	+30.000mV	+27.982mV	+30.018mV
4.	−30.000mV	−27.982mV	−30.018mV
5.	+40.000mV	+37.97mV	+40.03mV
6.	−40.000mV	−37.97mV	−40.03mV
7.	+300.000mV	+297.87mV	+300.13mV
8.	−300.000mV	−297.87mV	−300.13mV
9.	+400.000mV	+399.7mV	+400.3mV
10.	−400.000mV	−399.7mV	−400.3mV
11.	+3.00000V	+2.9987V	+3.0013V
12.	−3.00000V	−2.9987V	−3.0013V
13.	+30.0000V	+27.9878V	+30.013V
14.	−30.0000V	−27.9878V	−30.013V

WARNING

Dangerously high voltages are present in the next two steps.

15.	+300.000V	+297.87V	+300.13V
16.	−300.000V	−297.87V	−300.13V

5. Disconnect the calibrator.

IF NOT — recalibrate using table 4-2 steps 11 through 30.

3.5.2 Cold Junction Temperature Check (Models 50-1 and 50-2)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for Func: CJ TEMP (Cold Junction Temperature). Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Insert the precision laboratory thermometer into the Lo V input of the first measurement module. Wait approximately 2 minutes for the temperature to stablize.

VERIFY AND RECORD

The cold junction temperature must read within ±0.5°C of the thermometer reading.

4. Repeat step 3 of this check for all other Model 50-1 and 50-2 measurement modules.

IF NOT — recalibrate using table 4-2 steps 31 through 33.

5. Remove thermometer from input.

3.5.3 AC Voltage Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for **Func:** Vac and **Range:** Auto. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual*.
3. Connect all Model 50-1 measurement module Hi and Lo input connectors to the precision ac voltage calibrator and apply the correct input voltage.

VERIFY AND RECORD

	Input Voltage	Freq (Hz)	Min Reading	Max Reading
1.	3.000mV	300	2.955mV	3.095mV
2.	3.000mV	30k	2.910mV	3.140mV
3.	20.000mV	300	19.870mV	20.130mV
4.	20.000mV	10k	19.870mV	20.130mV
5.	20.000mV	30k	19.747mV	20.260mV
6.	40.000mV	10k	37.68mV	40.32mV
7.	40.000mV	30k	37.39mV	40.61mV
8.	200.00mV	50	198.88mV	201.12mV
9.	200.00mV	10k	198.88mV	201.12mV
10.	200.00mV	30k	197.78mV	202.21mV
11.	400.00mV	10k	396.8mV	403.2mV
12.	2.0000V	10k	1.9888V	2.0112V
13.	2.0000V	30k	1.9779V	2.0221V
14.	3.0000V	100	2.9838V	3.0162V
15.	20.000V	10k	19.888V	20.112V
16.	10.000V	30k	9.879V	10.121V

WARNING

Dangerously high voltages are present in the next two steps.

	Input Voltage	Freq (Hz)	Min Reading	Max Reading
17.	100.00V	10k	99.29V	100.71V
18.	100.00V	20k	98.79V	101.21V

CAUTION

Place the calibrator in the Standby mode.

4. Connect the wideband option of the 5100 Calibrator to the Model 52. The Datron Model 4200 does not require a wideband option. Terminate the calibrator into 50Ω (±0.1%) (Fluke 5100 only) at the Model 50-1 Hi and Lo inputs.

VERIFY AND RECORD

	Input Voltage	Freq (Hz)	Min Reading	Max Reading
1.	20.000mV	100k	19.340mV	20.660mV
2.	200.00mV	100k	195.70mV	204.30mV
3.	200.00mV	300k	193.40mV	206.60mV
4.	2.0000V	100k	1.9570V	2.0430V
5.	2.0000V	300k	1.9340V	2.0660V

Change the range of each Model 50-1 measurement modules to 30V (**Range:** 30V).

	Input Voltage	Freq (Hz)	Min Reading	Max Reading
6.	3.0000V	100k	2.910V	3.090V
7.	3.0000V	300k	2.850V	3.150V

5. Place the calibrator in the standby mode. Disconnect the calibrator from the measurement module inputs.

IF NOT — recalibrate using table 4-2 steps 36 through 42.

3.5.4 Zero Resistance Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for **Func:** Ohms and **Range:** 30Ω. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual*.
3. Connect the Short across the Hi and Lo inputs of the first measurement module.

VERIFY AND RECORD

The display should read <0.005Ω.

4. Repeat step 3 of this check for each Model 50-1 measurement module.

IF NOT — recalibrate using table 4-2 steps 44 through 50.

5. Remove the short from the input.

3.5.5 Resistance (>1kΩ) Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for **Func:** Ohms and **Range:** Auto. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual*.
3. Connect the test resistors to the first measurement module input (Hi and Lo). Check only one measurement module at a time.

VERIFY AND RECORD

	Test Resistor	Min Reading	Max Reading
1.	10MΩ	9.979MΩ	10.021MΩ
2.	1MΩ	0.9989MΩ	1.0011MΩ
3.	100kΩ	99.92kΩ	100.08kΩ
4.	10kΩ	9.992kΩ	10.008kΩ
5.	1kΩ	0.9992kΩ	1.0008kΩ

4. Repeat step 3 of this check for all other Model 50-1 measurement modules.

IF NOT - recalibrate using table 4-2 steps 52 through 55.

5. Disconnect the test resistors from the inputs.

3.5.6 Resistance (⩽100Ω) Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP". When using four-wire resistance measurements, the rear panel inputs must be selected (Channels 1_{00}, 2_{00}, 3_{00}, 4_{00}).
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for Func: Ohms and Range: Auto. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Set up the first measurement module for four-wire resistance measurements; refer to figure 3-1 and paragraph 4.5.2.6 of the *Models 51 and 52 Operator's Manual.*

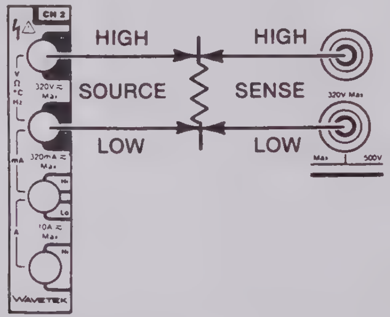


Figure 3-1. Four-Wire Resistance.

VERIFY AND RECORD

	Test Resistor	Min Reading	Max Reading
1.	100Ω	99.92Ω	100.08Ω
2.	10Ω	9.986Ω	10.014Ω

4. Repeat step 3 for all other Model 50-1 measurement modules.

IF NOT — recalibrate using table 4-2 steps 58 through 60.

5. Disconnect the test resistor.

3.5.7 DC Current (mA) Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for Func: Adc and Range: Auto mA. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Connect a precision current calibrator to the middle two inputs (mA) of the first measurement module.

VERIFY AND RECORD

	Test Current	Min Reading	Max Reading
1.	+20.000mA	+19.980mA	+20.020mA
2.	−20.000mA	−19.980mA	−20.020mA
3.	+200.00mA	+199.85mA	+200.15mA
4.	−200.00mA	−199.85mA	−200.15mA
5.	+1.000mA	+0.994mA	+1.006mA

4. Repeat step 3 of this check for all other Model 50-1 measurement modules.

IF NOT — recalibrate using table 4-2 steps 64 through 69.

5. Disconnect the measurement module from the calibrator.

3.5.8 DC Current (A) Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for Func: Adc and Range: 3A. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Connect a precision current calibrator to the bottom two inputs (A) of the first measurement module.

VERIFY AND RECORD

	Test Current	Min Reading	Max Reading
1.	+1.99999A	+1.9974A	+2.0026A
2.	−1.99999A	−1.9974A	−2.0026A

4. Repeat step 3 of this check for all other Model 50-1 measurement modules.

IF NOT — recalibrate using table 4-2 steps 70 through 72.

5. Change the range to 10A (Range: 10A).
6. Connect a precision current calibrator to the bottom two inputs (A) of the first measurement module.

VERIFY AND RECORD

	Test Current	Min Reading	Max Reading
1.	+1.99999A	+1.997A	+2.003A
2.	−1.99999A	−1.997A	−2.003A

7. Repeat steps 5 and 6 of this check for all other Model 50-1 measurement modules.

IF NOT — recalibrate using table 4-2 steps 73 through 74.

8. Disconnect the measurement modules from the current source.

3.5.9 AC Current (mA) Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for **Func:** Aac and **Range:** Auto mA. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Connect a precision ac current calibrator to the middle two inputs (mA) of the first measurement module.

VERIFY AND RECORD

	Input Current	Freq (Hz)	Min Reading	Max Reading
1.	20.000mA	300	19.870mA	20.020mA
2.	3.000mA	300	2.895mA	3.105mA
3.	200.00mA	300	198.88mA	201.12mA

4. Repeat step 3 of this check for all other Model 50-1 measurement modules.

IF NOT — recalibrate using table 4-2 steps 75 through 77.

5. Disconnect the measurement module from the current source.

3.5.10 AC Current (A) Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for **Func:** Aac and **Range:** 3A. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Connect a precision ac current calibrator to the bottom two inputs (A) of the first measurement module.

VERIFY AND RECORD

	Input Current	Freq (Hz)	Min Reading	Max Reading
1.	1.99999A	300	1.9810A	2.0190A

4. Repeat step 3 of this check for all other Model 50-1 measurement modules.

IF NOT — recalibrate using table 4-2 steps 78 and 79.

5. Change the range to 10A (**Range:** 10A).

VERIFY AND RECORD

	Input Current	Freq (Hz)	Min Reading	Max Reading
1.	1.99999A	300	1.978A	2.022A

6. Repeat step 5 of this check for all other Model 50-1 measurement modules.
7. Place the calibrator in standby and disconnect the inputs to the measurement modules.

IF NOT — recalibrate using table 4-2 step 80.

3.5.11 Frequency Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for **Func:** Freq, **Range:** Auto, **Disp:** RES, 9999999. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Connect a precision frequency source to the top two inputs (Hi and low) of the first measurement module. Any one of the five "Input Frequencies" listed below can be used to check the measurement module.

VERIFY AND RECORD

	Input Frequency	Min Reading	Max Reading
1.	1.000000 MHz	0.9999999 MHz	1.000001 MHz
2.	100.0000 kHz	99.99999 kHz	100.0001 kHz
3.	10.00000 kHz	9.999999 kHz	10.00001 kHz
4.	1.000000 kHz	0.9999999 kHz	1.000001 kHz
5.	100.000Hz	99.99999Hz	100.0001Hz

4. Repeat step 3 of this check for all other Model 50-1 measurement modules.

5. Disconnect the frequency source from the measurement module.

IF NOT — recalibrate using table 4-2 step 81.

3.5.12 Input Sensitivity Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for **Func:** Freq, **Range:** Auto, **Disp:** RES, 9999999. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Connect a precision frequency source to the top two inputs (Hi and low) of all the measurement modules. Set the frequency source to 10 kHz at 350 mV rms.

VERIFY AND RECORD

Record the reading for each Model 50-1 measurement module. All measurement modules must read the same and should be stable.

4. Disconnect the measurement modules from the frequency source.

3.5.13 Input Sensitivity (TTL) Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for **Func:** Logic, **Mods:** SENST, TTL. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Connect a precision voltage source to the top two inputs (Hi and low) of all the Model 50-1 measurement modules.
4. Increase voltage source from 0.0V to +2.2V in 0.1V steps.

VERIFY AND RECORD

   1. As the input voltage increases (starting at 0.0V), each channel reading should change from "0" to "1" when the input voltage is between +1.8V and +2.2V.
   2. As the input voltage decreases (starting at +2.2V), each channel reading should change from "1" to "0" when the input voltage is between +1.0V and +0.6V.

5. Disconnect the measurement module from the voltage source.

3.5.14 Input Sensitivity (CMOS) Check (Model 50-1 only)

1. Set up the Model 52 as described in paragraph 3.4 "INITIAL SETUP".
2. Select TEST channel list from the main menu and set up all channels (measurement modules) for **Func:** Logic, **Mods:** SENST, CMOS5. Refer to paragraph 4.6.2 of the *Models 51 and 52 Operator's Manual.*
3. Connect a precision voltage source to the top two inputs (Hi and low) of all the Model 50-1 measurement modules.
4. Increase voltage source from 0.0V to +3.7V in 0.1V steps.

VERIFY AND RECORD

   1. As the input voltage increases (starting at 0.0V), each channel reading should change from "0" to "1" when the input voltage is between +3.3V and +3.7V.
   2. As the input voltage decreases (starting at +3.7V), each channel reading should change from "1" to "0" when the input voltage is between +1.7V and +1.3V.

5. Disconnect the measurement module from the voltage source.

3.6 RS-232-C CHECK

1. Connect the RS-232-C terminal to the Model 52. Refer to paragraph 2.3.4 of the *Models 51 and 52 Operator's Manual.*
2. Set the Baud rate of the Model 52 to match the Baud rate of the terminal. Refer to paragraph 2.3.9 of the *Models 51 and 52 Operator's Manual.*
3. Send a "DIR" command to the Model 52.

VERIFY AND RECORD

The Model 52 returns a listing of all stored channel lists and programs. All directory listings terminate with "*END". If no channel lists or programs are stored in the multimeter, the Model 52 will return a "*END".

For example:

```
TEST.L
*END
```

4. Disconnect the RS-232 terminal from the Model 52.

3.7 IEEE-488 CHECK

1. Power On.

NOTE

The IEEE-488 option will only operate when the Model 52 is powered from an appropriate external power source.

2. From the main menu select "CONFIGURATION".

VERIFY AND RECORD

Verify the unit contains IEEE-488 (GPIB) board. Press Menu to return to the main menu.

3. Connect the IEEE-488 controller to the Model 52. Refer to paragraph 2.3.5 of the *Models 51 and 52 Operator's Manual.*
4. Set the IEEE-488 Address of the Model 52 to match the IEEE-488 Address of the terminal. Refer to paragraph 2.3.5 of the *Models 51 and 52 Operator's Manual.*
5. Send a "DIR" command to the Model 52. Check the Operator's manual for your IEEE-488 controller on how to send commands to the multimeter.

VERIFY AND RECORD

The Model 52 returns a listing of all stored channel lists and programs. All directory listings terminate with "*END". If no channel lists or programs are stored in the multimeter, the Model 52 will return a "*END".

For example:
TEST.L
*END

6. Disconnect the IEEE-488 controller from the Model 52.

3.8 DIGITAL I/O CHECK

1. Power On.
2. From the main menu select "CONFIGURATION".

VERIFY AND RECORD

Verify the unit contains Digital I/O board. Note the Digital I/O channel numbers. Press Menu to return to the main menu.

3. Set up a test channel list which includes all Digital I/O channels. Refer to paragraph 4.6 of the *Models 51 and 52 Operator's Manual.*

   For example: Set up a channel list named DTEST which produces a digital output byte from channel 5 and reads a digital input byte on the same channel.

   Locate and select "Channel List" from the main menu.
   Enter the channel list's name: "DTEST".
   Press Enter.
   Press 5, 1, 0 to select a digital output byte on channel 5.
   Press Func and select INCRMT to increment the output each reading.
   Press Func and select DELAY. Enter 2 (002) for a 0.2 second delay.
   Press Disp and select BCD to display the output value in BCD.
   Press 5, 0, 0 to read a digital input byte on channel 5.
   Press Disp and select BCD to display the input value in BCD.
   Press Enter twice.
4. Connect the outputs on the Digital I/O connector to the inputs on the same connector; see figure 3-2. HINT: Using the Wavetek Accessory 50-32 will make this task much easier.
5. Select DTEST channel list from the main menu and it; refer paragraph 4.6.4 of the *Models 51 and 52 Operator's Manual.*

VERIFY AND RECORD

Compare the displayed output byte with the displayed input byte; they must read the same. The digital output byte should increment each time the output channel is read. The 0.2 second delay makes it easier to observe the reading.

6. Repeat steps 3 through 5 for each Digital I/O channel.
7. Disconnect digital I/O connector from the multiplexer.

3.9 MEMORY EXPANSION CHECK

1. Power On.
2. From the main menu select "CONFIGURATION".

VERIFY AND RECORD

Check the location and memory capacity of the RAM boards. Press Menu to return to the main menu.

3. From the main menu select "MEMORY STATUS".

VERIFY AND RECORD

Verify the total memory capacity from step to equal the total memory capacity displayed.

4. Press Menu to return to the main menu. Select DATA ROUTING and from this menu select STORE: CH LIST. Refer to paragraph 4.4.1 of the *Models 51 and 52 Operator's Manual.*

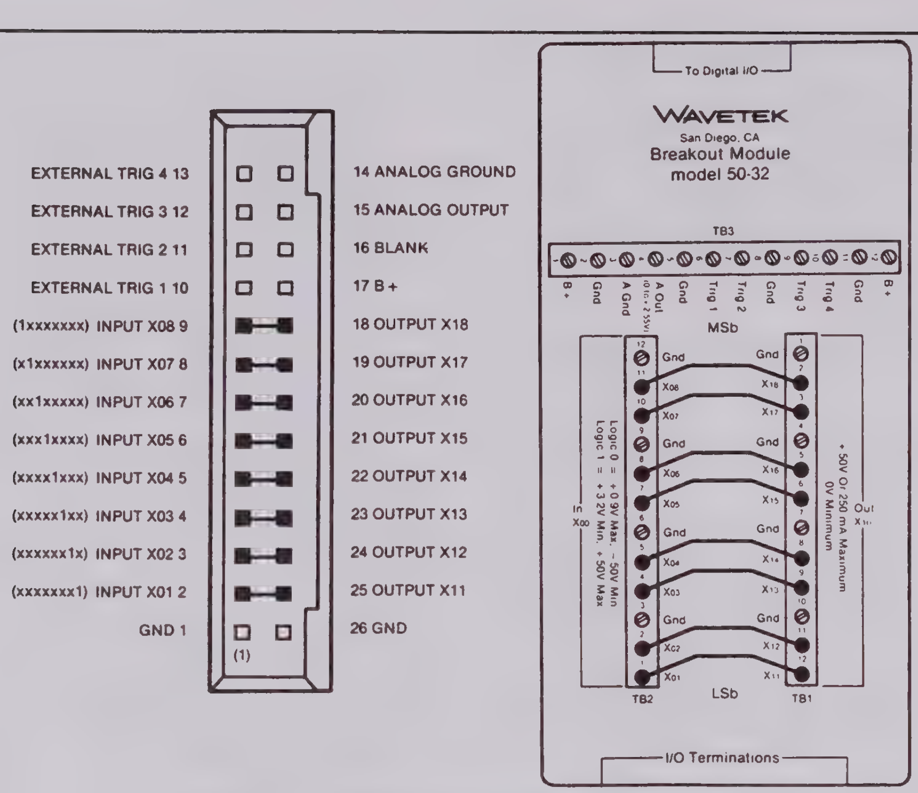

EXTERNAL TRIG 4 13
EXTERNAL TRIG 3 12
EXTERNAL TRIG 2 11
EXTERNAL TRIG 1 10
(1xxxxxxx) INPUT X08 9
(x1xxxxxx) INPUT X07 8
(xx1xxxxx) INPUT X06 7
(xxx1xxxx) INPUT X05 6
(xxxx1xxx) INPUT X04 5
(xxxxx1xx) INPUT X03 4
(xxxxxx1x) INPUT X02 3
(xxxxxxx1) INPUT X01 2
GND 1
(1)
14 ANALOG GROUND
15 ANALOG OUTPUT
16 BLANK
17 B +
18 OUTPUT X18
19 OUTPUT X17
20 OUTPUT X16
21 OUTPUT X15
22 OUTPUT X14
23 OUTPUT X13
24 OUTPUT X12
25 OUTPUT X11
26 GND
To Digital I/O
WAVETEK
San Diego, CA
Breakout Module
model 50-32
TB3
B +
Gnd
A Gnd
A Out
Gnd
Trig 1
Trig 2
Gnd
Trig 3
Trig 4
Gnd
B +
MSb
Gnd
X08
X07
X06
X05
X04
X03
X02
X01
X18
X17
X16
X15
X14
X13
X12
X11
Logic 0 = +0.9V Max, −50V Min
Logic 1 = +3.2V Min, +50V Max
In
X00
+50V Or 250 mA Maximum
0V Minimum
Out
TB2
LSb
TB1
I/O Terminations

Figure 3-2. Digital I/O Check Interconnections

5. Press **Menu** to return to the main menu. Select DMM. Then press **Chan** **9** and **Enter** to read and store time and date data.
6. Run the DMM for about 1 minute. Then press **Menu** to stop the DMM and return to the main menu.
7. Select RECALL DATA and from this menu select DISPLAY All; refer paragraph 4.4.3 of the *Models 51 or 52 Operator's Manual.*

VERIFY AND RECORD

The display should show the stored time and date data.

3.10 PRIMARY AND RECHARGEABLE BATTERY CHECK

1. Disconnect the Model 52 from the external power source.
2. Power the multimeter on.

VERIFY AND RECORD

The multimeter's display should show the main menu.

3.11 MULTIPLEXER CHECK

1. Connect the Multiplexer (Option 50-20) to the Model 52. See paragraph 2.3.7 "Connecting the Multiplexer to the Model 52" of the *Models 51 and 52 Operator's Manual.*
2. On the Multiplexer, set switch S1 position 1 to "TEMP EN"; see figure 2-11 of the *Models 51 and 52 Operator's Manual.*
3. Set up the Multiplexer for single ended configuration and enable Multiplexer channels 1-8 and 9-16 (S1 positions 10 and 9); refer to paragraph 2.3.7 "Setting Up the Multiplexer — Single Ended Setup" of the *Models 51 and 52 Operator's Manual.*
4. Power on the multimeter.
5. Set up a test channel list which measures the cold junction temperature of the multiplexer.

   For example:

   Locate and select CHANNEL LIST in the main menu.
   Enter the channel list name: MUXCK.

   Press **Enter**.

   Press **1**, **0**, **1**.

   Press **Func** and select CJ TEMP.

   Press **Enter** twice.

6. Select "MUXCK" from the main menu and run that channel list; refer to paragraph 4.6.4 of the *Models 51 and 52 Operator's Manual.*

VERIFY AND RECORD

The display shows the multiplexer's cold junction temperature.

3.12 VERIFICATION RECORD

The verification record provides a place to record the data taken during the Verification Procedure. This record should be copied and used with the procedure. The paragraph numbers (¶ 3.5) in the record refer to paragraph numbers in the procedure.

Models 51 and 52
VERIFICATION RECORD

Date: ________/________/________

Serial Number ________________

Last Calibration Date (¶ 3.3): ________/________/________.

Line Frequency (¶ 3.3): ______________ Hz.

DC Voltage Check (¶ 3.5.1)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
Short				
+ 2mV				
− 2mV				
+ 30mV				
− 30mV				
+ 40mV				
− 40mV				
+ 300mV				
− 300mV				
+ 400mV				
− 400mV				
+ 3V				
− 3V				
+ 30V				
− 30V				
+ 300V				
− 300V				

Cold Junction Temperature Check (¶ 3.5.2)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
CJ Temp				

AC Voltage Check (¶ 3.5.3)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
3mV @ 300 Hz				
3mV @ 30 kHz				
20mV @ 300 Hz				
20mV @ 10 kHz				
20mV @ 30 kHz				
40mV @ 10 kHz				
40mV @ 30 kHz				
200mV @ 50 Hz				
200mV @ 10 kHz				
200mV @ 30 kHz				
400mV @ 10 kHz				
2V @ 10 kHz				

AC Voltage Check (¶ 3.5.3) (Continued)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
2V @ 30 kHz				
3V @ 100 Hz				
20V @ 10 kHz				
10V @ 30 kHz				
100V @ 10 kHz				
100V @ 20 kHz				
20mV @ 100 kHz				
200mV @ 100 kHz				
200mV 300 kHz				
2V @ 100 kHz				
2V @ 300 kHz				
3V @ 100 kHz				
3V @ 300 kHz				

Zero Resistance Check (¶ 3.5.4)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
Short				

Resistance (>1kΩ) Check (¶ 3.5.5)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch**
10MΩ				
1MΩ				
100kΩ				
10kΩ				
1kΩ				

Resistance (<1kΩ) Check (¶ 3.5.6)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
100Ω				
10Ω				

DC Current (mA) Check (¶ 3.5.7)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
+20mA				
−20mA				
+200mA				
−200mA				
+1mA				

DC Current (A) Check, Range: 3A (¶ 3.5.8)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
+ 1.99999mA	________	________	________	________
− 1.99999mA	________	________	________	________

DC Current (A) Check, Range: 10A (¶ 3.5.8)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
+ 1.99999mA	________	________	________	________
− 1.99999mA	________	________	________	________

AC Current (mA) Check (¶ 3.5.9)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
20mA @ 300Hz	________	________	________	________
3mA @ 300Hz	________	________	________	________
200mA @ 300Hz	________	________	________	________

AC Current (A) Check, Range: 3A (¶ 3.5.10)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
1.99999A @ 300Hz	________	________	________	________

AC Current (A) Check, Range: 3A (¶ 3.5.10)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
1.99999A @ 300Hz	________	________	________	________

Frequency Check (¶ 3.5.11)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
See ¶ 3.5.11, Step 3	________	________	________	________

Input Sensitivity Check (¶ 3.5.12)

Enter reading.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
Record displayed frequency	________	________	________	________

Input Sensitivity (TTL) Check (¶ 3.5.13)

Enter transition voltage.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
Record "0" to "1" level	________	________	________	________
Record "1" to "0" level	________	________	________	________

Input Sensitivity (CMOS) Check (¶ 3.5.13)

Enter transition voltage.

Input	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
Record "0" to "1" level	______	______	______	______
Record "1" to "0" level	______	______	______	______

RS-232-C Check (¶ 3.6)

Multimeter returns directory: ______________ (✓).

IEEE-488 Check (¶ 3.7)

Multimeter returns directory: ______________ (✓).

Digital I/O Check (¶ 3.8)

Enter ✓.

	Ch 5	**Ch 6**	**Ch 7**	**Ch 8**
Digital input reads digital output.	______	______	______	______

Memory Expansion Check (¶ 3.9)

Total memory capacity from "CONFIGURATION" menu equal total memory capacity from "MEMORY STATUS" menu: ________________ (✓).

Stored Recall — Correct stored data recalled: ________________ (✓).

Multiplexer Check (¶ 3.10)

Cold junction temperatures displayed: ________________ (✓).

SECTION 4
CALIBRATION PROCEDURE

4.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

4.2 REQUIRED TEST EQUIPMENT

The test equipment required to perform the calibration procedures are listed in table 4-1.

Table 4-1. Required Test Equipment

Equipment	Manufacturer	Specification
Precision Calibrator	Datron 4700 (Recommended)	
Precision Calibrator	Fluke 5100 (Alternate)	With wideband option
Precision Thermometer		±0.1°C Accuracy
Precision Frequency		2ppm or better, 1MHz WWV down converter or equivalent.
DMM		
Short		<1mΩ

4.2.1 Calibrating the Models 51 and 52

Models 51 and 52 use a calibration process called "Flex-Cal". Flex-Cal means there is no need to open the box or make internal adjustments. All adjustments are made with internal software. To calibrate the Model 51 or 52, set up the unit and apply the proper input as shown in table 4-2. The Model 51 or 52 does the rest.

Model 52 front panel keys are illustrated as white letters in a black box.

NOTE

The completion of the calibration procedure returns the instrument to correct alignment.

CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS

Instrument specifications are given in Section 1 of the Models 51 and 52 Operators Manual.

Table 4-2. Calibration Procedure

Step	Check	Calibrator Set Up	51/52 Set Up	Remarks
1	**Initial Power Procedure**		Select CAL ENable on rear panel DIP switch.	See Paragraph 2.3.9, Item 6.[1] Set all other switches as required.
2			Connect power.	If power on, turn it off.
3	**Initialize**		Hold in **Clear** while pressing **Power**.	If "CALS PROBABLY CORRUPTED" appears, select "OK" to load default calibration.

[1] Refer to Model 51 and 52 Operator's Manual.

Table 4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	51/52 Set Up	Remarks
4	**Time/Date**		Select Time/Date from main menu. Select Time.	Verify time is correct. If incorrect, set the time (see para graph 4.3.6).[1]
			Select Date.	Verify Date is correct. If incorrect, set the date (see paragraph 4.3.6).[1]
5			Press Menu.	
6	Calibration Setup		This calibration procedure requires you to create a channel list that includes each of the measurement modules in the unit.	
7			Select "CHANNEL LIST". Enter Channel List name (for example: "CAL 5"). Press Func and select Vdc. Press Range and select 30 mV.	For more information, see paragraph 4.6[1]. (Set up each channel for Vdc, 20mV.) Allow unit to warmup 5 minutes before calibration.
8	**Vdc** CAL 0		Short Hi to Lo inputs of each channel.	
9			Select the first channel to be zeroed.	To select a channel, push the key next to the channel number (channel number highlighted).
10			Press Range, Press Mods, and select CAL 0.	Verify 30 mV range is selected. Wait
11			When the Mods screen appears, press Range. Select 300mV. Press Mods and select CAL 0.	Wait
12			When the Mods screen appears press Range and select 3V press Mods and select CAL 0.	Wait
13			When the Mods screen appears, press Range and select 30V. Press Mods and select CAL 0.	Wait

[1] Refer to Model 51 and 52 Operator's Manual.

Table 4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	51/52 Set Up	Remarks
14			When the Mods screen appears, press **Range** and select 300V. Press **Mods** and select CAL 0.	Wait
15			When the Mods screen appears press **Range** and select AUTO.	If the reading is >2 counts off, recalibrate zero for the 30 mV range (step 9).
16			Press **Enter** to return to the channel list display. Repeat steps 9 through 15 for all other channels.	
17	**DC Volts**		Remove short from input.	
18				Connect the calibrator to Hi/Lo inputs.
19			Select the first channel	
20	+ 20 mV	Press **Func** and + 20.000 mV	Press **Func** and select Vdc. Press **Range** and select AUTO. Press **Mods**, select CAL.	Wait until “CALIBRATED” appears.
21	– 20 mV	Set for – 20.000 mV[2]		Wait until “CALIBRATED” appears.
22	+ 200 mV	Set for + 200.000mV[2]		Wait until “CALIBRATED” appears.
23	– 200 mV	Set for – 200.000 mV[2]		Wait until “CALIBRATED” appears.
24	+ 2V	Set for + 2.00000V[2]		Wait until “CALIBRATED” appears.
25	– 2V	Set for – 2.00000V[2]		Wait until “CALIBRATED” appears.
26	+ 20V	Set for + 20.0000V[2]		Wait until “CALIBRATED” appears.
27	– 20V	Set for – 20.0000V[2]		Wait until “CALIBRATED” appears.

[2] Change voltage quickly and smoothly.

Table 4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	51/52 Set Up	Remarks
	WARNING **DANGEROUSLY HIGH VOLTAGES ARE PRESENT IN THE NEXT TWO STEPS.**			
28	+200V	Set for +200.000V[2]	Select CAL	Wait until "CALIBRATED" appears.
29	−200V	Set for −200.000V[2]		Wait until "CALIBRATED" appears.
30		Output Off (4700) Standby (5100) For safety.	Press Enter to return to the channel list display. Repeat steps 20 through 29.	
31	**Cold Junction Temp**			Disconnect all inputs.
32			Select the first channel. Press Func and select CJ TEMP.	Insert a precision lab thermometer into the Lo input of the measurement modules to be calibrated. Allow the thermometer to stabilize about 30s.
33			Press Mods, Select CAL	Enter the temperature value to the nearest resoluable reading in degrees C. (In other words, it the thermometer reads between 24.3 and 24.4°C, enter 24.35).
34			Press Enter to return to the next channel. Repeat steps 33 and 34.	
35	This completes calibration of the Model 50-2 Measurement Module. The remaining calibration steps apply to the Model 50-1 Measurement Module.			
36	**AC Volts**		Select the first channel. Press Func and select Vac. Press Range and select AUTO.	These steps calibrate both the Vac and Vac + dc functions. The only evidence you will have that the Vac + dc function is being calibrated will be two clicks of the relays.
37			Disconnect any input to a Model 50-2 Measurement Module.	

---

[2] Change voltage quickly and smoothly.

Table 4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	51/52 Set Up	Remarks
38	20 mV	20.000 mV at 300 Hz	Press Mods and select CAL.	Wait until the relay clicks twice and "CALIBRATED" appears.
39	200 mV	200.000 mV at 300 Hz		Wait until the relay clicks twice and "CALIBRATED" appears.
40	2V	2.00000V at 300 Hz		Wait until the relay clicks twice and "CALIBRATED" appears.

WARNING

DANGEROUSLY HIGH VOLTAGES ARE PRESENT.

CAUTION

Setting the Calibrator to 20V may place the calibrator in standby. If so, reset the calibrator.

41	20V	20.0000V at 300 Hz		Wait until the relay clicks twice and "CALIBRATED" appears.
42	200V	200.000V at 300 Hz	Select CAL.	Wait until the relay clicks twice and "CALIBRATED" appears.
43				Repeat steps 37-42 for each of the Model 50-1 modules.
44	**Ohms** 30Ω Zero		Select the first channel. Press Func and select Ohms. Press Range and select 30Ω. Short the Hi and Low input to the first channel. Press Mods and select CAL 0.	Wait until the Mods menu appears. If the reading is >0.005 repeat the process.
45	300Ω Zero		Press Range and select 300Ω. Press Mods and select CAL 0.	Wait until the Mods menu appears before continuing on.
46	3kΩ Zero		Press Range and select 3kΩ. Press Mods and select CAL 0.	Wait until the Mods menu appears before continuing.
47	30kΩ Zero		Press Range and select 30kΩ. Press Mods and select CAL 0.	Wait until the Mods menu appears before continuing.

Table 4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	51/52 Set Up	Remarks
48	300kΩ Zero		Press Range and select 300kΩ. Press Mods and select CAL 0.	Wait until the Mods menu appears before continuing.
49	3MΩ Zero		Press Range twice and select 3MΩ. Press Mods and select CAL 0.	Wait until the Mods menu appears before continuing.
50	30MΩ Zero		Press Range and select 30MΩ. Press Mods and select CAL 0.	Wait until the Mods menu appears before continuing.
51				Repeat steps — 44 through 50 — for all of the Model 50-1 modules channels.
52	Ohms Calibration 10MΩ	10MΩ	Remove short and connect Test Resistor across Hi and Lo inputs. Press Range and Select AUTO. Press Mods; Select CAL.	Wait until “CALIBRATED” appears before continuing
53	1MΩ	1MΩ		Wait until “CALIBRATED” appears before continuing.
54	100kΩ	100kΩ		Wait until “CALIBRATED” appears before continuing.
55	10kΩ	10kΩ		Wait until “CALIBRATED” appears before continuing.
56	1kΩ	1kΩ		Wait until “CALIBRATED” appears before continuing.
57				Repeat steps 53 through 58 for all the Model 50-1 Modules.
58	100Ω	100Ω	Connect the 100Ω resistor as shown in figure 4-1.	The following resistance calibration steps require the unit be setup for four-wire measurements (paragraph 4.5.2.6)[1] It will be easier to select the DMM mode. Press Menu, select DMM.

---

[1] Refer to the Models 51 and 52 Operator's Manual.

Table 4-2. Calibration Procedure (Continued)

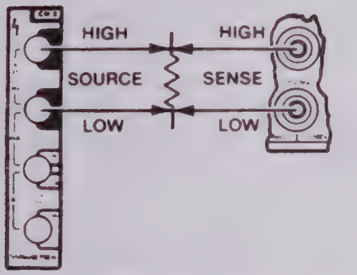


Figure 4-1. Four Wire Measurement

Step	Check	Calibrator Set Up	51/52 Set Up	Remarks
59			Press **Chan** and enter the rear panel subscript (for example, to select the rear panel inputs for channel 1: press **Chan**, **1**, **0**, **0**). Press **Func** and select OHMS. Press **Mods** and select CAL.	Wait until "CALIBRATED" appears before continuing.
60	10Ω	10Ω	Connect the 10Ω resistor as shown in figure 4-1. Press **Mods** and select CAL.	Wait until "CALIBRATED" appears before continuing.
61	MΩ		Disconnect all inputs. Press **Chan** and select the front panel inputs. Press **Func** and select OHMS. Press **Range** twice and select AUTO MΩ. Press **Mods** and select CAL.	Wait until "CALIBRATED" appears before continuing. Reading must be "OVRRNG".
62	100 MΩ TEST	100 MΩ 0.1% resistor	Connect 100 MΩ resistor to front panel inputs.	Reading must be between 95.30 and 103.8MΩ.
63	Optional 1000 MΩ TEST	1000 MΩ 1% resistor	Connect 1000MΩ resistor to front panel inputs.	Reading must be between 960 and 1060MΩ. Repeat steps 53 through 56 and 58 through 62 for all the Model 50-1 channels.

Table 4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	51/52 Set Up	Remarks
64	**Adc**		Connect the calibrator to the middle two (mA) inputs of the Measurement Module to be calibrated. Select the first Model 50-1 channel. Press **Func** and select Adc. Press **Range** and select AUTO mA.	
65	+ 20 mA	+ 20.000 mA	Press **Mods** and select CAL.	Wait until "CALIBRATED" appears before continuing.
66	– 20 mA	– 20.000 mA		Wait until "CALIBRATED" appears before continuing.
67	+ 200 mA	+ 200.000 mA		Wait until "CALIBRATED" appears before continuing.
68	– 200 mA	– 200.000 mA		Wait until "CALIBRATED" appears before continuing.
69	+ 1mA TEST	+ 1.000 mA		Reading must be between 0.995 and 1.005 mA. If not check the CAL 0 of 30 mVdc.
70	3A		Press **Range** and select 3A. Connect the calibrator to the bottom two inputs (A) of the measurement module to be calibrated.	
71	+ 3 A	+ 1.99999 A	Press **Mods** and select CAL.	Wait until "CALIBRATED" appears before continuing.
72	– 3 A	– 1.99999 A		Wait until "CALIBRATED" appears before continuing.
73	– 10 A	– 1.999999A	Press **Range** and select 10A.	Wait until "CALIBRATED" appears before continuing. Press **Mods** and select CAL.
74	+ 10 A	+ 1.99999 A		Wait until "CALIBRATED" appears before continuing. Repeat steps 64 through 74 for all the Model 50-1 Modules.

Table 4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	51/52 Set Up	Remarks
75	**AC Amps**		Connect the calibrator to the middle to (mA) input connectors. Select the first Model 50-1 channel. Press Func and select Aac. Press Range and select AUTO mA.	
76	20 mA	20.000 mA at 300 Hz.	Press Mods and select CAL.	Wait until "CALIBRATED" appears before continuing.
77	200 mA	200.00 mA at 300 Hz.	Press Mods and select CAL.	Wait until "CALIBRATED" appears before continuing.
78	3 A		Connect the calibrator to the bottom two (A) input connectors. Press Range and select 3A.	
79		1.99999A at 300 Hz.	Press Mods and select CAL.	Wait until "CALIBRATED" appears before continuing.
80		1.99999A 300 Hz.	Press Range and select 10A. Press Mods and select CAL.	Wait until "CALIBRATED" appears before continuing. Repeat steps 76 through 80 for all Model 50-1 modules.
81	**Frequency**	Frequency calibration requires a precision frequency source of 1.000000 MHz (100k, 10k, or 100 Hz are acceptable) 2 Vrms.	Connect the precision frequency source to the Hi and Lo inputs to any Model 50-1 Measurement Module. Select any Model 50-1 module. Press Func and select FREQ. Press Range and select AUTO. Press Mods and select CAL. The input sensitivity must be changed if the reference frequency voltage is not 2 Vrms; refer to paragraph 4.5.2.9[1]. Press Enter twice.	Only one Model 50-1 Measurement Module needs to be calibrated. Wait until "CALIBRATED" appears before continuing. This calibrates all the frequency functions on all the Model 50-1 modules.

---

[1] Refer to Model 51 and 52 Operator's Manual.

Table 4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	51/52 Set Up	Remarks
82			Select **Menu** and delete the calibration channel list; see paragraph 4.6.3[1].	This deletes the calibration channel list.
83	CAL ENABLE		Select CAL ENable off (switch closed). See paragraph 2.3.9 item 6[1].	This protects the calibration.

---

[1] Refer to Model 51 and 52 Operator's Manual.

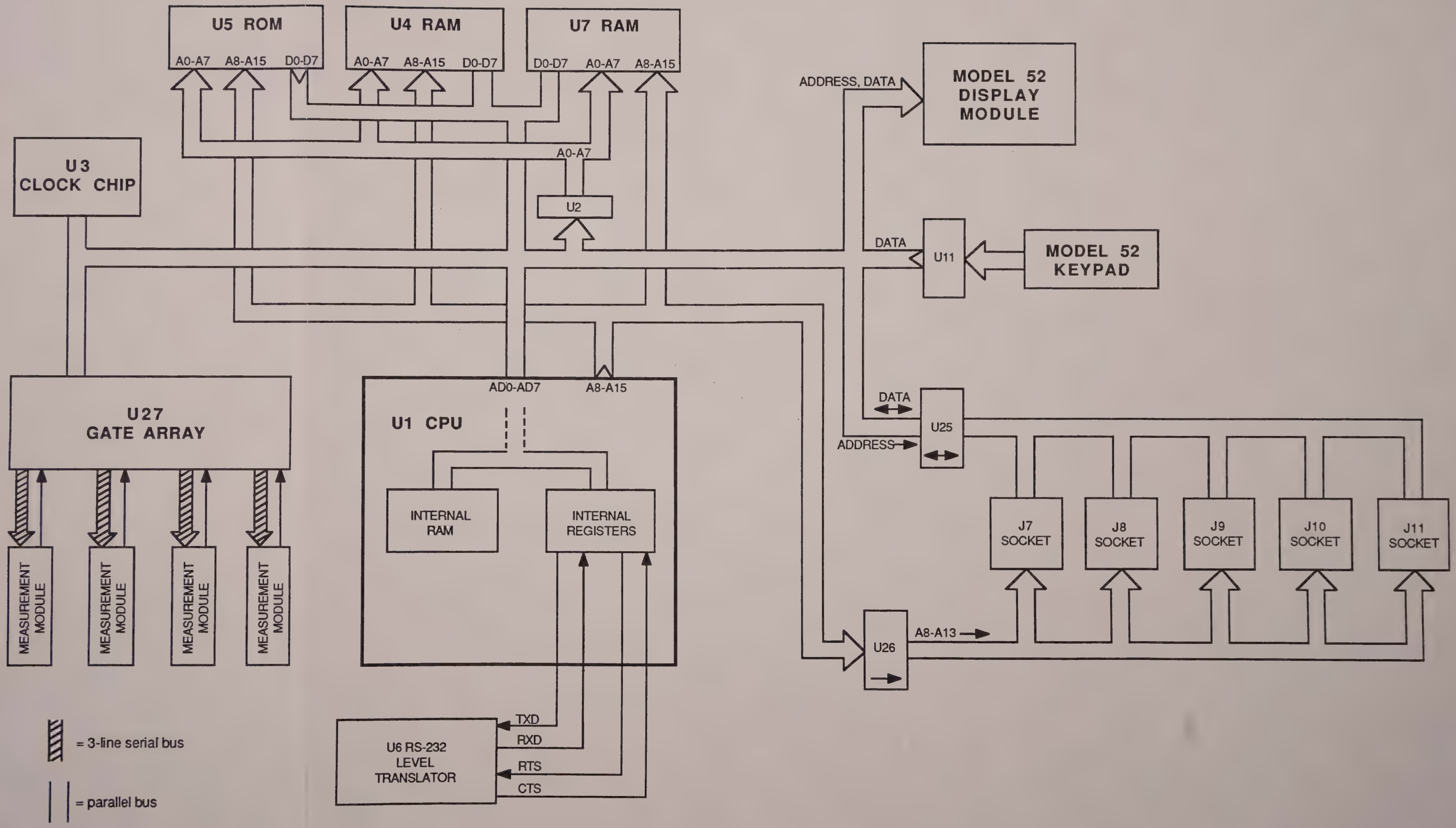

U5 ROM
A0-A7
A8-A15
D0-D7
U4 RAM
A0-A7
A8-A15
D0-D7
U7 RAM
D0-D7
A0-A7
A8-A15
A0-A7
U2
U3
CLOCK CHIP
ADDRESS, DATA
MODEL 52
DISPLAY
MODULE
DATA
U11
MODEL 52
KEYPAD
U27
GATE ARRAY
AD0-AD7
A8-A15
U1 CPU
INTERNAL
RAM
INTERNAL
REGISTERS
DATA
U25
ADDRESS
J7
SOCKET
J8
SOCKET
J9
SOCKET
J10
SOCKET
J11
SOCKET
U26
A8-A13
MEASUREMENT
MODULE
MEASUREMENT
MODULE
MEASUREMENT
MODULE
MEASUREMENT
MODULE
TXD
RXD
RTS
CTS
U6 RS-232
LEVEL
TRANSLATOR
= 3-line serial bus
= parallel bus

Figure 5-1. Buses Internal to the Model 52

SECTION 5

MODEL 52 CIRCUIT DESCRIPTION

5.1 INTRODUCTION

The purpose of this section is to familiarize the user or service personnel with the circuit level operation of the Model 51 or 52, plug-in boards, measurement modules, and multiplexers. This knowledge is helpful in troubleshooting an instrument failure, and may allow users to gain insights that increase the instrument's versatility.

The unexpanded Model 52 chassis comes with a motherboard, display assembly, and a keypad board. The Model 51 has a largely blank front panel instead of a display assembly and keypad. The motherboard for each is the same, with the exception of a few unique components. The motherboard contains the power supply regulators, power on-off control, microprocessor, RS-232-C communications, address decoding, ROM, standard RAMs, real-time clock chip, beeper, and a gate array used for measurement module interface.

Other assemblies within the chassis may include Measurement Modules, (channels 1-4), Digital I/O plug-in boards (rear panel slots 5-8), IEEE-488 (GPIB) plug-in (in one slot, 8 or 9), expansion RAM boards, (slots 5-9), and an internal battery pack. If the battery pack is the rechargable battery option (50-11), a recharger board is mounted on the pack.

Channel switching control signals for any multiplexers connected to an A/D measurement module input come from that measurement module.

Locating Parts Or Signals On The Schematics

Each page of a circuit schematic is divided into physical zones. The circuit description may describe a signal as going to or coming from a zone on the same sheet or another sheet of the schematic. For example, the $\overline{\text{8KRAM}}$ chip select signal comes from U18A-6 (2B7), and goes to U7-20 (1C2). 2B7 means schematic sheet 2, zone B7. 1C2 means sheet 1, zone C2. U18A-6 refers to integrated circuit U18, pin 6. Where the sections of an IC (often separate gates) are used in different areas of the schematic, the sections are usually referenced by letters, as in U18A, and U18B (2A5).

Signal Names

Signal names with a bar over them, such as $\overline{\text{ALARM}}$, denote signals that are active low. Signal names such as R/$\overline{\text{W}}$\ with the backslash after them, denote signals that are the same as the signal without the backslash except the backslash signal is a buffered version.

Numbering Systems

Three numbering systems are used in this maintenance manual: binary, hexadecimal, and decimal. Binary, when used, is obvious by all of the digits being either 1's or 0's. Hexadecimal is used in addressing descriptions because it is a succinct way of denoting the pattern (actually a binary pattern) on the sixteen address lines. Hexadecimal numbers will generally be identified by an H subscript (00_H) after them, if not in a table identified as hexadecimal. If not followed by the H subscript, four-digit numbers can usually be assumed to be decimal. In rare cases where ambiguity may occur, a 10 subscript will follow a decimal number.

Figure 5-1 shows the major blocks of the system from the viewpoint of internal communications. Plug-in boards plug into motherboard connectors J7 through J11. These correspond to rear panel slots 5, 6, 7, 8, and 9.

All communications are between the MPU (microprocessor) and some other block. All buses are parallel, except for the path between the gate array and a measurement module.

Not shown in figure 5-1 are the optoisolators between the gate array and each measurement module. The communication link that passes setups from the gate array to a measurement module is a three line serial data format (data, clock, and latch). Measurement "values" are passed from a measurement module to the gate array as a logic level transition on one line. In A/D conversion, the interval from when the microprocessor sends the latch pulse for a measurement setup to when the measurement module returns the transition is a measure of the amplitude of the measured signal. Software converts these intervals into meaningful, displayable characters.

The Model 51 and 52 operating firmware is stored in the U5 ROM, containing 64KBytes. The clock chip serves three functions: to keep track of real time, to time power down intervals, and to drive the beeper when commanded by the microprocessor.

An unexpanded unit comes with two standard RAMs, U7 and U4. These provide a basic memory of 16KBytes. Due to the amount of memory used by the unit's operating system, about 9.5K is available to the user. The amount of memory recognized by the microprocessor can be checked by using the MEMORY STATUS menu.

A Model 51 does not have the display module or keypad, U9, or U11.

Optional plug-in boards have a communication protocol that is unique to each type. This is explained in the address decoding paragraphs, and in the paragraphs unique to a plug-in board (5.7, 5.8, or 5.9). J7 through J11 may contain expansion RAM boards, optional digital I/O boards, or an optional IEEE-488 communications board.

RS-232 is controlled directly by the microprocessor U1. The IC U6 is just a level translator, changing 0 and 5 volt logic levels to + and − 10 volt levels suitable for RS-232.

5.2 MOTHERBOARD

5.2.1 Overview

The MPU

The MPU (MicroProcessor Unit) on the motherboard is the "brain" that ties the other circuit boards in the system together. Under the control of software stored in ROM, it reads the keyboard, sets up measurement modules and multiplexers, sets up the I/O board(s), takes readings from measurement module/s, digital I/O boards, or the motherboard (time, text, or math formula outputs), and sends data to the display module. It also controls data routing (storage of readings in memory), and communications with an external computer via an RS-232 chip or the optional GPIB interface card.

Major ICs

Refer to sheet 1 of the motherboard schematic, drawing number 0103-00-1808. Major IC's on the motherboard are the 63B03R microprocessor (U1), ST5152 gate array (U27), 146818 clock chip (U3), 27C512 64Kbyte ROM (U5), and the two SRM2064 8Kbyte RAMs (U4 and U7). The J7 through J11 sockets for optional plug-in boards are physically at the rear of the motherboard, to be near the rear panel 5 through 9 slots.

U1, the 63B03 MPU, operates in Mode 2, the expanded multiplexed mode: A0-A7 and D0-D7 share (time multiplex) the AD0-AD7 lines. The least significant 8 bits of addressing (A0-A7) are on these lines the first part of a cycle; the 8 bits of data (D0-D7) are on these lines during the second part of a cycle.

The MPU has 128 bytes of internal RAM. The 63B03 also has onboard port-address decoding. The two ports use some of the 32 internal registers. When a software command does a STORE to a port address, it sets some or all of the port lines to a high/low pattern. The value of the data that is output determines whether the line goes high or low.

Address Decoding

Refer to foldout figure 5-10 (at end of paragraph 5.2.8). Also see motherboard schematic, sheet 2, lower half, if desired. The address decoding circuitry may be thought of as the "traffic cop" that determines which device (aside from the MPU) will be allowed to put its data on the bus or receive from the bus at a given time. All devices that interface with the microprocessor are assigned a unique address. A device address may be thought of as its "telephone number". The MPU can communicate with only one device at a time. The combination of 1's and 0's on the 16 address lines makes up the address at any one time. There are up to 65,536 possible addresses. Devices that contain more then one internal location, such as memories, are assigned a block of addresses. When the microprocessor is communicating with another IC, it outputs one 16 bit address onto the address bus.

The job of the address decoder is to determine which device is being addressed by the combination on the address lines, and enable that device with a one-line signal. Some devices, such as RAM or ROM memories, have more than one address within the device. So, besides the device-select line from the address decoder, more address lines must go to the device. An additional address decoder within the device uses these address lines to determine and enable the location the MPU wants to send to, or receive from.

The address decoding is important because many failures that show up as a power on-off problem, are actually caused by bad devices on the MPU bus, bad address decoding circuitry, or associated components. Address decoding must be understood in order to isolate the problem.

5.2.2 Logic And Logic Levels Used

The 63B03 8-bit microprocessor is CMOS. The MPU senses and transmits logic levels basically meeting TTL thresholds (inputs are <0.8 or >2.0 volts; outputs are <0.55 volts or >2.4 volts). All MPU outputs will drive the equivalent of one regular TTL input (sink 1.6 mA). When high, each MPU output can source 200 uA to 2.4 volts.

The SSI and MSI logic chips used are either 4000 series CMOS, or 74HC series CMOS. Aside from the capacitive loading of each input, chip input impedances are virtually infinite. 4000 series output logic levels are within 10% of ground (<0.5 volts = low) or 10% of the positive supply (>4.8 volts = high). 4000 series inputs sense a low when the input is less than ⅓ of the positive rail (1.5V volts), and sense a high when the input is greater than ⅔ of the positive rail (3.5 volts).

5.2.3 The Motherboard Power Supplies

5.2.3.1 The Power Supplies Overviewed

There are three regulated 5 volt positive supplies for the circuitry on the motherboard. See sheet one of the motherboard schematic. They are V+, V++, and V+++. The unregulated power that is the source for the V+ and the V++ supplies is called B+. B+ may be supplied by either an external power source (typically a wall transformer), or, an optional internal battery pack.

RS-232 power is generated by the level-translating chip, U6, shown in sheet 1, zones A5 and A6. U6, a MAX232EPE, takes in +5.3 volt V+ on pin 16. It puts out +10 volts on pin 2, and −10 volts on pin 6, besides using + and − 10 volts for its own RS-232 drivers.

Measurement modules generate their own plus and minus voltages from an inverter module on the measurement modules. This inverter module requires V+6 (6.0 volts) from the motherboard. (Sheet 3, pin 10 on J12-J15.)

V+++

See sheet 1. V+++ supplies on-board backup power for calibration data and user-acquired data stored in the CALRAM (U4), and the standard user RAM (U7). See zones C3 and C2. These MOS RAMs use virtually no power when not being written to or read from. V+++ is backed up by a 2/3A-size 3-volt lithium battery BT1, via CR7, a Schottky diode.

If dipswitch S1-7 on the back panel is closed (physically down), V+++ also backs up the time and date stored in U3, the clock chip. For long storage periods when loss of the time and date are acceptable, the 6818 clock chip should be switched off by S1-7. (BT1 never gets any recharging current.)

V+++ also goes to a device-select signal blocker, U10A, on sheet 2, zone B2. The V+++ supply does not go to expansion (plug-in) RAM boards.

Some form of power to the U4 and U7 RAMs is always on. Either the unit has a source of B+ and therefore these RAMs have 5 volt V++ power feeding into the V+++ line via CR5. Or, the unit is off and these RAMs have the 3 volt V+++ backup power from the lithium battery, BT1.

V++ Overview

V++ is always on anytime either external power is applied to the chassis, or an internal battery pack is installed (and not discharged). 5.0 volt V++ provides power for the power-on circuitry (sheet 2; U13, U14, and U15). So, anytime external power is applied (typically from a wall module), or an internal battery pack (50-10 alkaline or 50-11 rechargeable) is plugged in, the unit can be turned on by pressing the front panel Power button.

When available, V++ also powers the clock chip U3, and any expansion RAM (plug-in) boards. V++ is supplied by linear regulator U12 on sheet 2 (zone D5).

V+ Overview

V+ is approximately 5.3 volts. It is on (+5.3 volts) when the chassis (display) is "on", and zero volts when the unit is "off". V+ supplies the higher currents for the microprocessor, address decoding, ROM, etc. See sheet 2, zones D4-D2. I.C. U16, power FET Q2, toroid L1, and associated passive components are a "buck type" switching regulator circuit which supplies a regulated 6.0 volt V+6 output. V+6 is dropped 0.7 volts by a diode to get the 5.3 volt V+ output.

V+ powers any digital I/O plug-in boards.

V+ may also power an IEEE-488 plug-in board, if the source of B+ is external power. (Paragraph 5.2.3.3, IEEE Power Control.)

The V+6 (6.0 volt) output of the switching supply indirectly powers the analog measurement modules, via the isolated power inverters on the measurement modules. See figure 5-2.

5.2.3.2 Power Down Feature Vs. Power Save Feature

See figure 5-2. Power down turns off V+ to the chassis (saves the most power). Power save turns off only measurement module channels — and only when they are not being used.

"PWR DOWN" is a choice for what to do with the "dead time" between scans of the user program's channel lists *while* the program is running. (Remote command MON, or the local main menu MONITOR MODE.) V+ power on-off controls are explained under paragraph 5.2.4.

"PWR SAVE" is a selection that can be made in local mode, by using the UNIT STATUS menu. The equivalent operation is accomplished remotely by using the STAT command. Measurement module power is discussed in paragraph 5.3.2.1.

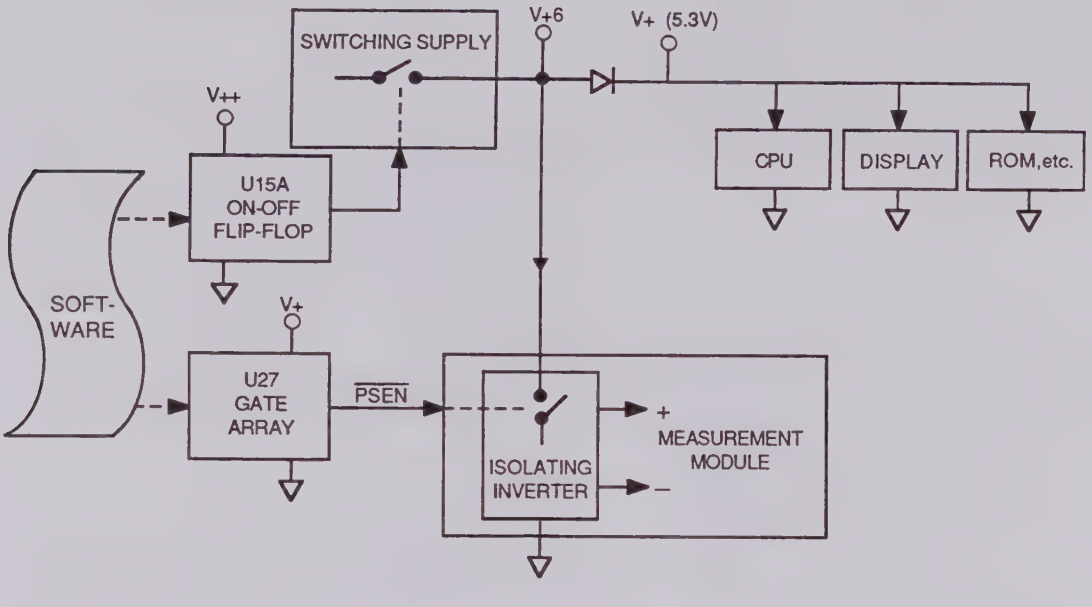


Figure 5-2. Power Down Vs. Power Save

5.2.3.3 Battery Pack Pin 4 Signals: 50-11 Vs. 50-10

The 50-11 lead acid rechargeable battery board has a fuse, identification capacitor, recharging circuit, and two comparators. The line from the battery board (J1-4) to the motherboard (J6-4) serves two purposes. It carries battery board identification information to the microprocessor during a power up subroutine. At all other times it tells an IEEE-488 board (if any) plugged into the motherboard, with a low-true $\overline{\text{INTPWR}}$ (INTernal PoWeR) signal, to not turn on when only battery pack power is available. Why and how this is done is covered in paragraph 5.2.3.4, IEEE-488 Power Control.

How the 50-11 battery recharging and comparator circuitry works is explained in paragraph 5.11. How the IEEE (GPIB) board works is explained in paragraph 5.9.

How Software Identifies Battery Type

A battery pack (50-10 alkaline, or 50-11 rechargeable) is approximately 2.6" × 4.1" × 2.3". During the power up routine, pin 4 on J6 is used for determining the battery pack type (alkaline or lead acid rechargeable). On the battery board, pin 4 goes to a capacitor, C7: 0.47 μF for an alkaline board, 0.1 for a rechargeable board. Pin 4 on J6 also goes to input/output port pin 19 on the motherboard microprocessor U1. The microprocessor momentarily toggles this line low (U1-19 in output mode). Then, it observes the time (U1-19 in input mode) for the capacitor to charge to a logic high. See figure 5-3, which shows the pertinent components for this operation connected by solid lines.

The time the microprocessor holds the line low is about 16 milliseconds. This ensures that the capacitor voltage is low. Then, the microprocessor makes pin 19 a high impedance input port. R5 begins charging the capacitor high. The time the capacitor takes to charge to a high logic level tells which kind of board it is on. An alkaline board will take 4 to 5 interrupt times; a rechargeable board will take 1 to 2 interrupt times. (For interrupt times, see paragraph 5.2.8.5.2.). This sequence happens twice during a power on routine: about 1160, and 1330 mSec into the routine.

If the port line charges high before even 1 interrupt time has elapsed, the software knows that there is no battery pack installed. If the port line never charges high, that is a sign to the microprocessor that there is a rechargeable board installed (and no external power is connected to the unit).

Except for this battery type test, pin 19 on the microprocessor is normally an input.

5.2.3.4 IEEE-488 Power Control

B+, the source for the V+ regulator circuit, comes from either external power, or an internal battery pack (50-10 or 50-11). An IEEE-488 board takes about 500 mA of V+.

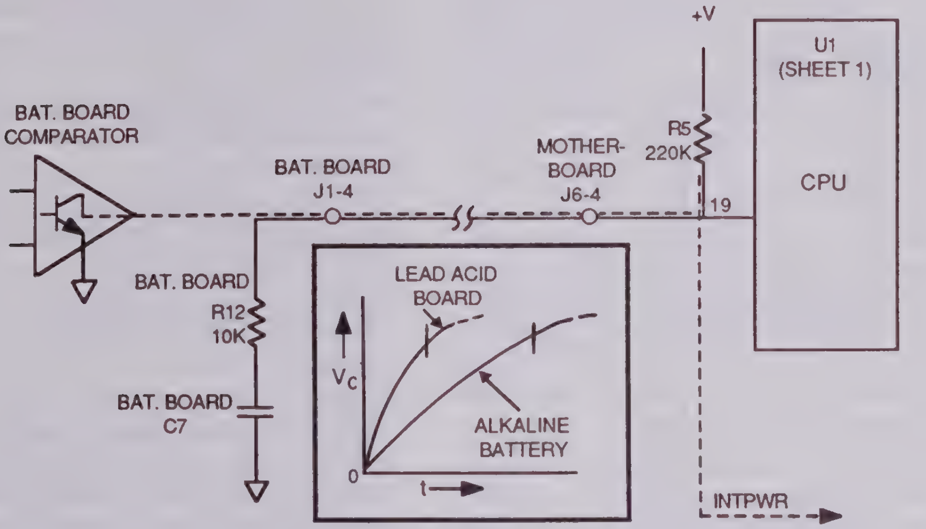


Figure 5-3. Battery Board Identification/IEEE Power Control

This is considered to be too much of a load for an internal battery pack to run in conjunction with everything else in the chassis. A signal from the 50-11 rechargeable internal battery pack, $\overline{\text{INTPWR}}$ at J6-4, controls whether or not the IEEE board will accept V+ power. See figure 5-3, which shows the pertinent components for this operation connected by dashed lines.

$\overline{\text{INTPWR}}$ is normally pulled up by R5 on motherboard schematic sheet 1 (zone C8). However, if external power is not connected, the 50-11 rechargeable pack board senses this and one of its open-collector-output comparators puts a low on J6-4. The IEEE board senses that $\overline{\text{INTPWR}}$ is low (pin 16A on the IEEE board) and thus refuses to take V+ power.

The 50-10 alkaline battery pack board has only an identification capacitor. This means that it can't sense when there is no external power and send the low-active $\overline{\text{INTPWR}}$ signal to turn off an IEEE board.

Note that an external battery could be the source of power. In this case, there is no circuitry that can tell the IEEE board to not take V+ power. So that the IEEE board doesn't have to be removed, there is a rear panel switch labelled IEEE On that will interrupt V+ power to the IEEE board when put in the down position. The mother board schematic shows the switch as IEEE ON, on shee 3, zone C6.

5.2.3.5 Raw B+ for V++ and V+ Regulators

See sheet 2, zones D8-D5. Either external powe (through J5) or an internal battery pack (through J6) ca supply unregulated B+ to the regulators. Depending o the line voltage, B+ is approximately +20 volts whe running off the supplied wall transformer. B+ from a internal battery pack is nominally +12 volts. The highes B+ allowable is 24 volts. Above this voltage, CR16 wi conduct heavily and blow the fuse: F1 on the mother board/rear panel if external power; or, F1 on the batter board.

The Paths of B+

External power comes in, dc or ac, at J5 and goe through F1 at the rear of the chassis. It gets rectified b CR11, a bridge diode module, and then goes to three c four places. The external source supplies main B+ power, via CR12, to the input of the linear regulator U12- (zone D6), and to the switching regulator (zone D4). I supplies B++, via CR15, to U12-8. It also supplies into J6-3, the current for recharging a rechargeable battery pack (if installed).

Internal battery pack power (+12V) comes onto the motherboard via J6-2, and then goes to three places. It supplies main B+ power, via CR13, to U12-3 (zone D6) and to the switching regulator (zone D4). Also, it supplies B++, via CR14, to U12-8.

Paragraph 5.11 covers how the rechargeable battery pack board works.

5.2.3.6 In Case Of Power Loss

B++ is a fast-discharging version of B+ used to tell U12 and, indirectly, the power off-request flip flop, U15B, that the source of B+ (external and internal) has been unplugged. If this happens, the MPU stores the current operating environment into battery-backed-up RAM before turning off V+. This all happens before C21, the 2200 μF B+ capacitor, can discharge.

Depending on the load, it takes C21 one-half to one second to discharge. B++ is loaded down by R48 and R49. Since B++ is held up only by C19, 0.1 μF, and isolated from C21 by CR12 and CR13, it discharges much faster. The −IN pin on the LT1020 chip is the negative input of a comparator in the IC. The positive input of that comparator, +IN, receives a 2.5VDC reference from REF. When the comparator switches, from −IN going below 2.5V, COMPN will go high. COMPN's signal, called B+<10.0V, goes to U15B-8, forcing it to generate a low-active nonmaskable interrupt. This is summarized in figure 5-4.

The microprocessor is able to complete its interrupt routine before the B+ voltage drops too low.

How the unit powers itself down will be further explained in paragraph 5.2.4.

If an external source is unplugged, the internal battery pack, if installed, will take over and keep B+ and B++ up. J6-2 is the output from the pack, feeding the anode of CR13 (for B+) and the anode of CR14 (for B++).

When an internal battery pack is not installed, a jumper must be installed from J6-1 to J6-2 to pull down any leakage current coming back through CR13. This leakage current otherwise would go through CR14 and keep up the B++ line regardless of whether or not external power is applied.

5.2.3.7 Too-low-to-operate Vs. "LOW BAT"

The lowest B++ (or B+) that the unit will operate on is 10.0 volts. This is set by the combination of R48 (1MΩ) and R49 (332KΩ) going into a 2.5 volt comparator (U12-8). The other input of the comparator (pin 7) is a 2.5 volt reference from U12-4. How the comparator works with other circuitry is explained under paragraphs 5.2.3.6, In Case Of Power Loss, and 5.2.4, Power On-Off Control.

Another comparator, in U16 (zone D4) detects when the B+ is down to +10.58 volts. R60 (1MΩ) and R59 (140KΩ) divide down B+. The LBR (Low BatteRy) input of U16 (pin 1) senses when the voltage there is below 1.3 volts. When this occurs, the low battery detected (LBD — pin 8) output of the chip goes low. This goes to the microprocessor, U1 pin 20, (sheet 1, zone C8). The software displays the message "BAT LOW" as a consequence.

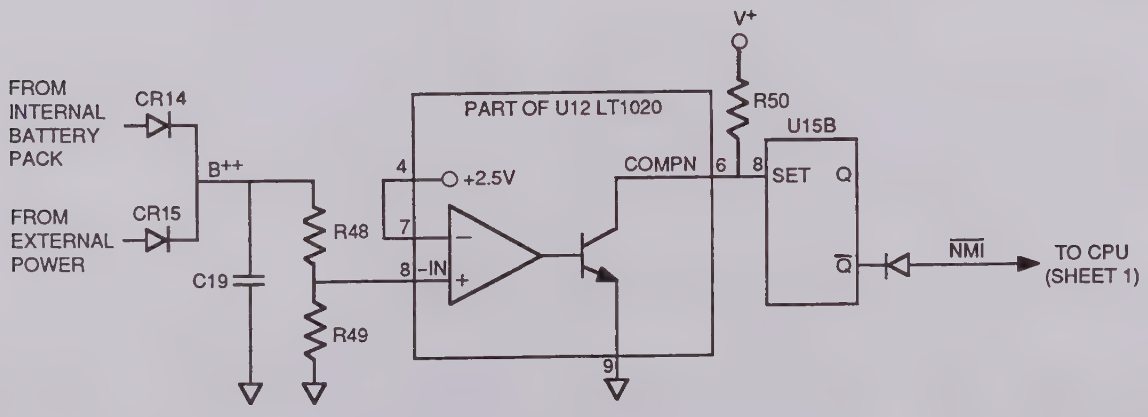


Figure 5-4. B+ Dropout/brownout Turn Off-Request Circuitry

The level on U1-20 is polled (sensed) approximately once for each time the microprocessor runs its timed interrupt routine (paragraph 5.2.8.5.2), or, between measurements, if they are being taken.

5.2.3.8 U12 Regulation of V++ Voltage

See sheet 2, zone D5. The heart of regulator U12 is an internal PNP pass transistor. Figure 5.5 is a simplified circuit of the regulator's voltage regulation circuitry, along with external voltage setting resistors R51 and R52.

The zener provides a +2.5V reference to the − input of the amplifier. The + input of the amplifier senses one-half of the regulator's output voltage (normally +2.5V). The pass transistor's base voltage is a few hundred millivolts below the emitter voltage, to keep the transistor partly on.

If the output voltage at pin 2 goes below 5.0 volts, it causes the + input of the amplifier to drop below +2.5 volts. The amplifier output will go down a few millivolts which will sink more current from the base of the transistor. This causes the transistor to turn on more, and bring the output voltage back up to +5.0 volts.

Likewise, if the output voltage tries to rise above 5.0 volts, this causes the + input of the amplifier to go above +2.5 volts. The amplifier output will go up a few millivolts which will sink less current from the base of the transistor. This causes the transistor to turn off somewhat, and bring the output voltage back down to +5.0 volts.

When the pin 2 output voltage is exactly 5 volts, the — input of the amplifier will equal the + input of the amplifier, and the amplifier will not increase for decrease the transistor's bias. The output voltage will remain stable.

Pin 5 on U12 is not used. Pins 8, 6, and 13 are discussed under Power on-off control.

5.2.3.9 Generation of V+ Voltage

U16 senses the output voltage V+6, and controls power FET Q2 so that V+ is indirectly regulated at +5.3 volts. U16 regulates V+6 (output of L1) to 6.0 volts. With always at least a light load on V+, there is a 0.7 volt drop across CR20, causing V+ to be +5.3 volts. (The 6.0 volt V+6 supply is required as the input to measurement module power inverters.)

Unlike U12, U16 is a switching regulator. Q2, switching diode CR19, L1, and C35 are in what is called a BUCK configuration.

See figure 5-6, a simplified drawing of the switcher.

One of a coil's electrical properties is that it resists any *change* in the amount of current flowing through it. If no current is flowing, the coil tries to keep things this way. Also, if for example, one-half ampere is flowing, the coil tries to keep things that way. It generates a voltage across its terminals that opposes the external voltage. The result is that even though the external voltage may change suddenly, the coil current always changes slower. This is the basis of the switcher.

Since Q2 is closed only at some duty cycle, the coil pumps current into the storage capacitor C at some average rate, modified by smaller spurts of current. The dc voltage on C is less than it would be than if B+ was always applied to the input of the coil. Since C is large,

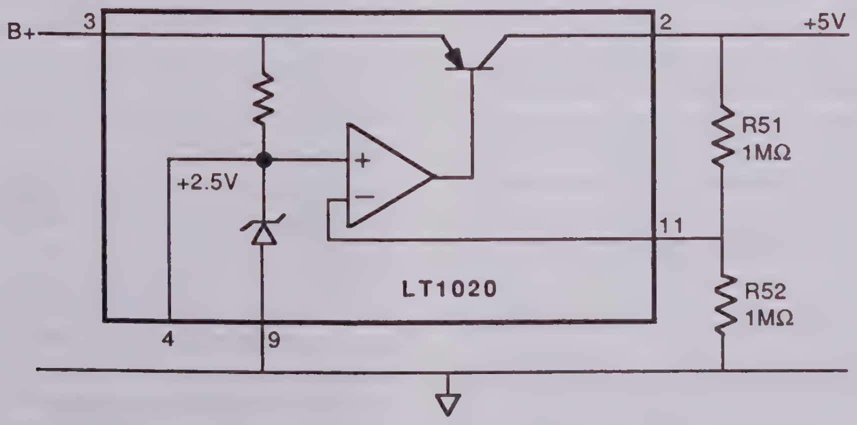


Figure 5-5. LT1020 Regulation Circuitry

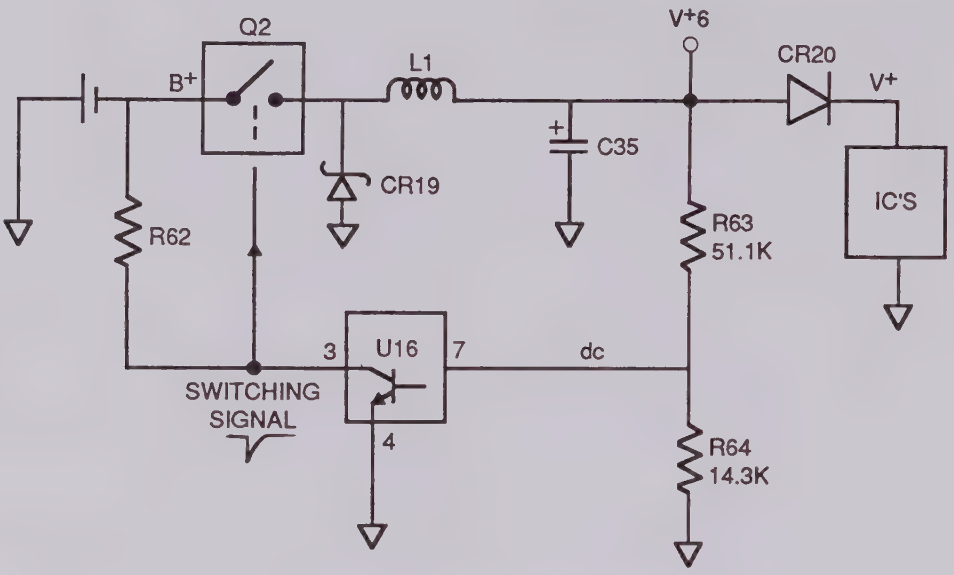


Figure 5-6. Simplified Switcher

it does not change its voltage significantly during an input current spurt (ripple is fairly small).

The L1 coil basically integrates or "remembers" what percentage of time that B + is applied to it, and translates this into a lesser dc voltage on C35.

The U16 switching regulator senses the output voltage (V + 6), and adjusts its pin 3 low-on pulses in width and frequency to maintain the correct output voltage. U16 can turn on Q2 assuming that U16-6 is being sourced current from U15A.

Power FET Q2, an RFP6P08, functions as the switch. It is either full on, or full off. The primary job of U16 is to regulate by controlling what percentage of time that Q2 is on, applying B + to the coil. U16 regulates V + 6 (6.0 volts) so that it gets 1.3 volts on the voltage feedback pin, pin 7. R63 and R64 provide the voltage division. U16-3 puts out approximately 0.1mS-wide low pulses. These turn on Q2 at about a 2.0 millisecond repetition rate. (This is a very rough number — it depends considerably on how much load current is being drawn.) U16-3 is an open collector output, so a pullup resistor, R62, is required.

When Q2 turns off, the coil attempts to keep drawing exactly the same amount of current it ramped up to during the B + pulse. It uses its stored energy to make its input go negative, in an attempt to pull current into its input. CR19, a fast recovery diode, provides the current while Q2 is off. The current is pulled out of ground (a very low impedance point), up through CR19, and into L1. CR19 clamps the flyback voltage at the input of the coil to within one diode drop of ground.

The output dc voltage on C35 is a function of how wide the applied pulses on the input of the coil are (allowing more time for the current to ramp up), the input voltage, the time from pulse to pulse, and the current drawn by the load.

Figure 5-7 shows the voltage waveforms on Q2 and L1 once the output capacitor C35 is charged up, and the coil is passing only "maintenance" current.

When V + is first turned on (by U15A-1 going high), C35 has be charged up. So the repetition rate of the Q2 turn-ons is very often: approximately every 0.8 milliseconds.

5.2.4 Power On-Off Control

5.2.4.1 Overview

This description assumes the reader has first read all of paragraph 5.2.3.

The Models 51 and 52 incorporate software control over the power supply (V +) that supplies the most current. This allows the unit to save battery power when the unit is not taking measurements, communicating, etc. To the Model 52 user, the most obvious indication that the unit is "on" or "off" is the front panel display. This is because the display is one of the loads for the V + supply. The front panel Power button is just one of several ways that the V + power can be affected.

The following summaries are followed by amplified descriptions in paragraphs 5.2.4.2 and 5.2.4.3.

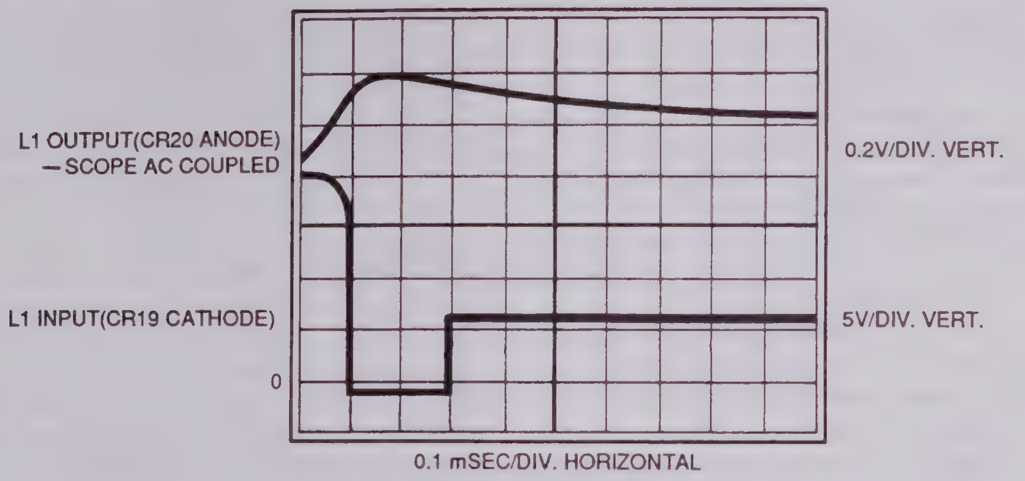


Figure 5-7. Switcher Voltage Waveforms

U15A: The Real On-off Switch

Refer to sheet 2 of the motherboard schematic, zone C4. U15A is the main power (V+) on-off control flip flop. When U15A is in the SET state (U15A-1 high), V+ is on. When U15A is in the CLeaR state (U15A-1 low), V+ is off.

U15B: The Turn Off-request-remembering Flip Flop

U15B, by being put into the SET state, "remembers" if a turn off sequence is to be done, even if the pulse that requested it is no longer available.

Items That Initiate a V+ Turn On

N1) An operator pushes the front panel Power button.
N2) A character comes in on the RS-232 RXD line (rear panel Auto Pwr switch must be up).
N3) The clock chip generates an $\overline{\text{ALARM}}$ signal.

Any one of the above turn-on initiators results in a positive going pulse at U15A-3 which makes the flip flop go to the set state, turning on U16. This makes V+ come up and stabilize in a short period of time. The microprocessor and associated circuitry must be held in the reset state during the interval in which V+ is stabilizing.

The power-up delay until $\overline{\text{RESET}}$ goes away is about 500 milliseconds, set by C29 and R66 on the input of U13A.

The low $\overline{\text{RESET}}$ signal while in reset also inhibits address decoding/device selection (lower part of sheet 2) for other devices on the MPU bus. This ensures that they won't put random addresses or data on the bus. To the extent that this applies to turn on's and turn off's, the clock chip can't generate an erroneous alarm, turning on the unit, and the address decoding won't erroneously decode a power off command.

Note

When the unit "does not turn on", the problem may also be that the turn off circuitry is malfunctioning.

Items That Initiate A V+ Turn Off

O1) An operator pushes the front panel Power button, while the unit is on. (U15B-11 gets clocked.)
O2) A Model 51 or 52 program enters the "dead time" (power down time) of a scan interval, and power down mode has been chosen. (There is no action with U15B.)
O3) Both the external power source and the internal battery pack are unplugged. An "early-dropout" version of the voltage on the main filter capacitor goes low, and is sensed in time by circuitry. If the B+ drops slowly, this also will initiate a turnoff sequence. (U15B is SET.)

Any one of the above turn-off initiators eventually results in firmware writing to the $\overline{\text{PWROFF}}$ address. This causes a high pulse at U15A-4 which makes the flip flop go to the clear state, shutting down U16.

5.2.4.2 Detailed Turn On Explanations

A Power Button Turn On

See sheet 1, zone A1. The front panel Power switch is a "soft switch". That is, it's function is defined by whether the unit is currently on or off. If the unit is off, pressing power will turn it on, and vice-versa. Each time the Power button is pressed, the $\overline{\text{POWERON}}$ line is grounded. The $\overline{\text{POWERON}}$ signal from the push button is debounced by R56 and C27.

For a Model 52, the Power button connects J3-2 with J3-1. The $\overline{\text{POWERON}}$ signal bypasses the decoding for the other keypad buttons, and goes directly to U13B-5. See sheet 2, zone C7. In a similar manner, a Model 51 $\overline{\text{POWERON}}$ signal is generated by its Power button being pressed. These cause a high at U13B-4. The high-going edge on U13B-4 makes a low-going edge on U14D-13. This normally makes a high-going edge on U14B-4. This ↑ edge clocks U15A into the set state. This sources current through R61, which starts V+ powering up.

$\overline{\text{RESET}}$ must be held low for approximately 500 milliseconds to give V+ and the MPU clock time to stabilize. C29 and R66 provide the delay for this. When U15A-2 goes low, the current to pull U13A-2 low must go through R66.

The turn on signal from U14B-4 can be inhibited if the rear panel PWR EN switch, S1-2, is closed (physically down). The high on U14B-6 "blinds" U14B to any turn on signal at U14B-5. (This is useful during shipping to prevent turn on of the unit, and rundown of the 50-10 or 50-11 battery pack. The normal condition is S1-2 open, with U14B-6 low.) Turn on may also be prevented if B+ is low enough that U12 has dropped out of regulation (causing the V+ +<5.2 line from U12-13 to be high).

If the turn-off-request flip flop, U15B, is asserting $\overline{\text{NMI}}$, the clock from U13B-4 will also cause U15B to go out of that state.

Incoming RS-232 Character Turn-on

See sheet 1, zone A6. The RS-232 receive-data line goes two places. It goes to the level translator chip, U6. It also goes through R11 to C25. See sheet 2, zone C8. R11 (sheet 1) and R53 form a two-thirds divider for ac. An RS-232 character coming in with a peak-peak amplitude of 6 volts would develop about 4-volt edges on the input of U13D, pin 12.

Since the normal state of a RS-232 link is to be MARKing time, the line is sitting at its most negative prior to the start of the character. The dc level at U13D-12 approaches zero during intervals of no RS-232 activity. This means that the incoming edges on the right side of C25 when the character starts will be completely positive with respect to ground. A signal greater than about 3.3 volts in peak-peak amplitude at U13-12 will cause U13D-11 to pulse low (assuming the rear panel Auto Pwr switch, S1-3, is open). This causes high pulses at U13C-10, and low pulses at U14D-13. This normally makes a high-going edge on U14B-4. This ↑ edge clocks U15A into the set state. This starts V+ powering up.

The turn on signal from U14B-4 can be inhibited if the rear panel PWR EN switch, S1-2, is closed. The high on U14B-6 "blinds" U14B to any turn on signal at U14B-5. (The normal condition is S1-2 open, with U14B-6 low.) Turn on may also be prevented if B+ is low enough that U12 has dropped out of regulation (causing the V+ +<5.2 line from U12-13 to be high).

$\overline{\text{ALARM}}$ Signal Turn-on

See sheet 1, zone C5. The clock chip, U3, generates an $\overline{\text{ALARM}}$ signal when it wants the MPU, U1, to read or update the current time stored in a U3 register. Two things may be the occasion: It may be time for another scan within a program, or the time chip may require updating by the MPU (real time clock going over midnight) during a program. The $\overline{\text{ALARM}}$ line goes two places. It goes to the V+ turn on circuitry on sheet 2, zone C7, and to the MPU (presenting an IRQ to the MPU once V+ stabilizes and the MPU comes out of reset). On sheet 2, $\overline{\text{ALARM}}$ goes to C33. The ↓ edge at U13C-9 becomes a ↓ edge at U14D-13. This normally makes a high-going edge on U14B-4. This ↑ edge clocks U15A into the set state. This starts V+ powering up.

Once the MPU comes out of reset, software identifies the IRQ as a clock interrupt, and services it.

The turn on signal from U14B-4 can be inhibited if the rear panel PWR EN switch, S1-2, is closed. The high on U14B-6 "blinds" U14B to any turn on signal at U14B-5. (The normal condition is S1-2 open, with U14B-6 low.) Turn on may also be prevented if B+ is low enough that U12 has dropped out of regulation (causing the V+ +<5.2 line from U12-13 to be high).

5.2.4.3 Detailed Turn Off Explanations

The last item in any turn off sequence is that software writes to address $07E0_H$, which causes a low pulse at U24-7 on sheet 2, zone B5. This causes a high pulse at U14C-10. This puts U15A in the clear state. The resulting low on U15A-1 turns off the V+ supply. Also, the high on U15A-2 goes through CR21 (bypassing R66) and rapidly causes a low on U13A-3. This puts the MPU in the reset state.

Address decoding is explained under paragraph 5.2.8.

The second to last item in a turn off sequence is that the software stores the operating environment into battery backed up RAM.

One item that starts the software part of a turn off sequence is an active-low $\overline{\text{NMI}}$ being asserted by flip flop U15B to the MPU U1. The function of U15B is to "remember" if the Power button, or a dropout, "requested" a turn off. If one of these two turn off initiators (O1 or O3) happens, U15B goes to the SET state and remains there until the V+ supply is turned off. What tells U15B that the unit has been turned off is that $\overline{\text{RESET}}$ goes low and U14A-1 goes high. This toggles U15B back to the CLeaR state ($\overline{\text{NMI}}$ not asserted anymore).

Also, the high at U14C-9 keeps U14C-10 low, inhibiting any off-writing to U15A-4 by random address lines.

While in reset, the unit still retains control over the state of U15B — the high at U15B-10 prevents any additional clocks at pin 11 from toggling U15B into an unknown state. Once the unit comes out of reset after the next turn on, U15B will again be free to toggle.

A Power Button Turn Off

The $\overline{\text{POWERON}}$ signal is also a signal that can turn off the V+ supply. For a Model 52, the Power button connects J3-2 with J3-1. The $\overline{\text{POWERON}}$ signal bypasses the decoding for the other keypad buttons, and goes directly to U13B-5. See sheet 2, zone C7. In a similar manner, a Model 51 $\overline{\text{POWERON}}$ signal is generated by its Power button being pressed. Either way causes a high-going edge at U13B-4. The high-going edge at U13B-4 goes to the clock input of the flip flop U15B-11 (pin 11). U15B is the $\overline{\text{NMI}}$-remembering flip flop. Since the clear input of U15B is normally low, and the $\overline{\text{Q}}$ output (and D input) of U15B is normally high, the clock edge at pin 11 will move the high at the D input to the Q output. This means, conversely, that $\overline{\text{Q}}$ will go low. This causes a nonmaskable interrupt signal to the microprocessor. As a result of servicing the interrupt, the MPU writes to the power off address, U24-7.

$\overline{\text{NMI}}$ must be "remembered" and asserted until it is serviced — that is, until software can get around to turning the unit off. U15B fulfills this function. When the software flips U15A into the clear state (V+ turning off), $\overline{\text{RESET}}$ of the microprocessor is also pulled low by U13A-3 (zone C3). U14A inverts this signal, and feeds it to the high-clear input of U15B, pin 10. This makes the $\overline{\text{Q}}$ output of U15B, pin 12 go back high, and the NMI request signal go away.

A Program Scan Interval Power Down

The unit can be set to turn off during the unused part of a scan interval of a program, in order to conserve battery power. Software writes to the power off address, which pulses U24-7 low, etc. (An $\overline{\text{ALARM}}$ from the clock chip will at some later time initiate a turn on sequence.)

A B+ Dropout/brownout-caused Turnoff

If both the external power source and the internal battery pack are unplugged, B++, a quick-discharging version of the voltage on the main B+ filter capacitor, goes low, and is sensed in time by circuitry. See also figure 5-3 in paragraph 5.2.3.6. B++ being too low causes U12-6 (sheet 2, zone D6) to be high. If the B+ drops slowly, this also will cause U12-6 to be high. U12-6 goes to the NMI flip flop, U15B-8. A high on the SET input of U15B will cause it to be set (pin 12 goes low) regardless of the state of the D or CLK inputs. So, B++ being too low causes a nonmaskable interrupt, as in the case of a Power button turn off. The $\overline{\text{NMI}}$ signal causes the interrupt routine to run, which writes to the $\overline{\text{PWROFF}}$ address, U24-7, etc.

5.2.5 MPU Bus Overhead Lines

5.2.5.1 MPU Clock And E Generation

The 63B03 MPU runs at 1.2288 Mhz. To get this, it divides the Y1 crystal frequency by four. The undivided crystal frequency of 4.9152 MHz, called REFCLK, goes to U27, the communications chip for the measurement modules.

The 1.2288 Mhz signal, "E", is used to latch data. One complete cycle of E, from falling edge to falling edge, is called "a cycle". A cycle is 814 nanoseconds. See figure 5-8.

5.2.5.2 R/$\overline{\text{W}}$

Pin 38 of the MPU controls whether other devices are being written to (R/$\overline{\text{W}}$ low), or read from (R/$\overline{\text{W}}$ high). R/$\overline{\text{W}}$ is asserted high or low near the start of a cycle, and continues its state throughout the cycle.

5.2.5.3 A0-A7 Address Latching

The data is put on the AD0-AD7 lines at approximately the midpoint of a cycle.

See figure 5-9. During approximately the first half of a cycle, the AD0-AD7 lines carry the A0-A7 information, which must be latched so it is available during the rest of the cycle.

Pin 39, AS (address strobe), goes high when the MPU first puts the address on the bus. The MPU stabilizes the address bits within 260 nanoseconds of the start of the cycle. AS high enables address latch U2 to buffer the A0-A7 address information to its outputs. The U2 outputs are latched and keep the state of the A0-A7 bits when the trailing (falling) edge of AS occurs. The MPU stabilizes the address information at the input of U2 at least 33 nanoseconds before it takes AS low.

After the trailing edge of AS, the AD0-AD7 lines from the MPU need no longer carry address information.

An address and the AS signal are sent out even if the MPU's internal addresses are being used.

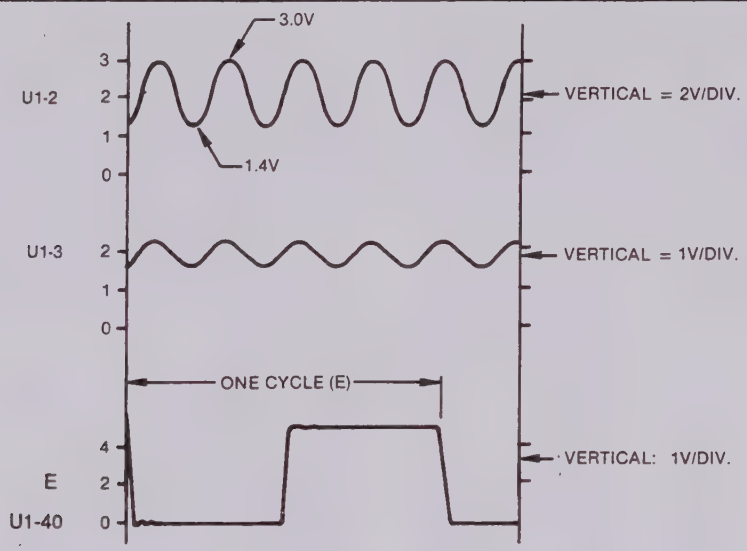


Figure 5-8. Y1 Crystal and E Waveforms

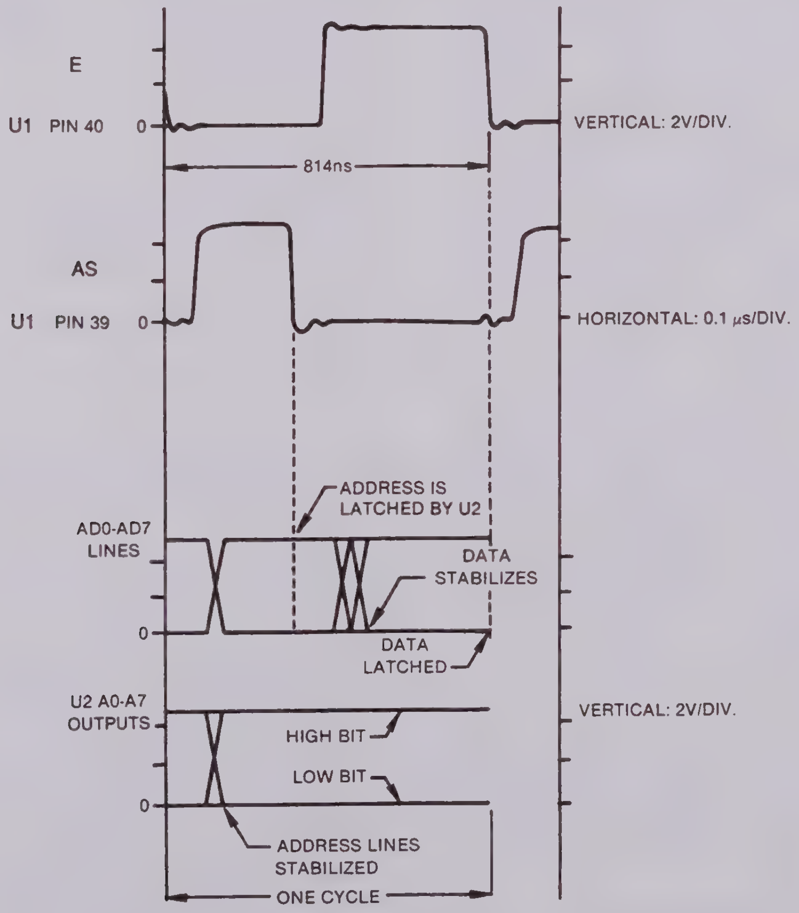


Figure 5-9. AD0-AD7 Address/Data Multiplexing

5.2.5.4 Data Latching

The signal from MPU pin 40, E, is used directly or indirectly by receiving devices on the bus to latch data. See figure 5-9 again. Data is latched on the falling edge of E.

During a write operation, the MPU stabilizes the outgoing data on the data lines at least 163 nanoseconds before it takes the E clock low.

During a read operation, the MPU must have incoming data stabilized on the data lines at least 50 nanoseconds before the falling edge of E.

5.2.6 Other MPU Lines

5.2.6.1 STBY Line

This low-active pin is not used in the Models 51 or 52, so it is tied high.

5.2.6.2 $\overline{\text{RESET}}$ Line

$\overline{\text{RESET}}$ is driven by U13A-3 on sheet 2. U13A-3 is a 500 millisecond-delayed signal from the main power control flip-flop, U15B. The delay is set by C29 and R66 on the input of U13-A. The delay is to allow the power supply to come up, and for the mode programming information at MPU pins 8, 9, and 10 to stabilize before the MPU attempts to come out of reset. (Power On-Off control is explained under paragraph 5.2.4.)

Reset States of AD0-AD7, E Clock and AS

When $\overline{\text{RESET}}$ is held low for at least 3 clock cycles, the high-order address lines become high impedance (tristated). The AD0-AD7 lines are high during AS time; tristated during data time. $\overline{\text{RESET}}$ also inhibits the address decoding circuitry on sheet 2, and any plug-in boards (J7-J11 on sheet 3), insuring that no device will attempt to put data on the bus. E clock and AS are still active; the R/$\overline{\text{W}}$ line is high.

When the $\overline{\text{RESET}}$ line is taken high, three things happen in sequence before the program starts executing:

1) Mode selection: The MPU latches in the state of pins 8, 9, and 10 (P20, P21, and P22) the instant of $\overline{\text{RESET}}$ going high. During Reset, these lines are high impedance inputs. In this unit, the pattern is 0, 1, 0, respectively, causing the MPU chip to go to mode 2, the expanded multiplexed mode. The 0, 1, 0 pattern is forced by R3, R1, and R4. The multiplexed mode makes pins 30-37 serve as both address and data lines. Also, pins 13-20, instead of being the low order address lines, will serve as the P10 through P17 port lines. (Later, when the program stored in ROM U5 is running, P20-P24 will be programmed as inputs and outputs.)

2) Program start address: The MPU automatically does READs at FFFE_H and FFFF_H, and loads the contents of these two 8-bit locations into the 16-bit program counter. The start address is F438_H (software versions 4.23 and on).

3) The MPU sets the interrupt mask. (U3, the clock chip, uses IRQ_1, so the startup routine clears the interrupt mask.)

5.2.6.3 P20-P24 Lines

Each individual bit on this 5-bit port can be either an input or an output assuming the MPU is not in reset. The direction is controlled by software setting a bit pattern in this port's data direction register.

P20: See paragraph 5.2.7. P21: Paragraph 5.2.8.5.2 explains the software "source" of this signal, and how it is used. P22-P24: See the following paragraph.

5.2.6.4 RS-232

RS-232 functions are controlled by MPU ports P11, P10, P24, P23, and P22.

P11 (pin 14) is an output from the MPU, and controls the power to the MAX232 chip (zone B5). When RECEIVE or XMIT is selected in the Model 52 RS-232-C menu, (or a remote command equivalent), P11 will be low. This line, $\overline{\text{RS-232EN}}$, goes to switching FET Q3, turning it on. This applies 5.3 volt power to U6-16. When Q3 is off, U6-16 may normally be up to approximately 2 volts. The purpose of turning off U6 (happens when RS-232 is not selected by menu), is to save battery power.

When U6 is powered up, an internal oscillator supplies + and − 10 volts for the outgoing RS-232 signals (U6 pins 14 and 7). C6 and C7 are the charge-holding capacitors for the + and — charge coupling supplies in the MAX232. The + 10 volts at U6-2 also powers two pullup resistors, R9 and R10. U6 has four inverters: one for each direction of the serial data, and one for each direction of hardware handshaking. RS-232-C levels are − 3 to − 15 volts for a logic 1, and + 3 to + 15 volts for a logic 0. So, the + and − 10 volt outputs from the MAX232 level translators to the RS-232 bus provide about 7 volts of noise immunity.

P10 (MPU pin 13), called $\overline{\text{CTS}}$, is an input to the MPU, and is a handshaking line. When CTS/DTR is selected in the RS-232-C menu, this pin must be low for the Model 52 to transmit. The signal is inverted coming through the U6 level translator. This means that for the other unit to be asserting CTS, CTS will be more than + 3 volts at U6-8. When the other unit is not asserting CTS, the incoming signal at U6-8 should be less than − 3 volts. If this line is not connected to the other unit, the U6-9 default signal to the MPU is a + 5 volt high. In this case, CTS/DTR should not be selected in the RS-232-C menu, so that Model 52 transmission is not inhibited.

P24 (MPU pin 12), called TXD, is an output from the MPU, and is the outgoing serial data line. A logic 1 is +5 volts at U6-11, and about −10 volts at U6-14. A logic 0 is about 0 volts at U6-11, and about +10 volts at U6-14. The normal (idling) state at U6-11 is a logic 1 (+5 volts).

P23 (MPU pin 11), called RXD, is an input to the MPU, and is the incoming serial data line. An RS-232 logic 1 (a mark) is less than −3 volts at U6-13, causing +5 volts at U6-12. A logic 0 is greater than +3 volts at U6-13, causing about 0 volts at U6-12.

(The $\overline{\text{RXD}}$ signal on the RS-232 side of U6 also goes to the power on circuitry. Power on theory of operation is explained in paragraph 5.2.4.)

P22 (MPU pin 10), called RTS, is an output from the MPU, and is a handshaking line. The Model 51 or 52 asserts this line when it can receive data. This line will be deasserted when CTS/DTR is selected in the RS-232-C menu, and the unit's receive buffer is ¾ full. This causes the sending unit to stop sending data until the Model 51 or 52 "digests" some of the characters in its receive buffer, and reasserts the RTS signal.

Normally, the signal at U6-10 is low (0 volts), meaning that the Model 51 or 52 receive buffer is not overloaded. This low signal causes a RS-232 signal at U6-7 of about +10 volts. See also paragraph 5.2.8.5.2.

J1 and J2 are connectors on the motherboard for a ribbon cable that runs to the RS-232 connector on the back of the chassis. One connector is wired as DTE equipment and the other as DCE equipment.

Information on setting up RS-232 parameters, and external RS-232 theory of operation, is contained in the operator manual.

5.2.6.5 P10-P17 Lines

Each individual bit on this 8-bit port can be either an input or an output assuming the MPU is not in reset. The directions are controlled by software setting a bit pattern in this port's data direction register. P10 and P11 are used for RS-232, as explained in paragraph 5.2.6.4.

P12-P15: Switch Reading/LCD Viewing Angle

In a Model 52, P12, P13, and P14 (MPU pins 15, 16, and 17) are normally steady-state outputs from the MPU, and used to set the viewing angle of the LCD display. Eight combinations are possible for these three lines. Operation of U9 is explained under paragraph 5.6.

In a Model 51, P12, P13, and P14 are also normally steady-state outputs from the MPU, but used to drive the three front panel LEDs.

During a power up routine, the display or LEDs aren't being driven yet, so these three lines are available for something else.

During a power up routine in a Model 51 or 52, these three lines are inputs used to read three rear panel DIP switches. The MPU takes P15 (pin 18) low, which drives rear panel dip switches S1-4, S1-5, and S1-6. If a switch is closed (physically down), its right side on the schematic will be a logic low. If the switch is open (physically up), its right side will be pulled up by a 220K resistor to V+. See note 7 on the schematic. The switches are also read at each user-initiated calibration request.

P16 and P17

P16 (MPU pin 19) is named $\overline{\text{INTPWR}}$ (internal power). This pin on the MPU is part of a scheme for identifying whether a primary (alkaline), or rechargeable (lead acid), battery option is installed. The scheme is explained under paragraph 5.2.3.3. P17 (U1 pin 20) is used to sense a low battery condition. Its use is explained under paragraph 5.2.3.7.

5.2.6.6 $\overline{\text{NMI}}$ Line

$\overline{\text{NMI}}$ (nonmaskable interrupt) is driven by the power-off flip-flop, U15B-12, on sheet 2. When pulled low, a power down sequence is run. The "operating environment" is stored, and then the MPU writes to the power off address. The causes of an $\overline{\text{NMI}}$ are explained under paragraph 5.2.4, Power On-Off Control.

5.2.7 Addresses Above 32K: ROM

The sixteen address lines normally could access up to 65,536 bytes of memory. In the case of the Model 52, devices other than memory chips are "memory mapped" into part of this address space. To recover 64K of space for read only memory, a ROMBNK line (MPU pin 8) is used to switch two banks of 32K into the circuit one at a time.

The MPU, on a write cycle, does a ROM bank selection (a software OUT to the port line), if necessary, prior to attempting to read from the ROM. The data for the OUT statement determines the state (1 or 0) that the ROMBNK line becomes. Several program steps later, the ROM read actually occurs.

Software keeps track of which bank is currently being used. The 32K of ROM currently switched in occupies the upper 32K of the MPU address space. U5, the 64Kbyte ROM (location 1D1), enables one of its two 32K segments based on the state of the ROMBNK line. The U5-20 chip enable, called $\overline{\text{ROM}}$, comes from the address decoder output, U19F-12 (2A8). See figure 5-10.

5.2.8 Addresses Less Than 32K

5.2.8.1 Memory Map And Sheet 2 Address Decoding

The address space below 32K serves several functions. Table 5-1 gives an overview of the address space useage below 32K (0-$7FFF_H$).

Table 5-1. 0-32K Memory Map

0000_H-$001F_H$	MPU Internal Registers
0020_H-$003F_H$	U27 Gate Array (A/D measurement module communications)
0040_H-$007F_H$	Unassigned
0080_H-$00FF_H$	MPU Internal RAM
0100_H-$01FF_H$	Clock chip (Real time clock, alarm, beeper)
0200_H-$05FF_H$	Local Display (Model 52)
0600_H +	Keyboard
$072X_H$-$07AX_H$	Plug-in Option Board Address Decoding
$07E0_H$-$07FF_H$	Power Off
0800_H-$1FFF_H$	Model 52A 6K ROM Bank
2000_H-$27FF_H$	Stack, communication buffers, power-on default values, tables.
2800_H-$2FFF_H$	CALRAM (calibration constants).
3000_H-$5FFF_H$	User Standard RAM
6000_H-$7FFF_H$	Expansion RAM

See the circuitry on the lower half of sheet 2.

U18A divides the lower 32K address space of the MPU into 4 blocks of 8K each. The three most significant address lines contain this information. A15 low enables U18A when the MPU is in the lower 32K. A14 and A13 contain the information as to which 8K block is selected. One output of U18A is low at a time.

False Signal Protection

When in a $\overline{\text{RESET}}$ state, the microprocessor's output lines are tristated (high impedance). To provide RAM and clock chip protection from false signals writing to them, U10-A (sheet 2) is used to provide isolation for the $\overline{\text{8KCALRAM}}$ and R/$\overline{\text{W}}$ signals.

Further decoding is explained under the paragraph for a particular smaller address area.

5.2.8.2 8-16K: CALRAM and User Storage

The 8-16K (2000_H-$3FFF_H$) address space covered by U4 is further broken up. The 2K area between 2000_H and $27FF_H$ is used for the stack, communication buffers, power-on default values, tables, and other things. The 2K area between 2800_H and $2FFF_H$ is for CALRAM (calibration constants). The 2K area above 3000_H is used for user storage.

The enabling line for the 2000_H-$3FFF_H$ area, U18A-5, (sheet 2, lower left), goes across to U10A-13. (Assuming $\overline{\text{RESET}}$, pin 19, is not true), the 8-16K low-enabling signal will be passed to U10A-7. From the U10A buffer it goes to the CALRAM chip select pin, U4-20, on sheet 1.

5.2.8.3 16-24K: User Standard RAM

The 16-24K (4000_H-$5FFF_H$) address space is allotted for the user standard RAM. U18A-6 ($\overline{\text{8KRAM}}$) goes to sheet 1, U7-20, the RAM's chip select pin. (Part of U4 is also available for user storage, to bring the total to about 9.5 Kbytes.)

5.2.8.4 24-32K: Expansion RAM

The 24-32K (6000_H-$7FFF_H$) address space is allotted for Bank RAM. In this address space, A12-A0 decode the individual byte addresses within whichever 8K bank of expansion RAM is switched into the circuit at the time. Which 8K bank of expansion RAM is switched into the circuit at the time is set by the pattern of a data byte sent out on a previous MPU cycle to the appropriate option card slot address. (This address was in the HEX 07XX's. See also paragraph 5.2.8.5.9.)

For theory of operation of expansion RAM boards, see paragraph 5.8.

5.2.8.5 0-8K

5.2.8.5.1 0-8K Overview

The 0-8K (0-$1FFF_H$) address space is allotted for several purposes. The G2B (active low) input of U23 is enabled when the MPU is in the lowest 8K area. The other enabling input of U23, G2A, gets a low true when the MPU is below 2K (0800_H) in any 8K block. Between both G2 inputs, they enable U23 when the MPU is below 2K (0800_H). A10, A9, and A8, contain the information to divide this 2K into 8 blocks of 256 bytes. The lowest 256 byte area (addresses 0-255) is enabled by Y0. The second 256 byte area is enabled by Y1, and so on.

5.2.8.5.2 MPU Internal Registers (00-$1F_H$)

Overview

These lowest 32 bytes are allotted for MPU registers.

The four lowest bytes are used for the two I/O ports (paragraphs 5.2.6.3 and 5.2.6.4.) Each port has its own address. The address lines show this address when the port is being used, even though no address decoding external to the MPU is used. Each port also has a data direction control register associated with it. The state of the bits in this register define whether the respective lines of the port are to be inputs or outputs (0 = input; 1 = output). Table 5-2 summarizes this.

Table 5-2. Some Internal MPU Registers

Address	Function
0000_H	Data direction register, port 1
0002_H	Port 1 port address
0001_H	Data direction register, port 2
0003_H	Port 2 port address

RS-232

The external pins on the MPU corresponding to bits in the port 1 and port 2 registers are used individually — see also paragraphs 5.2.6.3 to 5.2.6.5. RS-232 uses some pins from each port. Four other internal registers in the under-20_H MPU address area contain RS-232 baud rate control, an RS-232 transmit/receive control and status register, and the RS-232 transmit and receive data registers.

Periodic Timing Interrupt

Five other addresses in the under-$1F_H$ area are used for an internal 16-bit MPU timer, a corresponding 16-bit compare register, and a timer control and status register. The combination produces interrupts at either an 8.33 millisecond rate (60 Hz operation), or a 10.00 millisecond rate (50 Hz operation). (50 or 60 Hz operation is set by the UNIT STATUS menu.) Every time this timed interrupt occurs, an interrupt service routine associated with it is run. As part of the routine, the keyboard is scanned (paragraph 5.2.8.5.8, KEYBOARD.)

Also, as part of the routine, if a channel list or DMM mode is running, the MPU pin 9 TOUT ("timer out") line goes low, and then high. TOUT is the source of the latch pulse for the serial transmissions to the measurement modules.

> *Note*
>
> *This timer produces interrupts at fixed intervals. This MPU timer should not be confused with a timer in the clock chip which is programmed when the unit is to be powered up at essentially user-settable times. The timer in the clock chip outputs on the* $\overline{ALARM}$ *line.*

Two other uses for the timed interrupts are for controlling the length of beeper beeps, and to time pre-measurement delays. In these cases, software counts the number of interrupts to get the correct interval.

One more task the MPU does at these timed-interrupt times is to poll (sense) its pin 20. A low on this pin indicates that the B+ is less than +10.58 volts. (Paragraph 5.2.3.7 has more information on "LOW BAT".)

5.2.8.5.3 U27 Gate Array (20_H-$3F_H$)

32-63 (decimal) area. The ST5152 gate array (A/D measurement module interface) is mapped into this area. Different functions of the gate array use various addresses in this area. For theory of operation of the gate array, see paragraph 5.4.

5.2.8.5.4 Unassigned 40_H-$7F_H$

This is the 64-127 area.

5.2.8.5.5 MPU Internal RAM (80_H-FF_H)

This is the 128-255 area. The RAM internal to the MPU is 128 bytes.

5.2.8.5.6 Clock And Beeper (100_H-$1FF_H$)

U3, in the 256-511 area, provides the real time clock function plus an alarm mode. To save battery power, the Model 52 can be "turned off" (V+ supply off). Then at a preset time, the 52 will turn itself on again.

The real time part (not the alarm timer) of the clock chip keeps track of time (year, month, day, hour, minutes, seconds) without needing the MPU, and regardless of whether the V+ power is on or off.

The alarm timer output causes an interrupt when the unit is to be automatically turned on at a set time:

1. A program is to start at a set real time or delta time, and the unit is in power down (monitor) mode.
2. A program scan interval is being timed, and the unit is in power down (monitor) mode.
3. The alarm timer is set for a time anytime in the next day. Since the alarm timer by itself keeps time only in hours, minutes, and seconds, when it goes over midnight, the MPU will be turned on temporarily to reset the timer to a new value counting from midnight. (Then software will turn V+ back off.)

U3 also energizes the beeper, LS1, when the MPU addresses it.

5.2.8.5.7 Local Display (200_H-$5FF_H$)

The 512_{10}-1535_{10} area is pixel on-off storage for the current Model 52 local display pattern. Four of the 256-each decode lines from U23 are required to cover this area. $\overline{DISP1}$-$\overline{DISP4}$ (one low at a time) enable one of the four quadrants of the LCD display to be written to. $\overline{DISP1}$

covers the area from 200_H to $2FF_H$. $\overline{\text{DISP2}}$ covers the area from 300_H to $3FF_H$. $\overline{\text{DISP3}}$ covers the area from 400_H to $4FF_H$. $\overline{\text{DISP4}}$ covers the area from 500_H to $5FF_H$. The system uses address lines A15 through A8 to specify to this level. Display signals are discussed in paragraph 5.6.

5.2.8.5.8 Keyboard (600_H+)

The seventh group of 256 addresses is allotted for the keyboard (1536_{10}+); most are not used.

The MPU reads addresses 0606_H, 0605_H, 0603_H sequentially. This causes the $\overline{\text{KEYBD}}$ line from the decoder to enable the keyboard three times. Each time, a different sector of the keypad is scanned. Keyboard circuitry is discussed in paragraph 5.5.

5.2.8.5.9 Plug-in Option Board Address Decoding ($72X_H$-$7AX_H$)

An address in the eighth group of 256 addresses (U24) is selected when the MPU is used for setting up bank selection of part of the memory on one of the expansion RAM boards, or, when software is turning the unit off. A low from U23-7 enables U24-4. A name for this line might be "$\overline{1792_{10}\text{-}2047_{10}\ (700_H\text{-}7FF_H)}$". Anytime an address in this range is being accessed, one of the eight outputs of U24 is true low.

The combination of A5, A6, and A7 divides this 256 byte range into 8 blocks of 32 bytes each (20_H).

There are 5 motherboard sockets for plug-in rear panel option boards such as Digital I/O, GPIB, or Expansion RAM. The sockets are J7-J11, corresponding to rear panel slots 5 through 9. The Y1 through Y5 ($\overline{\text{BD1}}$-$\overline{\text{BD5}}$) outputs of U24 (sheet 2) select one of the five slots that the MPU will talk to. To decode to this level, A15 through A5 are used. The addresses that the MPU uses to communicate with any digital I/O or GPIB board are in the $72X_H$-$7AX_H$ area.

The address 07X0 is also used for sending a bank selection byte to an expansion RAM board. The number that the software uses for X (2, 4, 6, 8, or A) determines which of the five plug-in slots the bank selection byte will go to. Expansion RAM addressing is discussed under paragraph 5.2.8.4.

The 32 possibilities within one of these blocks are addressed by A4-A0. A given address within the block serves a different purpose depending on which kind of board is plugged in the slot. Table 5-3 summarizes the routing of the signals from U24.

The block of 32 bytes beginning at 07C0 are not used.

Table 5-3. U24 Decoder Outputs

Pin #	Block Begins At Hex Address	Signal Name	To Mother-Board Connector	Rear Panel Slot #
U24-15	0700_H	$\overline{\text{BANKSEL}}$		
U24-14	0720_H	$\overline{\text{BD1}}$	J7	5
U24-13	0740_H	$\overline{\text{BD2}}$	J8	6
U24-12	0760_H	$\overline{\text{BD3}}$	J9	7
U24-11	0780_H	$\overline{\text{BD4}}$	J10	8
U24-10	$07A0_H$	$\overline{\text{BD5}}$	J11	9
U24-9	$07C0_H$			
U24-7	$07E0_H$	$\overline{\text{PWROFF}}$		

5.2.8.5.10 Plug-in Slot Address Line Buffering

See schematic sheet 3. Since the MPU has limited drive capability, U25 and U26 are used for data and address line buffering. U25 is a bidirectional buffer. U26 always drives toward the plug-in slots; it always has its left-side signals on the schematic as inputs.

U25 must buffer the low order address information from left to right during the first part of a cycle. Then, it must buffer the data from a plug-in slot onto the MPU bus during the data part of a cycle, if an appropriate address is being read from. The direction control for U25 is "DIR", pin 1. When DIR is high, U25 will buffer (transmit) the MPU's low-order address information to plug-in cards. When DIR is low, U25 buffers any data from plug-in cards onto the MPU bus.

I/O Direction Control

DIR comes from the direction flip-flop, U22C/D, on sheet 2, zone A3. The flip-flop is set or reset by one of its inputs going high. The flip-flop will go to (or remain in) the DIR-high state each time an AS (address strobe) high-pulse arrives at U22D-12.

See zone B5. Input of inverter, U19A-1, is the 700_H-$7FF_H$ decode line. (Recall that this is the low-enable line for digital I/O or GPIB transfers. This is also the low-enable line for expansion RAM bank-selection transfers.) Input of inverter, U19B-3, is the 800_H-$1FFF_H$ decode line. (This is the low-enable line for the Model 52A 6K ROM.) When the MPU selects an address in either of the two foregoing address spaces, OR-gate output U20D-11 goes high.

If the MPU is setting up to write to or read from the 6000_H-$7FFF_H$ area (an expansion RAM), then U18A-7 will be driving inverter input U19C-5 low. U19C-6 will be high.

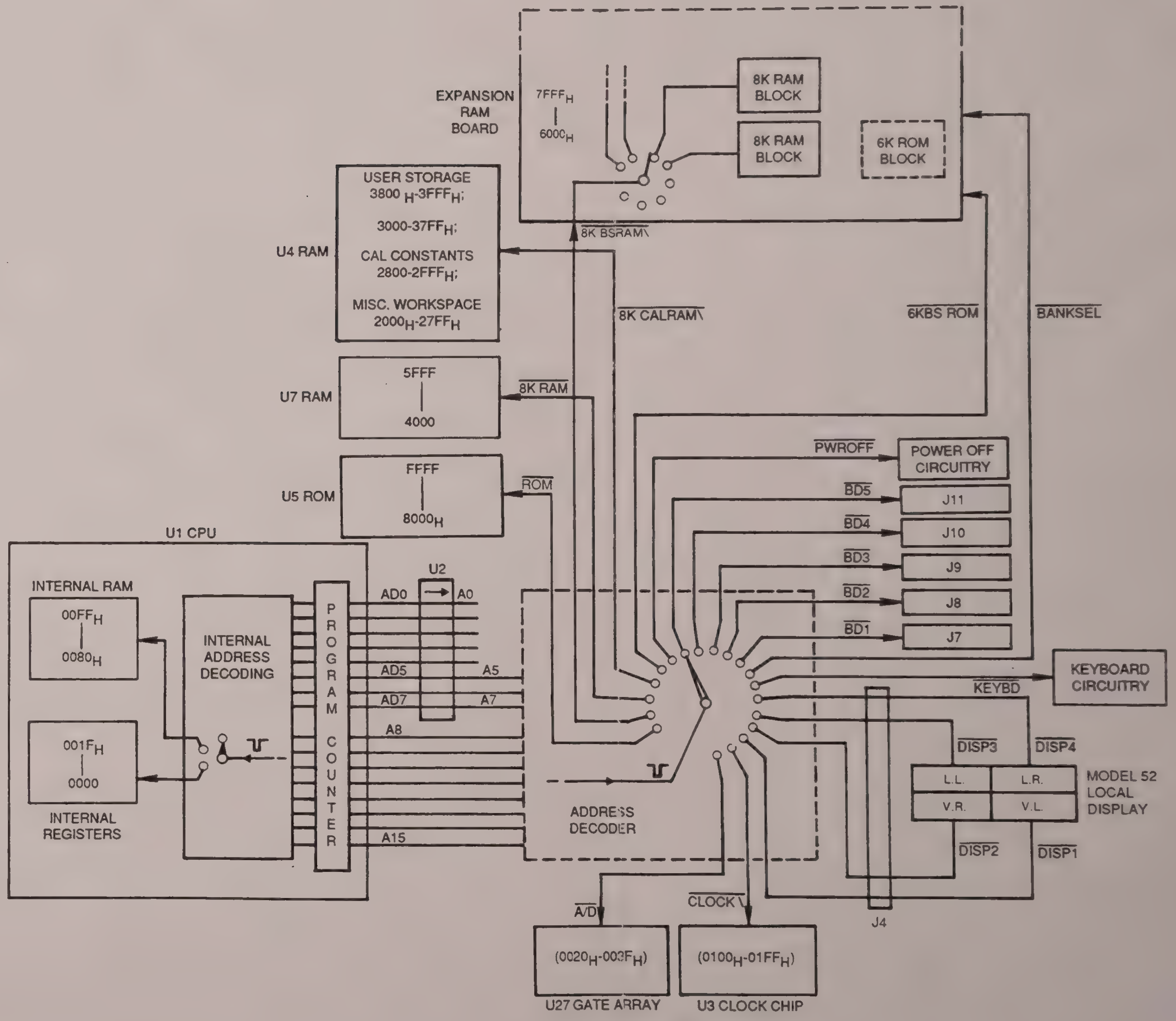
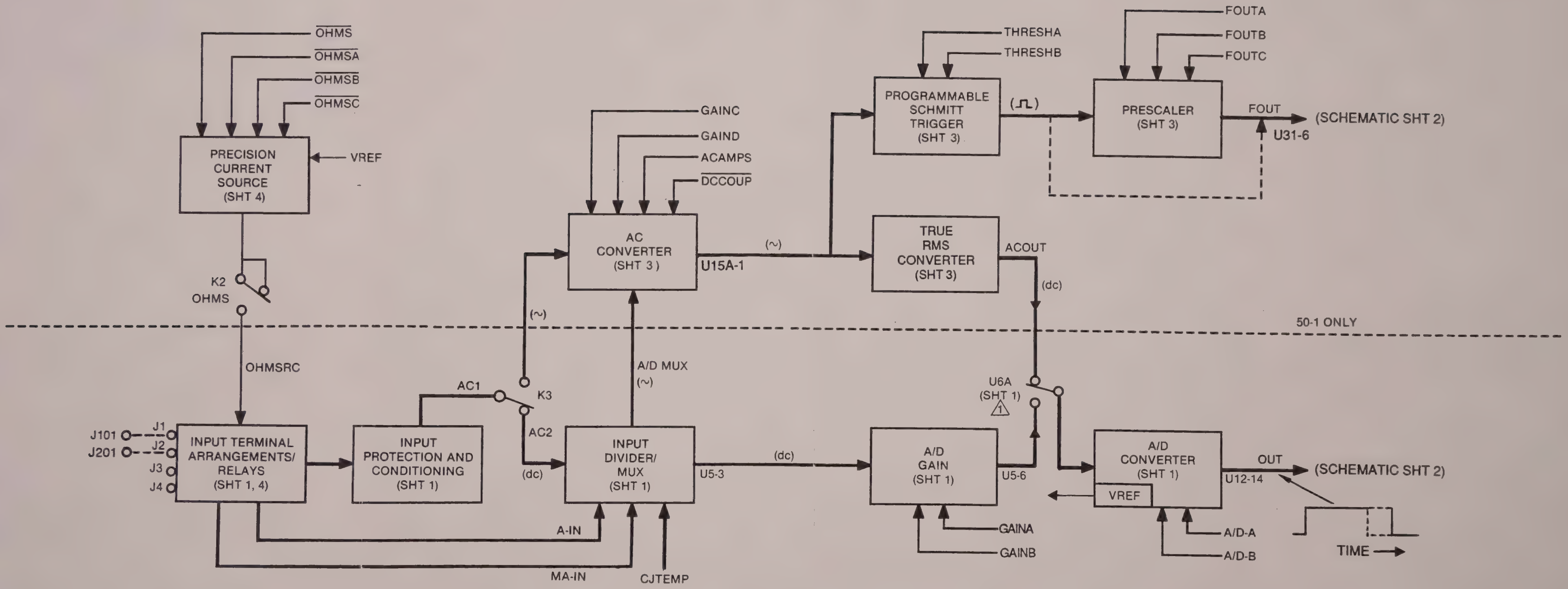

EXPANSION RAM BOARD
7FFFH
6000H
8K RAM BLOCK
8K RAM BLOCK
6K ROM BLOCK
USER STORAGE 3800H-3FFFH;
3000-37FFH;
CAL CONSTANTS 2800-2FFFH;
MISC. WORKSPACE 2000H-27FFH
U4 RAM
8K BSRAM\
8K CALRAM\
6KBS ROM
BANKSEL
U7 RAM
5FFF
4000
8K RAM
U5 ROM
FFFF
8000H
ROM
PWROFF
POWER OFF CIRCUITRY
BD5
J11
BD4
J10
BD3
J9
BD2
J8
BD1
J7
U1 CPU
INTERNAL RAM
00FFH
0080H
001FH
0000
INTERNAL REGISTERS
INTERNAL ADDRESS DECODING
PROGRAM COUNTER
U2
AD0
A0
AD5
A5
AD7
A7
A8
A15
ADDRESS DECODER
KEYBOARD CIRCUITRY
KEYBD
DISP3
DISP4
L.L.
L.R.
V.R.
V.L.
MODEL 52 LOCAL DISPLAY
DISP2
DISP1
J4
A/D
CLOCK\
(0020H-003FH)
(0100H-01FFH)
U27 GATE ARRAY
U3 CLOCK CHIP

Figure 5-10. Devices Using Address Decoding


OHMS
OHMSA
OHMSB
OHMSC
PRECISION CURRENT SOURCE (SHT 4)
VREF
K2 OHMS
OHMSRC
GAINC
GAIND
ACAMPS
DCCOUP
AC CONVERTER (SHT 3)
U15A-1
(~)
THRESHA
THRESHB
PROGRAMMABLE SCHMITT TRIGGER (SHT 3)
FOUTA
FOUTB
FOUTC
PRESCALER (SHT 3)
FOUT
U31-6
(SCHEMATIC SHT 2)
TRUE RMS CONVERTER (SHT 3)
ACOUT
(dc)
50-1 ONLY
(~)
A/D MUX
(~)
AC1
K3
AC2
(dc)
U6A
(SHT 1)
J101
J201
J1
J2
J3
J4
INPUT TERMINAL ARRANGEMENTS/ RELAYS (SHT 1, 4)
INPUT PROTECTION AND CONDITIONING (SHT 1)
INPUT DIVIDER/ MUX (SHT 1)
U5-3
(dc)
A/D GAIN (SHT 1)
U5-6
A/D CONVERTER (SHT 1)
VREF
OUT
U12-14
(SCHEMATIC SHT 2)
A-IN
MA-IN
CJTEMP
GAINA
GAINB
A/D-A
A/D-B
TIME

NOTES

1. U6A is an Analog Switch.
2. 50-2 Module does not contain the circuitry above dashed line.
3. Some, but not all programming signals are shown.
4. (SHT X) refers to a sheet number of the measurement module schematic.

Figure 5-11. Block Diagram, Measured-Quantity Signal Flow

A high at an input of U22A, from being in either of the two preceeding paragraphs' address spaces (700_H to $1FFF_H$, or 6000_H-$7FFF_H$), will cause U22A-1 and thus U22B-5 to be low.

The $\overline{RD}$ signal at U22B-6 is high except during the data time of a read cycle. $\overline{RD}$ comes from U18B-9. $\overline{RD}$ goes low when $R/\overline{W}$ is high (a read cycle is being performed) and then E goes high (data time).

In zone A3, when the address space is correct (low at U22B-5) and the data period of a read cycle starts (low at U22B-6), then the high at U22B-4 will flip the DIR line low. This will cause the U22 buffer (sheet 3) to receive from the slots and transmit to the MPU (until the next AS comes along).

This illustrates that only a read from an appropriate address space will switch the U25 buffer back "toward" the MPU.

In summary, an MPU write to any address (plug-in address or not) will have the U25 and U26 buffers sending address and data to the plug-in slots. And only a read from an appropriate address will turn the U25 buffer around so that data from a plug-in board can be put on the MPU data bus.

5.2.8.5.11 Power Off (7E0-7FF)

Any read or write to address $07E0_H$ to $07FF_H$ activates the $\overline{PWROFF}$ decode line and turns the unit off. Software uses $07FF_H$. Turn off sequences are explained in paragraph 5.2.4.

5.3 MEASUREMENT MODULES

5.3.1 50-1 And 50-2 Overview

5.3.1.1 Measured-quantity Signal Flow

The following discussion covers the 50-1 measurement module which contains the circuitry for all 24 analog measurement functions. If the reader has the 50-2 measurement module, the sections pertaining to the blocks above the dashed line on figure 5-11 may be skipped.

Refer to the block diagram of the analog signal flow, figure 5-11. (Bold lines denote measured-signal flow. Lighter lines are mode-setup signals controlled by software.)

Any signal that the Model 52 is to measure must be in, or converted to, a frequency or time-duration parameter so the digital circuitry on the motherboard can process it. The two signals, **OUT** and **FOUT**, are of this type. They go through some gating circuitry that selects which one, and then through an opto-isolator onto the motherboard.

DC Voltages

A front panel voltage or thermocouple signal to be measured comes into the instrument at J1 with respect to J2. A rear panel signal to be measured comes into the instrument at J101 with respect to J201. Relay K1 selects either front or rear panel, and puts the selection on K1-13. The signal then passes by the input protector E1 (600 volt breakdown), and goes to K3-13 (point AC1, schematic locations 1D6 and 3D8). Since DC is being measured; software tells K3 to route it to AC2 and the INPUT DIVIDER/MUX. This stage divides it by either 1 or 100. Then the A/D GAIN stage multiplies it by 1, 10, or 100. This combination allows possible gains of 0.01 through 100. The DC signal then goes to the A/D Converter through U6A. The output of the A/D Converter is a logic-level high signal whose time-duration is proportional to the input DC voltage.

An internal signal, called CJTEMP, used for thermocouple cold-junction compensation, can be switched into the system, as an input to the INPUT DIVIDER/MUX.

AC Voltages

A front panel voltage or time-domain signal to be measured comes into the instrument at J1 with respect to J2. A rear panel voltage or time-domain signal to be measured comes into the instrument at J101 with respect to J201. Relay K1 selects either front or rear panel, and puts the selection on K1-13. The signal then passes by the input protector E1 (600 volt breakdown), and goes to K3-13 (point AC1, schematic locations 1D6 and 3D8). Assume AC is being measured; software tells K3 to route it to the AC Converter circuit.

The AC CONVERTER (an amplifier) can multiply the signal by 0.01, 0.1, 1, 10, or 100. The circuit's output at U15A-1 is a normalized ac signal in the 0 to 3.2 volt rms range. If voltage is to be measured, the True RMS Converter converts it to a positive DC signal at ACOUT, in the 0 to + 3.2 VDC range. Analog switch U6A routes this to the A/D Converter. The output of the A/D Converter at OUT is a logic level (high) signal that has a duration proportional to the input voltage. This signal gets gated through an opto-isolator to the motherboard.

Other AC Signals

If a time-domain signal such as frequency, period, pulse width, or time is to be measured, the output of the AC CONVERTER goes to the Programmable Schmitt Trigger. The upper and lower levels where this circuit switches logic state are programmable. The output is "cleaned up", electrically noiseless, logic levels (high or low) with fast rise and fall times.

If pulse width or time is to be measured, the Programmable Schmitt Trigger output goes around the prescaler to FOUT. The FOUT signal gets gated through the same opto-isolator as in the previous paragraph to the motherboard.

If frequency or period are to be measured, the prescaler circuitry is programmed to divide by a number between 1 and 16384. The divided-down signal, FOUT, goes to the opto-isolator.

Resistance

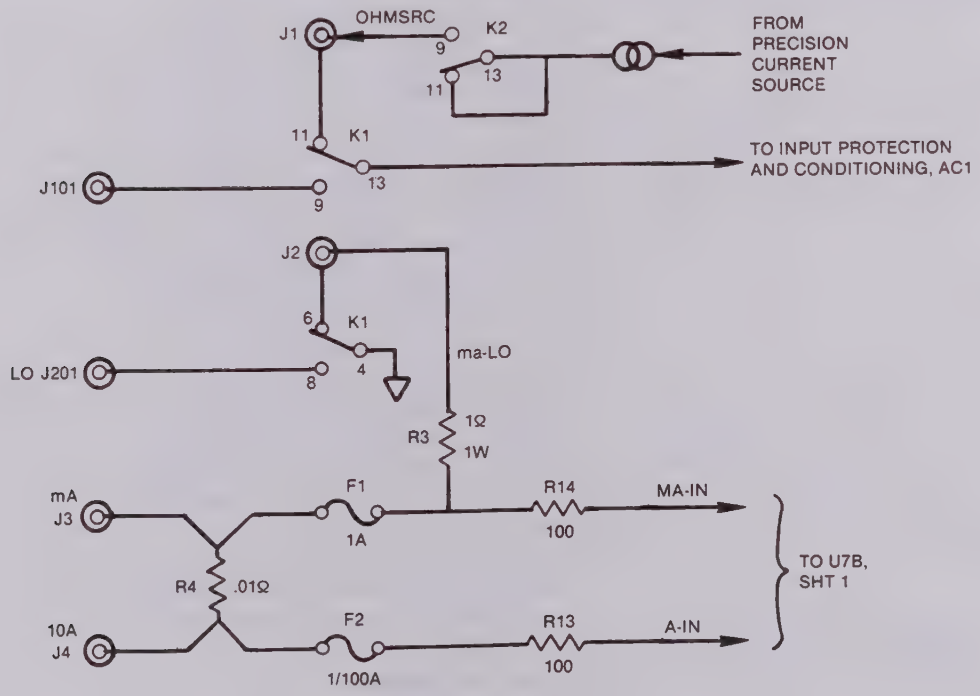
Two-terminal resistance measurements are done by sourcing a known current through an unknown external resistance connected across J1 and J2 (on the front panel). By Ohm's law, the resultant voltage at J1 is proportional to the resistance.

The programmable Precision Current Source is the source of the tightly controlled constant current. After going through the switching relay K2 (schematic location 4B7), this constant current feeds out through J1. The dc voltage developed follows the same signal path as a normal dc signal: in J1, into K1-11, out K1-13, to K3-13 and AC1.

Four-terminal current measurements are done by sourcing current from the front panel J1 terminal, with J2 as the current return. J101 and J102 on the rear of the measurement module sense the voltage generated across the unknown resistance. Even though the rear panel input is specified as the measurement channel, the source current comes only from the front panel J1.

50-2 Module

A 50-2 measurement module has no Ohms or AC capability. Since the ability to switch these functions in or out is not required, K2 (ohms switching) and K3 (AC switching) are not installed. Where K3 would have been installed are two solder pads: AC1 is next to K3-13, and AC2 is next to K3-11. "R5", a 0-ohm chip resistor, is connected across here, to make the connection that the pole of K3 would have made.



Note 1) Not Shown: Current measurement (4-terminal) using an external MUX.

Figure 5-12. Input Terminal Arrangements, Measurement Module

Current

Current measurements use shunt resistors in the Model 52 to create a small voltage. Currents up to 320 milliamps AC or DC, use the input J3 terminal as high and the J2 terminal as low. Currents up to 10 amps are measured using J4 as high and J3 as low. Refer to the Input Terminal Arrangements drawing, figure 5-12. The 320 milliamp terminals use the 1-ohm resistor R3 as the current sense. The 10 amp terminals use the .01-ohm resistor R4 as the sense.

If the current being measured is **AC**, the A/D INPUT MUX routes either the A-IN or the MA-IN signal to the AC Converter via the A/D MUX line. After being amplified by the AC Converter, the True RMS Converter converts it to the positive dc signal called ACOUT. Then ACOUT goes through U6A to the A/D Converter.

One reason that ac and dc signals have different gain paths is that the dc path must be optimized for low offset voltage, while the ac path must be optimized for wide bandwidth to preserve high frequency gain accuracy.

Note

How FOUT or OUT is gated onto the motherboard, and how the motherboard processes this signal, is explained in paragraph 5.4, Measurement Control. Paragraph 5.4 also explains in detail how a measurement setup is serially transmitted to a measurement module and converted into parallel control lines. Readers interested primarily in the analog theory may skip paragraph 5.4. If skipping paragraph 5.4, the reader may refer to figure 5-27, Measurement Control, at the end of paragraph 5.4.

5.3.1.2 Software Controlled Lines And Relays

The microprocessor on the motherboard controls which function, gain, current, and divide ratio the circuits in the measurement module are set to. U27, the gate array on sheet 3 of the motherboard schematic is the CPU's interface to the measurement modules.

See sheet 2 of the measurement module schematic. Setup data goes to a module in serial format using opto-isolators U24A, U24B, and U23. It can be sent 8 bits or 32 bits at a time. U30, U34, U13, and U10 are serial-in, parallel-out shift register/latches (SIPO's). See figure 5-13, a simplified schematic of the serial-in, parallel-out shift register arrangement. For an 8-bit shift, data is sent only to U30; the clock to U34, U13, and U10 is inhibited. For a 32-bit shift, all four IC's get clocked and data streams serially through U30, U34, U13, and U10 in that order. When an IC gets the LATCH signal, it latches the data and updates the parallel outputs.

These shift register outputs are static ones and zeroes, until updated by a new serial shift from the motherboard.

Control Lines Functional Overview

U30 output lines A/D-A and A/D-B (schematic location 2C6) are used to cycle the dual slope A/D CONVERTER. The LEDEN line enables or disables signals to the U22 opto. FOUTA, FOUTB, and FOUTC select the divide ratio of the frequency counter PRESCALER. K5SET and K5RST are used to set or reset the divide-by-one-hundred relay (contacts at 1C6 and 3C8). (See also The Latching Relays, below.)

U34 (2A3) controls the 9-pin D connector (J6) on the back of the measurement module. U34 outputs Q1-Q6 send subchannel selection information out of the Model 52 to a MUX. Also, U34 Q7 and Q8 send threshold-level

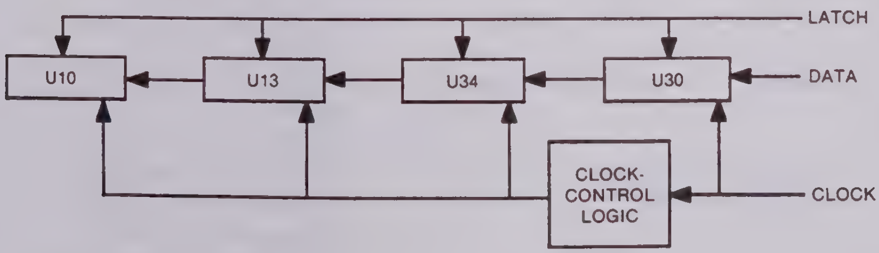


Figure 5-13. SIPO Control Registers

programming information to the PROGRAMMABLE SCHMITT TRIGGER circuit. Since the schmitt trigger is not used during temperature measurements, J6-7 can serve another function: A high commands an external multiplexer to send its cold-junction value.

U13 (2A5) provides four lines of gain-programming information to the AC CONVERTER amplifier section. The lower four control lines from U13 are inverted by U8, which feeds four lines of ohms-range information to the PRECISION CURRENT SOURCE. When the current sourcing function is not needed, the OHMS, OHMSA, OHMSB, and OHMSC logic states are irrelevant. This allows ACAMPS (OHMSB) to be used on the AC AMPereS measurement function (3C7). This also allows DCCOUP (OHMSC) to control DC COUPling (3D3). Also, A/DINA and A/DINB are used to control the U7B "selector switch" position (1C5).

U10 (2A6) supplies eight bits of relay control. The signals from U10 are inverted by inverters in U9 and U8. A high from U10 causes a low on the corresponding output of U8 or U9, which energizes the relay coil.

U8 and U9 each have six open-collector Darlington transistor stages. Each stage has internal diode protection from the turn-off inductive kick from the relay coil.

The Latching Relays

K1 through K5 are double pole, double throw, self-latching type relays, with a SET coil, and a RESET coil. Removing drive from the set coil (pin 16 going back high) does not reset them — they would need a pulse in the reset coil to reset them, and vice-versa. This functions like a set-reset flip flop.

To save power, a relay is pulsed only for the duration of one timing period. One timing period using 60-HZ line power is 8.33 milliseconds. One timing period using 50-HZ line power is 10.0 milliseconds. The timing period is set by the UNIT STATUS menu.

Figure 5-14 shows the electrical pinout of a latching relay.

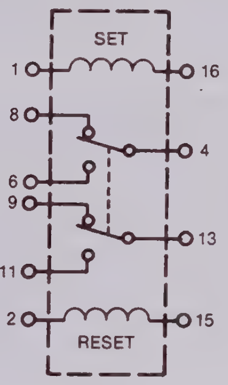


Figure 5-14. Latching Relay Pinout

The relay poles in figure 5-14 are shown in the set position. This means that the relay coil between pins 1 and 16 was the last coil to have a potential difference across it.

Table 5-4 shows where in the measurement module the contacts of each relay are used, and the general function of each.

Table 5-4. Latching Relay Usage

Relay	Contacts	Location	Contacts	Location	General Function
K1	4, 6, 8	1B6	9, 11, 13	1D7	When SET, selects rear panel input; typically a multiplexer.
K2	4, 6, 8	1B6	9, 11, 13	4A7	When SET, connects the constant current source to front panel.
K3	4, 6, 8	3B8	9, 11, 13	3D8	Routing of input signal to DC or AC section. If AC, is SET; this also turns on +12VSW (and indirectly, −12) to AC section.
K4	4, 6, 8	3D8	9, 11, 13	1D5	SET for DC coupling in the AC section, if measuring AC. SET for divide by 100, if measuring DC volts, or to select MA-IN, A-IN (from current shunts), or to select the CJTEMP signal.
K5	4, 6, 8	3C8	9, 11, 13	1C6	SET for divide by 100 (/100) in AC section, or DC section.

Full explanations of relay usage are in the individual circuit descriptions in paragraph 5.3.2.

5.3.2 Measurement Module Detailed Circuit Description

5.3.2.1 Power Supply

The power source for the Measurement Module is an electrostatically-isolated, oscillating voltage-converter module made by Burr-Brown. The low capacitance resulting between the measurement module common and the motherboard allows the Low input of the measurement module to function as a second input for differential measurements, even for ac. Refer to sheet 5 of the measurement module schematic.

The capacitance between the input and output sides of the Burr-Brown converter, U25, is typically 25 picofarads with no other circuitry connected. The total measurement module J2-input capacitance to chassis ground is typically under 100 picofarads.

U25 takes in +6 volts from the motherboard on the V+6 line, and has two unregulated outputs. U25-5 is about +6 volts DC with respect to TP1. U25-4 is about +6 volts DC with respect to U25-5. This makes U25-4 about +12 volts with respect to TP1 ground. These voltages vary somewhat as the loading changes.

Via U27, the CPU can remove power from any measurement module (the $\overline{\text{PSEN}}$ line). This occurs if the unit is in the power save mode, and the measurement module in question is not currently taking a measurement. When the $\overline{\text{PSEN}}$(n) line from the motherboard is high, the Burr-Brown module will be off.

+6VRAW

The +6VRAW line, about +6 volts, feeds the relay coils, and U9-9, on sheet 2.

+5, −V

VR2 is a low quiescent current, low dropout voltage regulator. It takes in +6VRAW from U25-5 and regulates it to +5 volts. This +5, besides going to several ICs, feeds the input of the ICL7660.

U26 takes whatever DC voltage is on pin 8 and converts it to virtually the same voltage, but negative, at pin 5. −V equals −5 volts. U26 uses internal FET switches to alternately connect C53 across the input pins (pin 8 and pin 3), and then reversing C53, connect it across the output capacitor (pin 3 and pin 5). One pair of analog switches, A and C, or B and D, are closed at one time. A pair disconnects C53 before reconnecting it the other way.

This charge-transfering from capacitor to capacitor, or "charge pumping", is controlled by an internal 10 KHz oscillator in the ICL7660. If either the charge pump capacitor, C53, or the charge reservoir capacitor, C52, are open, the circuit won't function. The action is illustrated in figure 5-15.

+11.5V

VR3 is a low power version of the LM317 regulator. A feedback amplifier in the LM317 maintains about

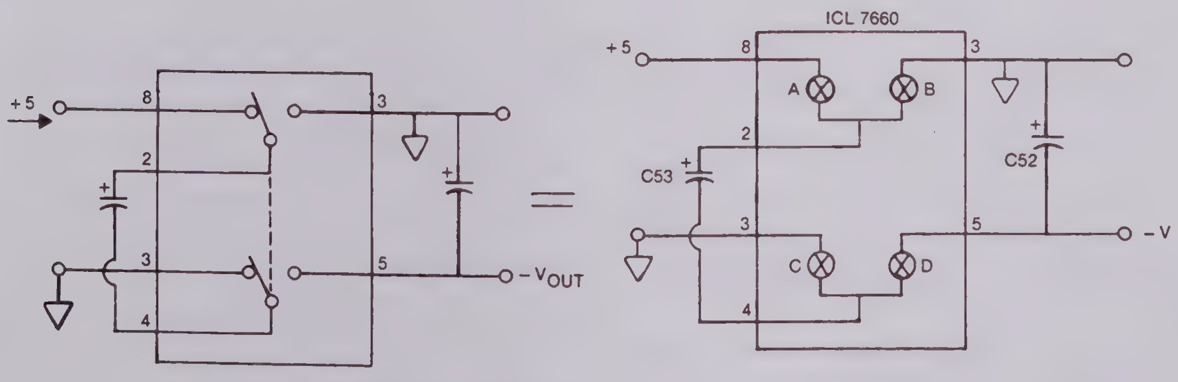


Figure 5-15. ICL7660 Operation

1.25 volts between the OUT and ADJ terminals. By dividing down the feedback to the ADJ pin, VR3 pin 2 is made to put out a nominal +11.5 volts. Due to lighter loading in the ohms mode, as opposed to an ac measurement mode, VR3 loses regulation and pin 2 rises to above 12 volts. This is desired — to get more voltage for the current source circuit.

+12VSW, −12

+12VSW is switched +11.5V. See sheet 3, zone B7. K3 turns off plus power to U15 and U16 (3C2) when the measurement module is not doing an ac measurement function.

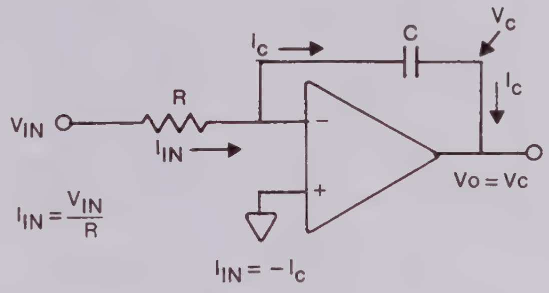
U11 is a positive-to-negative voltage converter. It takes in a nominal +12 volts on pin 8 and outputs −12 volts on pin 5. The operation is the same as the ICL7660. Since the ICL7660 is rated to only 10 volts on its input, the higher rated 7662 is used here.

When the +12VSW is removed by K3 opening, −12 is also removed from U15 and U16.

5.3.2.2 A/D Converter

The A/D Converter is the heart of the measurement module in any mode where amplitude is being measured — volts, amps, or ohms. It converts an analog dc voltage input to a time-duration, logic-level signal. Refer to the measurement module schematic, sheet 1. VR1 is a precision 2.5 volt bandgap reference. The A/D Converter, U12, is a TSC500 IC made by Teledyne Semiconductor. U12 is a dual-slope integrating type of converter. It integrates first the unknown signal to a level determined by the signal amplitude, then switches to a known reference input and "deintegrates" until the integrator output ramps back to zero. The time this second slope takes is proportional to the amplitude of the unknown signal.

See figures 5-16 and 5-17. The voltage change across a capacitor is a function of the current fed into it times the time this occurs. It follows the equation CΔv = IΔt.



a) $C\Delta V = I\Delta t$

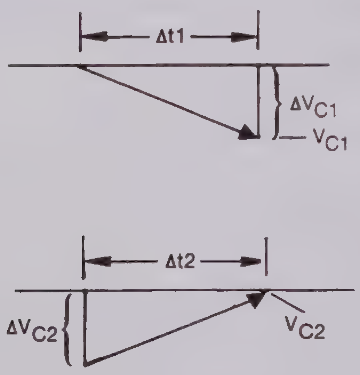
b) or $V_c = \frac{I\Delta t}{C}$

c) $I_c = -\frac{Vin}{R}$

d) $\Delta V_c = -\frac{Vin}{R} * \frac{\Delta t}{C}$

Figure 5-16. Simplified Integrator

C21 and R19 correspond to R and C in the circuit above. Assume the output of the integrator starts at zero. Then let an unknown + dc voltage be connected to Vin. Since the op amp wants to keep its negative input at virtual ground, it will source (−) current back through the capacitor to balance out the input current through the resistor. The magnitude of the feedback current is given by equation c.



Let the integrator output start and end at zero. Then

$0 + \Delta V_c = -\frac{Vin}{R} * \frac{\Delta t_1}{C}$ Op amp output ramps to a negative voltage, described by equation d.

$0 = V_{C2} = V_{C1} + \Delta V_{C2}$ Op amp output ramps back to zero.

$V_{C2} = -\frac{Vin}{R} * \frac{\Delta t_1}{C} + -\frac{Vref}{R} * \frac{\Delta t_2}{C}$ (Circuit makes Vref opposite in effective polarity to Vin.)

$-\frac{Vref\Delta t_2}{RC} = \frac{Vin\Delta t_1}{RC}$ Dropping the V_{C2} term.

$-Vref\Delta t_2 = Vin\Delta t_1$

$-Vref\frac{\Delta t_2}{\Delta t_1} = Vin$ But $\frac{-Vref}{\Delta t_1} = K$, a constant. So $K\Delta t_2 = Vin$

Figure 5-17. Integrator Ramps

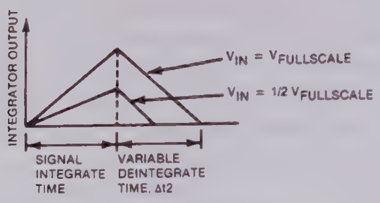


Figure 5-17a. Combined Integrator Ramps

Since Vref and Δt_1 are fixed, the duration of Δt_2, the deintegrate time, gives the measure of Vin, the unknown.

By using dual instead of single slope conversion, the accuracies of R and C no longer affect the accuracy of the conversion process. In the example the unknown signal was stable dc. But it could have had noise riding on it: the circuit, being an integrator, is relatively insensitive to noise which has no dc component. If the signal was changing dc level during the integration period, the converter would produce the average value.

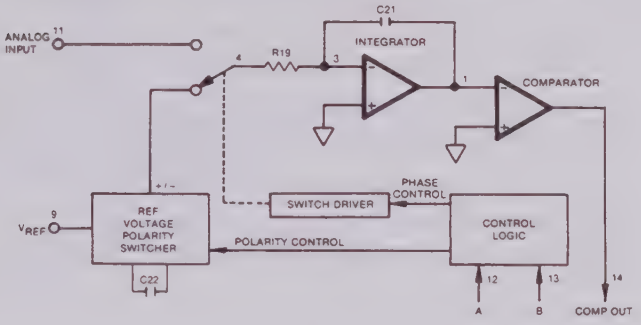
Time of the Integrate Phase

A common frequency of signal noise is the line frequency, 50 or 60 Hz. By setting the integration phase time period to some multiple of the periods of these frequencies, a high degree of rejection is achieved. At 60 Hz, for a 4 1/2 digit resolution reading, integrate time is **66.66 mSec**. At 50 Hz, the time is **60 mSec**. For 3 1/2 or 2 1/2 digit readings, 60 Hz time is **16.66 mSec**.; 50 Hz time is **20 mSec**.

U12 has two other phases besides integrate and deintegrate. They are an integrator output zero phase and a system zero (auto zero) phase. The integrator output zero phase is useful for making the integrator recover quickly from an overrange signal on the previous measurement cycle. The auto zero phase balances out any errors due to buffer, integrator, and comparator offset voltages. This ensures that a zero input will cause a zero output. C23 is the auto zero capacitor which holds the sum of these small offset voltages.

Which state the converter is in is controlled by the state of the A/D-A and A/D-B lines.

Figure 5-18a is a simplified block diagram of the circuits in the TSC500 A/D Converter. Figure 5-18b shows the four possible phases of the TSC500.



a

A/D-A	A/D-B	Converter State
0	0	Zero Integrator Output
0	1	Auto Zero
1	0	Signal Integrate
1	1	Deintegrate (V_{REF})

b

Figure 5-18. Simplified Converter Operation

Controlling the Integrate Phase

The motherboard MPU causes the gate array U27 to send out an 8-bit serial data stream which sets the output bits in U30 (sheet 2) to the proper 1 or 0 states. When the motherboard sets the A/D-A and A/D-B lines to 1,0 respectively, the A/D converter starts the integrate phase. Internal analog switching connects the unknown signal (A/D INPUT) to the integrator input. The ramping waveform can seen with an oscilloscope on the end of C21 connected to the integrator output, U12-1. (The other end of C21 stays near virtual ground, having only small offset voltages on it.) The beginning and end times of the integrate time are precisely controlled by when the MPU and software cause the latch pulse to be sent to the measurement module. These times correspond to interrupt times on the motherboard. At the proper times the MPU sends out latch pulses on the TOUT line, U1-9.

Starting the Deintegrate Phase

After the integrate phase is complete (a preset time), the motherboard does another 8-bit shift to the measurement module. Now the A/D-A and A/D-B lines switch to 1,1 respectively. This 1,1 on the control lines puts the converter into the deintegrate phase. Instead of the unknown signal, the input for the converter is now the

VREF signal (+2.5 volts) at pin 9. Internal logic circuitry in the converter selects the proper polarity of input to the integrator so that it's output will ramp back to zero. This logic circuitry controls analog switches that apply the correct polarity of the Cref cap, C22, to the integrator input. Prior to the start of the deintegrate phase, C22 was connected across REFHI and REFLO, so it has a voltage equal to VREF. The time from the start of this 1,1 on the control lines to the time the comparator OUT line switches back low is the measure of the amplitude of the A/D INPUT.

Time of the Deintegrate Phase

If the unknown signal amplitude were very small, pin 14 would switch back low almost instantaneously, to give an example. A full scale input to the A/D Converter is +3.2 or -3.2 volts. This corresponds to a deintegrate time of 3.2/2.5 times the integrate time. The time of the deintegrate phase is Vin/2.5 times the integrate time. For example, if the unknown Vin is 1.25 volts (+ or −), the deintegrate ramp will take one-half as long as the integrate ramp. The pin 14 transition goes immediately to the motherboard U27 gate array, to stop a counter. A small time later, the motherboard shifts over a new serial setup to take the A/D converter out of the deintegrate phase. The user can specify as a display modifier the desired resolution:

32000 counts — 4 1/2 digit resolution,
3200 counts — 3 1/2 digit resolution,
or 320 counts — 2 1/2 digit resolution.

(The Model 52 RES menu presents the choice in terms of the number of counts, not the number of digits. In remote, the Models 51 and 52 require a RES:LOW, MED, or HIGH specification, according to Operator Manual table 5-11.)

Table 5-5 gives the deintegrate times for various Vin's and resolutions.

Table 5-5. Deintegrate Times

Vin	Digits Resolution	Integrate Time (mSec)		Resulting Time To Deintegrate (mSec)	
		50 Hz	60 Hz	50 Hz	60 Hz
1.25	4 ½	60.0	66.66	30.0	33.33
2.50	4 ½	60.0	66.66	60.0	66.66
3.20	4 ½	60.0	66.66	76.8	85.4
1.25	3 ½ or 2 ½	20.0	16.66	10.0	8.33
2.50	3 ½ or 2 ½	20.0	16.66	20.0	16.66
3.20	3 ½ or 2 ½	20.0	16.66	25.6	21.3

Table 5-6 is a table showing the state of the pin 14 comparator output "OUT" in relation to which of the two ramping phases the converter is in. Pin 14 has polarity information on it during the integrate phase: high means Vin is positive, low means Vin is negative. After going through some gating and an opto to the motherboard, this polarity is read by the U27 gate array during the integrate phase. At the start of the deintegrate phase, the converter forces pin 14 high regardless of input polarity.

Table 5-6. Comparator Output Pin States

Operating Phase	Input Signal Polarity	Comparator Output
During integrate	+	1
During integrate	−	0
During deintegrate	Don't care	1
Deintegrate finished	Don't care	↓

C21, C22, and C23 are low leakage, low dielectric absorbtion types. Low dielectric absorbtion is particularly important for C21, the integrating cap. Since the voltages on C22 and C23 are fairly stable voltages, low dielectric absorbtion is not so important for them.

Inputs to the A/D Converter

Analog signal switching in the measurement module is done by relays and analog switches. The analog switches are monolithic dual one-of-four's. U2, U6, and U7 are of this type. The A/D converter can have as an input from U6A either the output of the dc gain stage (U5-6), or the output of the ac section (ACOUT). The noise filter, R17 and C19, is −3dB at about 724 Hz.

5.3.2.3 True RMS Converter

The TRUE RMS CONVERTER circuit, (3C2), converts ac signals to dc so that the A/D CONVERTER can measure them. The AD637 rms converter's circuits implement the terms in the equation

$$\mathrm{Vrms} = \mathrm{Avg}\left|\frac{\mathrm{Vin}^2}{\mathrm{Vrms}}\right|$$

Although this is not the form of the RMS equation probably most familiar to the reader, using this analog "running average" approach to implementing the rms function avoids the problems associated with piecemeal calculations for an rms value. The AD637 combines high speed performance with high accuracy. Complex ac or ac + dc waveforms are fed to the Vin terminal and a running representation of the RMS value appears at pin 14, the BUFFOUT terminal, as a dc voltage.

In figure 5-19, a simplified schematic of the converter is shown. The input, Vin, is at the lower left, pin 13. The absolute value of this term is produced by the circuit around op amp A1. It can be thought of as a clamping type of circuit. The one-quadrant squarer produces the Vin^2 function which is divided by the feedback signal, RMS OUT. This RMS OUT signal can be further filtered before going to the DENIN (denominator input) (as in our case) to increase low frequency accuracy. A capacitor (C39) around A4 (pins 9 to 8) provides the averaging function in the equation.

An on-chip buffer amplifier is used to make a two-pole low pass filter. It is redrawn in more familiar form in figure 5-20. Note that the final term, ACOUT, from the circuit, is taken from the output of the buffer, pin 14, and not from pin 9.

Input impedance of the AD637 is 12Kohms. Gain of the device is 1 — that is, 1 volt rms in produces + 1 volt dc out. Further information on rms-to-dc converters of this type is available in Analog Devices, Inc. publications, or in texts on op amp applications.

5.3.2.4 AC Converter

The AC CONVERTER section (measurement module schematic sheet 3) provides ac gain. Quad op amp U15 is a high slew rate type.

If taking voltage (or frequency) readings, the circuit amplifies ac (or ac + dc) voltage signals coming in J1. The gains available for this function are (–).01, (–).1, 1, 10, and 100. Gain changes are achieved by switching in or out op amp sections.

If taking current readings, the circuit amplifies a signal coming in on the A/DMUX line which is a voltage representation of the current through the resistive shunt. The gains available for this function are 10 and 100.

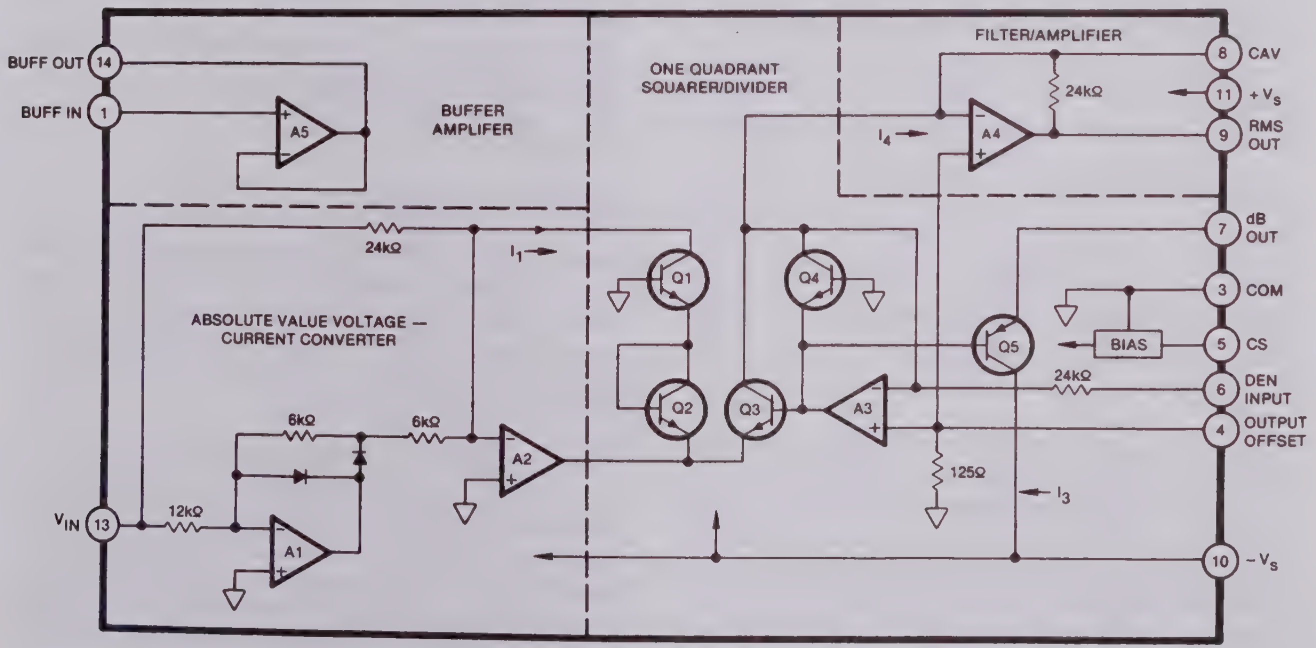

BUFF OUT
14
BUFF IN
1
A5
BUFFER AMPLIFER
ONE QUADRANT SQUARER/DIVIDER
FILTER/AMPLIFIER
8
CAV
24kΩ
11
+Vs
I4
A4
9
RMS OUT
24kΩ
I1
Q1
Q4
7
dB OUT
3
COM
ABSOLUTE VALUE VOLTAGE — CURRENT CONVERTER
Q5
BIAS
5
CS
24kΩ
6
DEN INPUT
6kΩ
6kΩ
Q2
Q3
A3
4
OUTPUT OFFSET
A2
125Ω
I3
VIN
13
12kΩ
A1
10
-Vs

Figure 5-19. AD637 Block Diagram

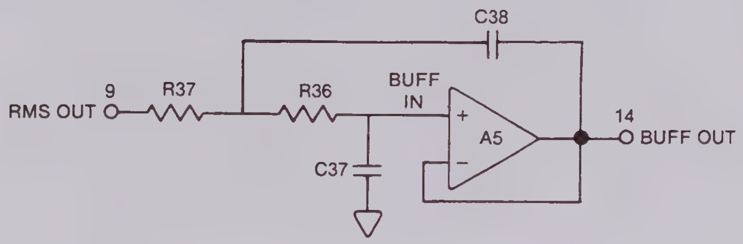


Figure 5-20. AD637 Two-Pole Filter

Whatever the gain, it should be such that the rms converter is presented with a signal level less than or equal to 3.2 volts rms. This is because the A/D CONVERTER (sheet 1, zone C2) is scaled so that 3.2 volts dc is its maximum input.

The AC CONVERTER section can block the dc component of an incoming signal — by C2 and C35. To pass dc, relay K4 (3D8) shorts around C2, and analog switch U18A (3D3) closes around C35.

Table 5-7 shows the gains provided by the sections of U15 on the various ac voltage ranges.

Table 5-7. AC CONVERTER Gain Switching

Voltage Range	U15D	U15C	U15B	U15A	Total Gain
30mVac	X1	X10	X10	X1	X100
300mVac	X1	X10	Bypassed	X1	X10
3Vac	X1	Bypassed	Bypassed	X1	X1
30Vac	÷100	X10	Bypassed	X1	X.1
300Vac	÷100	Bypassed	Bypassed	X1	X.01

U15A, one section of the MC34085 quad op amp, provides the rms converter with a fairly low source impedance throughout the passband. It is configured as a X1 ("times one") buffer amplifier: the feedback path from U15A-1 to U15A-2 through R29 is not divided down with respect to ground. The capacitors around U15A are to tailor a flat frequency response consistent with stability.

U15C has a fixed gain of 10. (1 + R27/R28). This stage is used on the 30mV, 300mV, and 30V ranges. Analog switch U17A is closed (GAIND high and ACAMPS low); U18C is closed (GAIND high and GAINC low); U18B is open (GAIND high); and U17D and U18D are open (GAINC low).

U15B provides an added gain of 10. (1 + R34/R35). It is switched in in series with U15C on the 30 mV range. U18C is opened and U17D and U18D are closed. To cause this, GAIND is high and GAINC is high. GAIND can be thought of as the (X10 or X100) control line. GAINC can be thought of as the X100 control line.

If GAIND is low, gain stages U15C and U15B are totally bypassed, resulting in a "gain" of X1. U18B closes; U17A, U17D, U18C, and U18D are open. U17C also closes, grounding the input of U15C.

The 300 volt range is when U15C and U15B are bypassed. On the 30 volt range, U15D divides by −100, and U15C provides a gain of 10. GAIND is low. This closes U18B. U14C-10 high opens U17A. U14B-4 high opens U18D. U14D high opens U18C.

U15D at ÷100

U15D can be configured either for a gain of +1, or a gain of −.01. For a gain of −.01 (division by −100), relay K5 is down. This allows the + input of U15D to be at ground potential through R21 and R22. U15D-13 (the — input) now becomes a virtual ground. The input signal goes through R23 to the (−) input of the op amp. The gain is set by −R26/R23, or −.01. Software keeps track of the polarity of the U15D gain.

The MC34085 op amp isn't stable at a gain of 1 (it oscillates). So U15D, like U15A, has a capacitive-resistive network between its inputs to reduce the feedback loop gain slightly. Recall from basic op amp theory that reducing feedback loop gain by a factor of two does not measurably affect the gain accuracy of the circuit, since the open loop gain started out at "infinite".

U15D at X1

For U15D to have a gain of +1, the pole of K5 is "up" (on the schematic). This turns U15D into a positive-input buffer. Minus capacitors, the circuit is redrawn in figure 5-21.

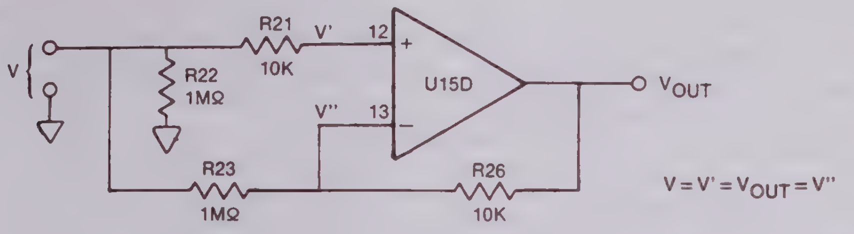


Figure 5-21. U15D At X1 Gain.

An input signal of amplitude V goes through R21 to the high impedance of the pin 12 input. Since there is negligible current draw through R21, the voltage at pin 12 is also V. Pin 13 is no longer a virtual ground as in the previous case. It follows pin 12, with current provided through R26.

The pin 13 voltage is virtually identical to the voltage V at the input of the circuit. With no voltage across R23, there is no current through it, and it is as if it were no longer physically in the circuit. It may be helpful to the reader to remove it mentally.

Current Measurements

Note that there is a maximum gain of 100 available after the input of U15C. The preceeding discussion considered only volts for the sake of clarity. In the case of "current", which comes in at A/DMUX (from location 1C5), switching is just slightly modified: both U18B and U17A are open at the same time. The source for U15C is now the A/DMUX line; U17B is closed. The ACAMPS line is high, forcing this.

Volts Vs. Current

The parameter, volts or amps, that U15C and U15B are to multiply is selected by whether U17A or U17B is closed. When ACAMPS ("AC AMPereS") is high, the A/DMUX input to U17B is enabled, and the volts input at U17A is disabled.

Table 5-8 summarizes the switching of U15C and U15B for the volts and current ranges.

Table 5-8. U15C and U15B Gain Switching

Volts Range	AC Amps Range	U17C, U18B	U17A	U18C	U17D, U18D	U17B	GAIND	GAINC	Total Gain
30mV		open	closed	open	closed	open	1	1	X100
300mV		open	closed	closed	open	open	1	0	X10
3V		closed	open	open	open	open	0	0	bypass (X1)
30V		open	closed	closed	open	open	1	0	X.1
300V		closed	open	open	open	open	0	0	X.01
	30mA	open	open	open	closed	closed	1	1	X100
	300mA	open	open	closed	open	closed	1	0	X10
	3A	open	open	open	closed	closed	1	1	X100
	10A	open	open	closed	open	closed	1	0	X10

5.3.2.5 Programmable Schmitt Trigger

What It Does

Accurate time interval, pulse width, frequency, and period measurements require that the signal being measured be separated from any noise riding on it. A slow-moving input signal with noise riding on it could cause digital circuitry to count multiple transitions when there is only one. The Programmable Schmitt Trigger takes in a signal with an unknown rise and fall time and possibly noise riding on it, and puts out clean logic-level states of high and low having very fast rise and fall times. The rise and fall times are fast enough so that there is no possibility of race conditions in the digital circuitry that follows.

The output changes state when the input passes through specified amplitude set points. The set points are programmed by software. The amplitude of the Schmitt Trigger input signal should be normalized. That is, the signal amplitude should be attenuated or amplified so that the input to the Schmitt Trigger is within its range. See figure 5-22, showing a signal level with a average value below the lower threshold, and whose noise peaks are insufficient to switch the upper threshold.

The Schmitt Trigger output (U27B-6) switches high when the input signal passes through the upper setpoint, or threshold, in a positive-going direction. The output won't switch low until the input signal passes through the lower threshold, in a negative-going direction. The two thresholds are separated by a "deadband" where no change occurs. So noise riding on the signal cannot cause a false change of state on the output. (This assumes that the peak noise amplitude is less than the distance from the real signal level to the opposite threshold.)

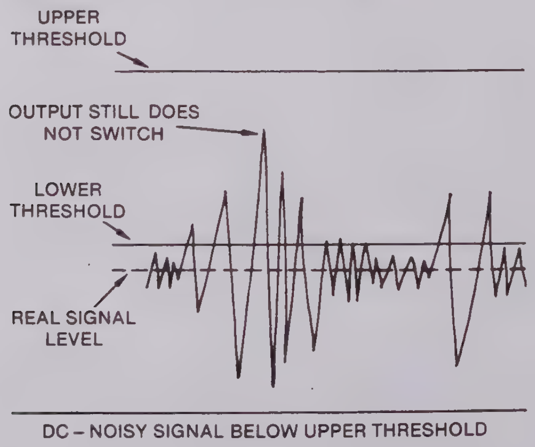

UPPER THRESHOLD
OUTPUT STILL DOES NOT SWITCH
LOWER THRESHOLD
REAL SIGNAL LEVEL
DC – NOISY SIGNAL BELOW UPPER THRESHOLD

Figure 5-22. Schmitt Trigger Noise Immunity

Refer to the measurement module schematic, sheet 3. Recall that the AC Converter section can pass dc if so programmed. The Schmitt Trigger selects one of four levels for a lower threshold, and one of another four levels for an upper threshold. The Trigger provides set thresholds for TTL, 5-volt CMOS, and 12-volt CMOS.

By changing the gain ahead of the Schmitt Trigger, and whether the AC Converter is ac or dc-coupled, the effective threshold levels can be changed.

For TTL the effective thresholds (external to the unit) are 0.8 volts and 2.0 volts. For 5-volt CMOS the effective thresholds are 1.5 volts and 3.5 volts. For 12-volt CMOS the effective thresholds are 4.0 volts and 8.0 volts.

How It Works

U19 is a dual (ganged) one-of-four analog switch. Depending on the state of the THRESHA and THRESHB lines, two of the eight inputs from the resistive divider string are switched to the outputs (U19 pins 3 and 13). U19A-3 is the upper threshold level and U19B-13 is the lower threshold level. The upper threshold level goes to the (+) input (pin 4) of upper comparator U21A. Any input signal to U21A-5 that rises above the threshold on pin 4 will cause the comparator pin 12 to switch low.

This low to U27B-5 will cause U27B-6 to go high if it isn't already high. Since U27B and U27C are connected as a latch, if U27B-5 should go high again, that in itself won't cause a low on U27B-6. (U27B and U27C are connected as a set-reset flip-flop which changes state only when one input goes low for the first time since the other input went high.)

The lower threshold from U19B goes to U21B-10. If the signal input to comparator U21B-9 should go below the threshold on pin 10, it will cause the comparator pin 7 to go low. This low to U27C-10 will force U27C-8 high. (Since the signal input can't be in two places at one time — below the lower threshold *and* above the upper threshold, it's a very safe bet that U27B-5 is high.) When U27C-8 goes high, it enables U27B for the next time the input signal rises above the upper threshold.

U27B-6 provides an output that goes high when the input signal rises above the upper threshold, and goes low when the input signal goes below the lower threshold. It's complement, U27B-8, provides an output that goes low when the input signal rises above the upper threshold, and goes high when the input signal goes below the lower threshold.

5.3.2.6 Prescaler and Frequency Divider Circuitry

U33, the 4020, is a fourteen-stage divider with selected outputs. The Q1 output (pin 9) is one-half the input frequency on pin 10. The outputs change state on the falling edge of pin 10. This is equivalent to the rising edge of the Schmitt Trigger input signal. The next output used in the circuit (Q5) is four stages down from Q1 so its frequency is 1/16 of Q1. This makes its frequency 1/32 of pin 10. The Q8 output has a frequency 1/256 of the input, and the Q11 output has a frequency 1/2048 of the input. Q14 has a frequency 1/16384 of the input.

The Q1 output goes to U32A, the 4013 D-flip-flop. It is connected as a divide by two. This makes U32A-1, its output, ¼ the frequency of U33-10. The output of U32A changes state on the rising edge of the pin 3 clock input.

If FOUTC is high, U32A-1 is forced low.

U31, an HC151, is an eight-input multiplexer. Depending on the state of the FOUTA, FOUTB, and FOUTC lines, it selects one of the inputs D0-D7, complements it, and puts the result on pin 6. Note that the undivided Schmitt Trigger outputs are routed to U31. D0 gets the "divide by one" signal, and D1 gets its complement. These undivided inputs are used in pulse width or time measurements.

Note that the control line $\overline{\text{FEN}}$ must be low to enable the HC151 and get anything out at pin 6. The inactive state of U31-6 is a high. FOUT goes to an input of U20B on sheet 2. On sheet 2, zone D5, FOUT is enabled to go to U22, and from there to the motherboard.

5.3.2.7 A/D Gain

Refer to sheet 1 of the measurement module schematic. The A/D GAIN stage, U5, provides the programmable dc gain function. U5 is connected as a noninverting amplifier. See figure 5-23. The gain from U5-3 to U5-6 is given by 1 + Ra/Rb.

RN3 is a monolithic resistor network. Between pins 1 and 2 it has 45Kohms of resistance. Pins 2 to 3 are 4.5Kohms, and pins 3 to 4 are 0.5 Kohms. U6B is a one-of-four analog switch. Depending on the state of the GAINA and GAINB lines, it selects a tap of RN3 to feed back to U5-2. This puts a different division ratio in U5's feedback loop. Table 5-9 shows the division ratios for the three selectable gains of 1, 10, and 100.

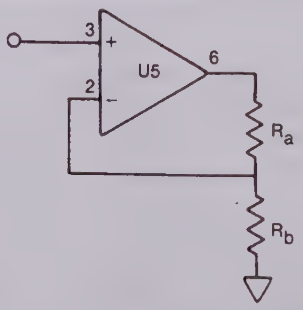


Figure 5-23. U5 Gain Configuration

Table 5-9. U5 Gain Derivation

	X1	X10	X100
Ra	Bypassed	45K	45K + 4.5K
Rb	Bypassed	4.5K + 0.5K	0.5K
Ra/Rb Ratio	N/A	9	99

For a gain of 1, the resistor network is bypassed and U5-6 is fed back directly to U5-2 (via U6B pin 12 to 13), making it a buffer. C9 reduces noise on any gain.

The dc gain function uses the GAINB and GAINA combinations of [0,0], [0,1], and [1,0]. For a gain of 1, GAINB and GAINA are 0,0. For a gain of 10, GAINB and GAINA are 0,1 respectively. For a gain of 100, GAINB and GAINA are 1,0 respectively. A combination of 1,1 selects the Y3 input on U6A, (ACOUT) — the ac input to U6A. In this case, the output of U5 is tied back to the negative input through U6B pin 11 to prevent an open-loop condition.

U5 is set to a gain of 1 during ohms measurements on the 3kΩ and higher ranges. On the 300Ω range, gain is X10. On the 30Ω range, gain is X100.

C7 is for noise filtering. It is a polypropylene type to prevent errors from dielectric absorbtion.

5.3.2.8 A/D Input MUX

Refer to sheet 1 of the measurement module schematic. (It may be helpful to refer back to the Measurement Module Circuit Overview at this point.) The A/D Mux circuit consists of R6, RN2, U7B, R65, and K4. It can be broken down into five major functions:

- Selection of either straight through (X1) or divide by 100 when in Volts dc mode.
- Routing Ohms signals or raw thermocouple signals straight through to U5.
- Selecting which current input on the front panel, J3 or J4, a current measurement will be taken from.
- If that current-signal is dc, routing it to U5. If the current is ac, routing it to the ac section on the A/DMUX line.
- Routing of the CJTEMP signal to U5 when required by a themocouple measurement.

U7B is a one-of-four analog switch. It's selection control lines are shown twice: at 4D4, and 1C5, of the measurement module schematic. The two control lines that control U7B (or U7A) are $\overline{\text{OHMS}}$ and $\overline{\text{OHMSA}}$. These two control lines can serve two purposes, since when an Ohms measurement (sheet 4) is being done, U7B is not used. ($\overline{\text{A/DINA}}$ = $\overline{\text{OHMS}}$, and $\overline{\text{A/DINB}}$ = $\overline{\text{OHMSA}}$.)

When not doing an Ohms measurement, a relay (K2 on sheet 4) disconnects the Precision Current Source from the J1 input terminal.

X1 or ÷100

In the Volts mode, a ratio of X1 or X.01 must be selectable ahead of U5. For X1, K4 is up and K5 is to the left. The input signal from J1 flows through R6 and K4 directly to U5. For division by 100, K5 switches to the right (pin 9 connected to 13), and K4 is down. The $\overline{\text{A/DINA}}$ and $\overline{\text{A/DINB}}$ lines are 1,1 (both high). The signal path is through K5, the RN2 100-to-1 divider, in U7B at Y3, and up through R65 and K4 to U5-3.

Ohms, Diode Test, or Thermocouple Signals

In the Ohms or Diode Test modes, the signal always takes the X1 path to U5. This is also true when measuring thermocouples. (The small thermocouple signal would never need to be divided by 100.) In the Ohms mode, the sensed voltage signal is "normalized", or adjusted in amplitude, by the current source having been set to an appropriate current.

Current

Current is measured by routing the external current through shunt resistors in the Model 52. J4, the high current input, has a 0.01 ohm shunt. J3, the low current input, has a 1.00 ohm shunt. The voltage signals developed across these shunts are called the A-IN and MA-IN signals, respectively. These are the two "current" inputs to U7B, at Y1, and Y0.

To select the low current shunt, J3, the control lines $\overline{\text{A/DINA}}$ and $\overline{\text{A/DINB}}$ would be set to 0,0. This selects the Y0 input of U7B. To select the high current shunt, J4, the $\overline{\text{A/DINA}}$ and $\overline{\text{A/DINB}}$ control lines would be set to 0,1, respectively. This selects the Y1 input of U7B.

DC

The output of U7B is available at U7B-13. To measure dc, the signal path is up through R65 and K4, to U5-3.

The Model 52 has four dc current-measuring ranges. The dc ranges and the corresponding states of the $\overline{\text{OHMS}}$ ($\overline{\text{A/DINA}}$), $\overline{\text{OHMSA}}$ ($\overline{\text{A/DINB}}$), GAINA, and GAINB control lines are given in table 5-10.

AC

In the case of an ac measurement, the signal is again available at U7B-13, but the signal goes to the AC Converter (sheet 3) on the A/D MUX line. The gain after this point is described in the AC Converter circuit description section. Remember that in this case, U6, (the input switch for the A/D Converter), would select the ACOUT line as its input.

Thermocouples

Thermocouples can be directly connected to the front panel inputs, J1-J2. They may also connect "to" the rear panel inputs (J101-J201) via multiplexers 50-20, 53-1, or 53-2 which have on-board cold junction sensors. One common output from a multiplexer feeds J101-J201. Thermocouple linearization information is stored in the motherboard ROM.

Electronic Cold Junction Compensation

When thermocouple leads are directly connected to the input of an amplifier, additional thermocouples are created at the thermocouple wires-to-copper (of the amplifier) junctions. See figure 5-24.

Table 5-10. Control Line States for Measuring DC Current

Terminals Used	Current Range	Max Shunt Voltage Developed	$\overline{\text{A/DINA}}$ $\overline{\text{OHMS}}$	$\overline{\text{A/DINB}}$ $\overline{\text{OHMSA}}$	GAINB	GAINA	Required U5 Gain
J3-J2	30 mA	30 mV	0	0	1	0	X100
J3-J2	300 mA	300 mV	0	0	0	1	X10
J4-J3	3 A	30 mV	0	1	1	0	X100
J4-J3	10 A	100 mV	0	1	0	1	X10

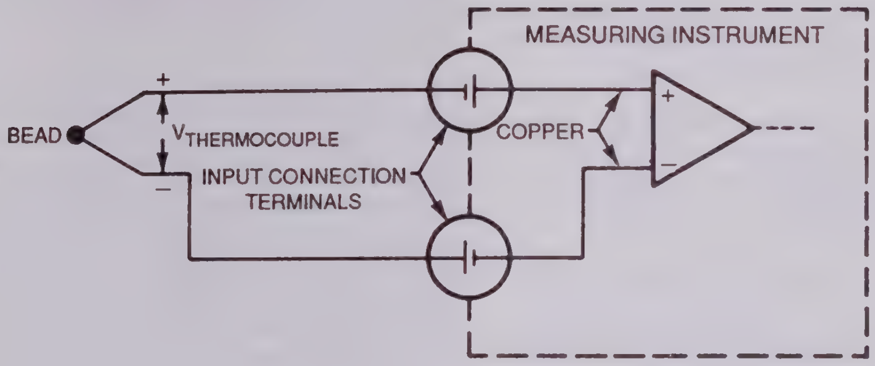


Figure 5-24. Thermocouple Wires-to-Copper Thermocouples

These thermocouple junctions generate small emf's that vary with the ambient temperature. This would cause an error, since the only thermocouple that is desired to be measured is the junction at the pickup end of the two thermocouple wires. The two thermocouples at the input terminals of the instrument are often lumped together and called the "cold junction". (The "cold junction" term comes from the early practice of keeping these two terminals at 0°C, in order to use one set of standardized thermocouple tables.)

Fortunately, the thermocouple voltages created at the input of the Model 52 are known functions — the voltages versus temperature that these junctions put out have been measured and tabulated. This information is stored in the Model 52 ROM. By measuring the ambient temperature, and knowing the thermocouple type, the would-be error voltages due to the input connections can be subtracted out by the Model 52's microprocessor. This is called electronic cold junction compensation. Sometimes it is done by analog circuitry — the Model 52 does it digitally.

On sheet 1 of the measurement module schematic, there is a device which puts out a voltage that corresponds to the ambient temperature. This device is U1, the LM35. It puts out a linear +10 mV for each degree Centigrade. For example, at +3.0 degrees Centigrade its output is +30.0 mV; at +70.0 degrees Centigrade its output is +700.0 mV. At room temperature (about 21.0 degrees Centigrade), the output is +210.0 mV.

The signal from U1, called CJTEMP, goes through R12 to U7's Y2 input. To get a cold-junction reading, the microprocessor sets the $\overline{\text{A/DINA}}$ and $\overline{\text{A/DINB}}$ lines to 1,0 respectively, and K4 is switched down.

U1 is thermally bonded to the front panel J2 in order to give a very accurate reading of the cold-junction temperature at J1-J2. In the single channel DMM mode, or a channel list using the front panel input, the Model 52 takes a cold-junction reading every 20 seconds.

Thermocouples may not be connected directly to the rear panel inputs, as no means of sensing rear panel input jack temperature is provided. In a situation where there are one or more external multiplexers, the thermocouple signal first comes onto copper in a totally different chassis from the Model 52. So, each external multiplexer (option 50-20, 53-1, or 53-2) has its own LM35 cold-junction temperature sensor.

In the case of an external multiplexer, the cold-junction ambient temperature information comes into the Model 52 on the same bus as thermocouples — via J101-J102. The external MUX is commanded to put the cold-junction information on its output when the Model 52 makes J6-7 on the rear panel MUX connector a logic high.

Unlike front panel temperature measurements, for rear panel thermocouple measurements to be read, they must have a cold-junction (on the multiplexer) reading *specified* as part of the CHANNEL LIST.

5.3.2.9 Precision Current Source

The precision current source provides a constant current for the ohms, high megohms, diode check, and continuity test functions. The output voltage of the current source is made to be whatever is required to generate the proper current through the unknown resistance or diode. The resulting voltage drop across the resistor, diode, or circuit under test becomes an input for the dc voltage measuring parts of the measurement module.

The constant current is directly settable by the user to five different levels, 0.1 uA to 1 mA, for the diode test function. Selecting a resistance range from 30Ω to 30MΩ indirectly selects one of the five currents.

The high megohms ranges (300 MΩ, 3000 MΩ) use only the 0.1 uA current level. This is sourced partly through an internal 10 MΩ resistor (RN2, sheet 1), switched in parallel with the external unknown high megohms value.

Continuity tests are based on 10% of a resistance range and so use the normal current for the particular resistance range. This is summarized in table 5-11, Constant Currents Generated, by Function.

Table 5-11. Constant Currents Generated, By Function

	Range			
Iout	**Ohms**	**High Mohms**	**Continuity**	**Diode Check**
1 mA	30 Ω		30 Ω	1 mA
1 mA	300 Ω		300 Ω	
1 mA	3 KΩ		3 KΩ	
100 uA	30 KΩ		30 KΩ	100 uA
10 uA	300 KΩ		300 KΩ	10 uA
1 uA	3 MΩ		3 MΩ	1 uA
.1 uA	30 MΩ		30 MΩ	.1 uA
.1 uA		300 MΩ	300 MΩ	
.1 uA		3000 MΩ	3000 MΩ	

Refer to sheet 4 of drawing number 0103-00-1811. Four control lines set the amount of output current from the precision current source. The four lines are $\overline{\text{OHMS}}$, $\overline{\text{OHMSA}}$, $\overline{\text{OHMSB}}$, AND $\overline{\text{OHMSC}}$. Another input to the circuit is VREF, which comes from the VR1 bandgap reference on sheet 1. VREF is +2.5 volts.

U4A multiplies the VREF input by four, based on the resistor ratios in RN1. Three reference voltages are derived from the U4A output and RN1 resistor string: +10.0, +5.5, and +5.0 volts dc. Since the U4A inputs are at +2.5 volts, the pin 1 output of U4A will be (2.5 volts)(1 + 75K/25K), or 10.0 volts. The 5.5 volts is produced by (10 volts)(55K/100K) = 5.5 volts. The 5.0 volts is produced by (10 volts)(50K/100K) = 5.0 volts.

U3 uses the 5.0 volts as a reference to its pin 3. U3 will control the output current through K2 so that 5.0 volts is also maintained at its pin 2 input. The output current from U3's pin 2 node must equal the node's input current, if the node is not to change voltage. The node's output current goes through Q1, R7, CR1, K2, and then out the unit via front panel banana jack J1. The U3 pin 2 node input current comes from U4B pin 7, via one of the "ports" on U2B.

See figure 5-25.

In figure 5-25, the scheme for generating U3-2 node input current has been redrawn for the purpose of explanation. An equal amount of current feeds out of this node to an external resistor under test. (How U3 regulates the output current will be explained later.) In figure 5-25, $I_{out} = I_{in}$ at pin 2. The I_{in} currents come through one of three resistors. Which resistor (5K, 50K, or 5M) supplies the current, depends on which one has a voltage impressed on it by U2B. U2B is an analog switch, connecting pin 13 to only one of its outputs (pin 12, 14, 15, or 11) at a time. How much current the resistor selected passes, is a function of how much voltage is impressed on it. The source of the voltage is U4B pin 7.

U4B can put out one of two voltages: +10.0 volts, or +5.5 volts. 10.0, 5.5, or 0.0 volts is switched to U4B-5 by U7A. U4B always operates as a X1 buffer. So the voltage on the right side of one of the resistors in figure 5-25 is either 10 volts, 5.5 volts, or no connection. No connection is made to the resistors from U2B's pin 13 input if no output current is wanted.

For an output current of **1mA**, U4B's input and output are 10.0 volts, and the ten volts is switched to the 5K resistor by U2B. U3 pin 2 is at 5 volts, since U3 pin 3 is. So the current through the 5K resistor is

(10V-5V)/5K = 1mA.

For an output current of **100ua**, U4B-7 is still 10 volts, but now this is switched to the 50K resistor by U2B. The current through the 50K resistor is

(10V-5V)/50K = 100uA.

For an output current of **10ua**, U4B-7 is 5.5 volts, and this is switched to the 50K resistor. So the current through the resistor is

(5.5V-5.0V)/50K = 10uA.

For an output current of **1uA**, U4B-7 is 10 volts, and this is switched to the 5M resistor. So the output current is

(10V-5V)/5M = 1uA.

For an output current of **100nA**, U4B-7 is 5.5 volts, and this is switched to the 5M resistor. So the output current is

(5.5V-5.0V)/5M = 0.1uA.

Since U2B has some resistance on whatever internal switching path is on, the current flowing through U2B would cause a voltage drop across U2B. And then, the current-setting resistors above would not get quite the ideal voltage. This would be the source of an error. To

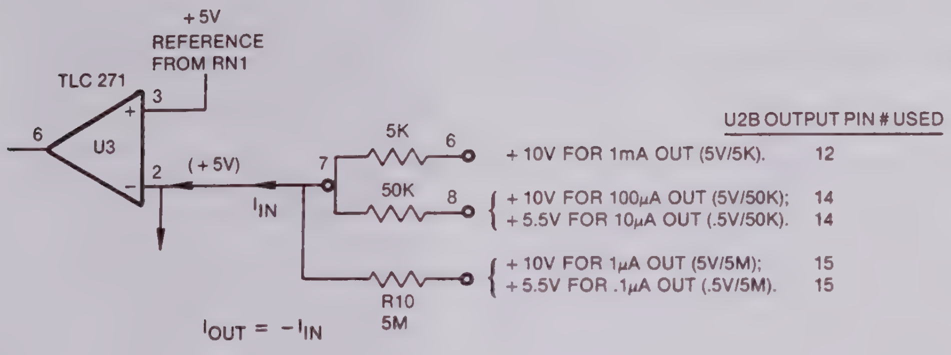

+5V
REFERENCE
FROM RN1
TLC 271
3
+
6
U3
2
−
(+5V)
IIN
7
5K
6
50K
8
R10
5M
IOUT = −IIN
U2B OUTPUT PIN # USED
+10V FOR 1mA OUT (5V/5K). 12
+10V FOR 100μA OUT (5V/50K); 14
+5.5V FOR 10μA OUT (.5V/50K). 14
+10V FOR 1μA OUT (5V/5M); 15
+5.5V FOR .1μA OUT (.5V/5M). 15

Figure 5-25. Setting U3-2 Input Currents/Simplified Feedback Loop

prevent this error, U4B's minus input is not taken from U2B-13, but from the actual inputs of the resistors. This allows U4B to boost its output voltage slightly to compensate for the voltage drop through U2B. This also requires that the minus input of U4B be switchable to the appropriate resistor on each range. U2A does this.

Now that the U3-2 node input current is determined, how does op amp U3 control the output current? See figure 5-26.

Recall that the job of the current source is to provide whatever output voltage is required to produce the correct current through the unknown resistance or diode. Since the current node (U3-2) voltage is 5.0 volts, almost 5 volts is available across the load to do this.

Q1 is a P-channel enhancement mode FET. With no voltage bias between its gate (G) and source (S), it is off. That is, its channel resistance from source to drain (D) is virtually infinite. As the gate is taken negative with respect to the source, the drain-source channel begins to lower in resistance. At a bias of about −2 to −3 volts on the gate with respect to the source, the device is fully on (for our purposes). Since Q1's source is always at 5.0 volts (assuming the external resistance is not overrange), this means the fully-on voltage on the gate is about 2 to 3 volts dc.

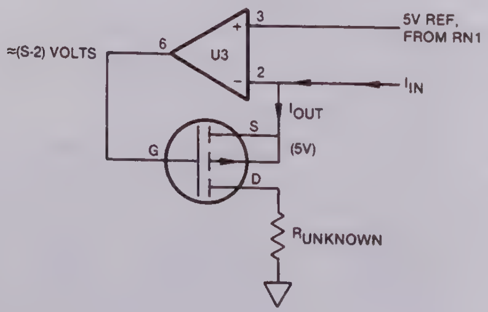


Figure 5-26. Making the I_{out} go Through $R_{unknown}$

The job of U3 is to provide a bias voltage such that **Q1's channel resistance plus the resistance of the load lets the proper amount of I_{out} flow**. How does U3 "know" if the proper amount of I_{out} current is flowing? Well, if I_{out} does not exactly equal I_{in}, the voltage at U3-2 will go up or down. If the voltage at begins to go up, this represents too little output current flowing (I_{out} is less than I_{in}). With U3-2 above 5 volts, the op amp will compensate by lowering the voltage on pin 6. This will turn on Q1 more, raising the output current back to the proper level.

If the voltage at U3-2 should begin to go down, this means too much current is being let out (I_{out} is greater than I_{in}). When the U3-2 voltage begins to go below 5.0 volts, U3-6 will go up. This will tend to turn off Q1, thereby reducing the output current.

The "settling point" will be when I_{out} exactly equals I_{in}.

When an external resistance is too high for the current selected, the voltage it drops will be above 3.2 volts, and the unit will display OVRRNG (overrange). At an even higher resistance, U3-2 will also rise above

5.0 volts, as U3 loses regulation of the output current. The output open circuit voltage may be up to approximately 9.4 volts. But in no case can the output current exceed the amounts set forth in table 5-11.

5.3.2.10 Input Terminal Arrangements; Grounds

Front Panel Vs. Rear Panel

See the poles of K1 at D7 and B6 on sheet one. K1 is set or reset by pulses from U9 (2C7).

Voltage type, ohms, and thermocouple signals come into the instrument by either J1 and J2 (front panel), or J101 and J102 (rear panel). K1 functions as the front/rear panel switch. If in a measurement setup (DMM or channel list), a channel number (1 through 4) was specified, and with no other numbers after the number, the unit knows front panel is meant. In this case, K1-11 (front panel Hi input) would be switched to K1-13, and K1-6 (front panel Lo input) switched to K1-4 (ground). The relay is in the reset position.

The measurement module ground is isolated from actual earth ground, so it can follow the input signal on the Lo terminal.

If a two-digit subchannel number (could be zero's) follows the measurement module channel number, the unit knows that the rear panel is meant. For example, 1_{00} would cause K1-9 (rear panel Hi input) to be switched to K1-13, and K1-8 (rear panel Lo input) switched to K1-4. The relay is set.

Grounds

See zone B6 on sheet 1. This zone shows K2-4, "mecca", where the four types of grounds come together. The ground sign with the circle around it represents the current source ground (sheet 4). The solid dark ground represents the ground of the ac amplifier and RMS converter (sheet 3). The ground with a **1** beside it represents analog ground. The last ground, with no modifiers, is the high-level-signal or digital ground.

Ohms

When resistance is being measured, the K2 relay is set. K2-13 connects to K2-9 (4A7), and K2-8 connects J2 to K2-4.

Volts Ground Vs. Current Ground

Current measurements are done using either front panel J3 or J4 as the input high. The end of R3 marked mA-Lo (4B2) is the electrical (not physical) low for the shunt resistor voltage outputs. mA-Lo is the ground reference for the amplifiers that follow. During a current measurement, K1-6 is not connected to K1-4. This forces ground 1 to be referenced only to mA-Lo. Note that the rear panel low, (J201), although unnecessary, is connected into the mA-Lo.

5.4 MEASUREMENT CONTROL

5.4.1 Introduction

Section 5.4 explains in detail how the motherboard controls the measurement modules and retrieves readings from them. Section 5.4 may be skipped by casual readers — however, familiarity with figure 5-27, Measurement Control is helpful. Readers who must troubleshoot the measurement module will normally use this section as the primary reference, referring to the appropriate supporting circuit-oriented paragraphs in section 5.3, as necessary. Both kinds of readers should be already familiar with paragraph 5.3.1, the analog overview.

The latter part of paragraph 5.4.1 contains an overview of the measurement control circuitry.

Paragraph 5.4.2 explains the format of the 3-line serial shifts from the motherboard to the measurement modules, and how a serial pattern is converted into parallel control bits for the analog circuitry.

Paragraph 5.4.3 explains the special case of the measurement module type test (50-1 vs. 50-2) that occurs during a power on routine.

Paragraph 5.4.4 explains how the value of a measurement is "formatted" and passed to the motherboard.

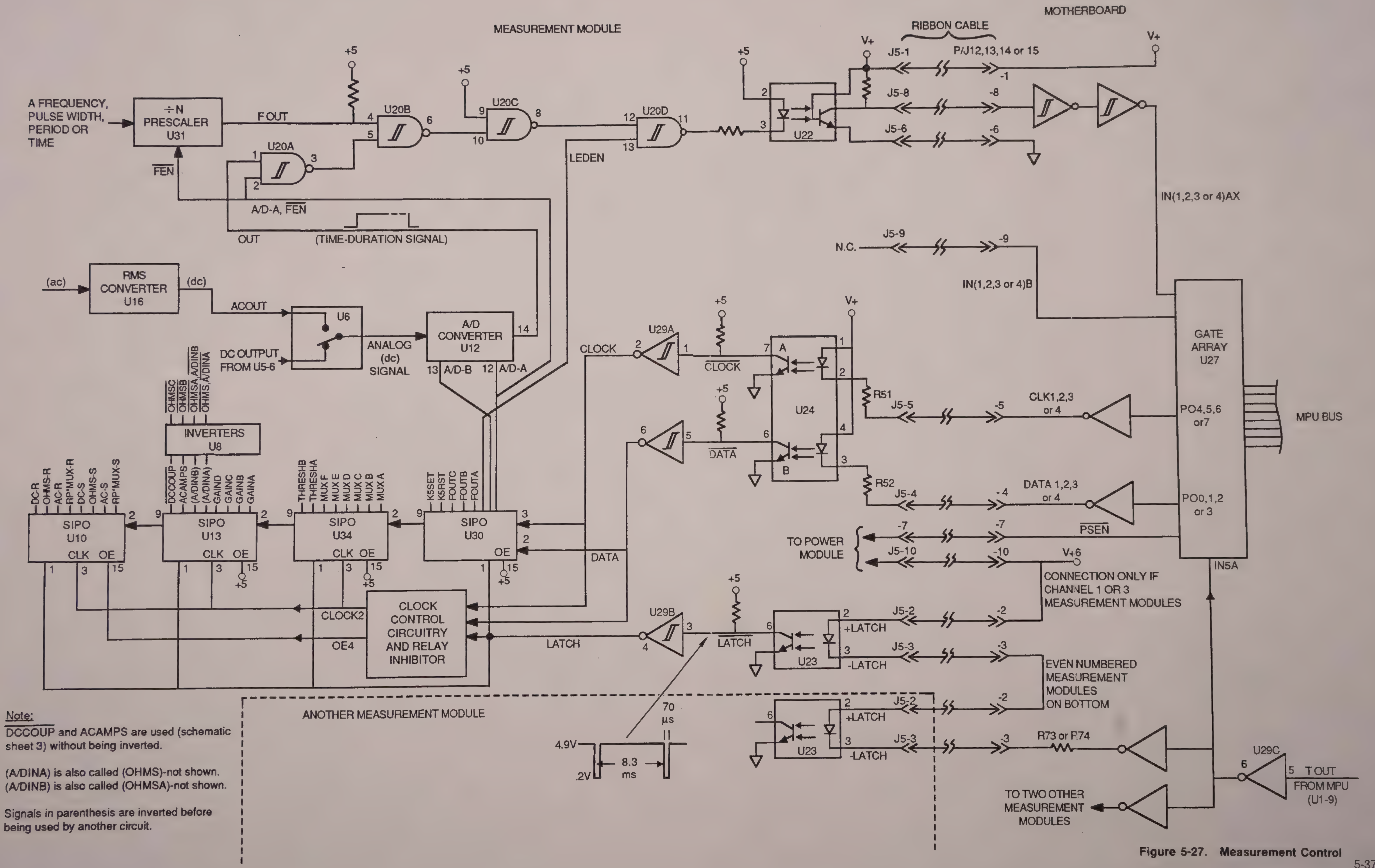
Paragraph 5.4.5 gives the parallel control bit patterns, by measurement function, on the output of the serial to parallel shift registers. Paragraph 5.4.5 also explains the overall effect upon the measurement module signal flow for each type of measurement function. (For a detailed explanation of the effect of a control bit upon a particular analog circuit stage, consult the appropriate circuit under paragraph 5.3.)

Control Circuitry Overview

Review paragraph 5.3.1, the overview of the measurement module circuits, if unfamiliar with it.

See figure 5-27, Measurement Control.

Figure 5-27 shows the digital circuitry on both the motherboard and a measurement module that is required to control a measurement module in the process of making a measurement. Compare this figure with figure 5-11 in paragraph 5.3.1.1, which summarizes the analog circuits of a measurement module. On the right side of figure 5-11 are two signals, FOUT and OUT. In the upper left area of figure 5-27 these two signals also


MEASUREMENT MODULE
MOTHERBOARD
RIBBON CABLE
A FREQUENCY, PULSE WIDTH, PERIOD OR TIME
÷N PRESCALER U31
FOUT
FEN
+5
U20B
U20C
U20D
U20A
LEDEN
A/D-A, FEN
OUT
(TIME-DURATION SIGNAL)
U22
V+
J5-1
P/J12,13,14 or 15
J5-8
J5-6
IN(1,2,3 or 4)AX
N.C.
J5-9
IN(1,2,3 or 4)B
(ac)
RMS CONVERTER U16
(dc)
ACOUT
U6
DC OUTPUT FROM U5-6
ANALOG (dc) SIGNAL
A/D CONVERTER U12
A/D-B
A/D-A
CLOCK
U29A
CLOCK
U24
R51
J5-5
CLK1,2,3 or 4
DATA
R52
J5-4
DATA 1,2,3 or 4
GATE ARRAY U27
PO4,5,6 or7
PO0,1,2 or 3
MPU BUS
PSEN
IN5A
TO POWER MODULE
J5-10
V+6
CONNECTION ONLY IF CHANNEL 1 OR 3 MEASUREMENT MODULES
OHMSC
OHMSB
OHMSA,A/DINB
OHMS,A/DINA
INVERTERS U8
DC-R
OHMS-R
AC-R
RP*MUX-R
DC-S
OHMS-S
AC-S
RP*MUX-S
DCCOUP
ACAMPS
(A/DINB)
(A/DINA)
GAIND
GAINC
GAINB
GAINA
THRESHB
THRESHA
MUX F
MUX E
MUX D
MUX C
MUX B
MUX A
K5SET
K5RST
FOUTC
FOUTB
FOUTA
SIPO U10
SIPO U13
SIPO U34
SIPO U30
CLK OE
DATA
CLOCK2
OE4
CLOCK CONTROL CIRCUITRY AND RELAY INHIBITOR
LATCH
U29B
LATCH
U23
+LATCH
-LATCH
J5-2
J5-3
EVEN NUMBERED MEASUREMENT MODULES ON BOTTOM
ANOTHER MEASUREMENT MODULE
4.9V
.2V
8.3 ms
70 µs
R73 or R74
U29C
T OUT FROM MPU (U1-9)
TO TWO OTHER MEASUREMENT MODULES

Note:

DCCOUP and ACAMPS are used (schematic sheet 3) without being inverted.

(A/DINA) is also called (OHMS)-not shown.
(A/DINB) is also called (OHMSA)-not shown.

Signals in parenthesis are inverted before being used by another circuit.

Figure 5-27. Measurement Control

appear. OUT is the point where an analog measurement value has turned from analog into digital.

FOUT is a frequency or time-duration signal. Like OUT, it is a clean, noiseless, digital signal.

One or the other signal, depending on the measurement function, is gated to the motherboard.

The **A/D** converter is used on the following **functions:**

Vdc
dBdc
CJTEMP
TEMP

OHMS
CONT
—▶|— CHK

Vac
Vac + dc
dB (ac)

Adc
Aac
Aac + dc

Wdc
VAac
VAac + dc

Counter functions (none of which use the A/D converter) are the following:

EVENTS
FREQ
PERIOD
TI
TI..1Shot
PW
PW..1Shot
LOGIC

Counter functions all use the SCHMITT TRIGGER, and the U31 selector IC.

5.4.2 MPU to Measurement Module Communications

5.4.2.1 U27 — The Parallel To Serial Converter

The U27 gate-array integrated circuit contains four channels of a 24-bit counter each, including extensive control circuitry. This high degree of integration minimizes the amount of SSI or MSI logic circuitry that is required between the 63B03 MPU and up to four measurement modules. (This is one of the keys to the Model 52's small size.)

Communication with the measurement modules is in serial format — so the gate array performs the parallel to serial, and serial to parallel format conversion for four channels. The gate-array also relieves the MPU of measuring time for counter type measurements such as frequency or period. The MPU must still feed setup data to the measurement modules, and control the timing of the measurement modules' A/D converters.

5.4.2.2 Three-line Serial Shift Format

See figure 5-27, and schematic numbers 0103-00-1808 (sheet 3) and 0103-00-1811 (sheet 2).

U27↔measurement module data is sent and received serially via opto-isolators. There is one common latch signal for all modules. It is sent out via pins 2 and 3 on J5. Data goes to a module via J5 pins 2 and 4. The input LED of the LATCH opto requires a current loop — one pin high AND the other simultaneously low. So one pin on J5 can do double duty. $\overline{\text{CLK}}$ goes to the modules via J5 pins 1 and 5. Note that U29E and U29D each drive two LED's in series. So if one of the two modules driven by one output is removed, a dummy LED must be plugged in to complete the loop. A module sends "data" to the motherboard using J5-8 for data and J5-6 for signal return.

DATA and CLOCK to a measurement channel come from port outputs of U27, the gate array. On U27, P00 through P03 are DATA outputs, one for each measurement module. P04 through P07 are CLOCK outputs, one for each measurement module. The latch signal to the measurement channels comes directly from the MPU (sheet 1), as TOUT, bypassing the gate array. DATA and CLOCK are simultaneously shifted to a measurement module. Later, at a precisely controlled time, the MPU sends out a latch pulse, which typically initiates a new phase of the A/D converter on one or more measurement modules. The latch pulse for the preceding shift is sent out just prior to the setup data being sent for the next shift. Recall that DATA and CLOCK can be sent, but do not appear at the parallel shift register outputs on a measurement module until the LATCH pulse is sent later. With this arrangement, software does not have to keep track of how long a particular shift takes — A/D timing is based upon the latch pulses.

5.4.2.3 How Three-line Serial Turns Into Parallel

5.4.2.3.1 Overview

The serial shift pattern from the motherboard to the measurement module may be 8 bits long, or 32 bits long. (A "32-bit" shift is 32 *data* bit times — there is actually an extra "data" and "clock" bit at the beginning, for formatting, making a total of 33.)

Recall from paragraph 5.3.1.2 and figure 5-13, that the clock to U34, U13, and U10 is inhibited if only an 8 bit shift is being done. An 8-bit shift updates the parallel output control bits of U30 only.

Figure 5-28 shows the two clusters (bursts) of a shift for a counter function, such as a frequency measurement: one 32 bit burst, followed by an 8 bit burst. The bottom trace in figure 5-28 is the $\overline{\text{CLOCK}}$ line on the measurement module, and the top trace is the $\overline{\text{LATCH}}$ pulse. The $\overline{\text{DATA}}$ signal (not shown) occurs at about the same times as the clock signal.

Most A/D functions, such as a Vdc measurement, have 8 clusters (bursts) in the shift making up the overall measurement cycle.

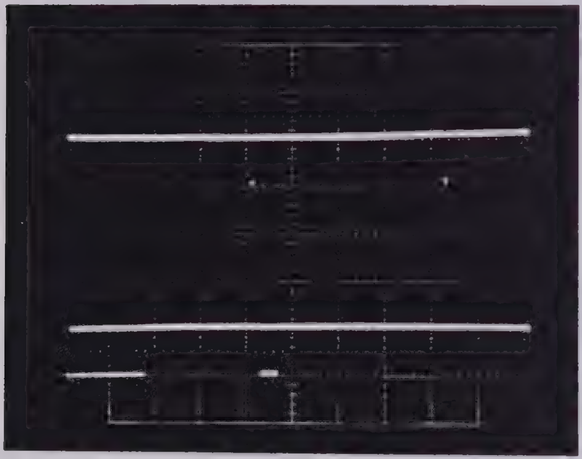


Figure 5-28. Counter Function Shift

5.4.2.3.2 8-bit Shifts

8-bit shifts are used on both A/D functions and counter type functions. On one A/D measurement cycle, several 8-bit shifts happen in the process of cycling the A/D converter through its states (reference paragraph 5.3.2.2).

For an 8-bit shift, flip flop **U32A** stays in the **reset** state. U32-1 is low, and U27D-13 is low, inhibiting the clock input on U27D-12. Since inverter U29E-10 puts out no clock pulses, the lower three shift registers (U10, U13, U34) don't clock in data.

The clock pulses from U29A-2 go to U30-3.

> *Each CLOCK pulse goes back low, before the next data bit sets up, such as a transition to a high level.*

Each time U30 receives a rising edge on its CLK input, the present bit data value shifts into the register. Approximately 6 milliseconds later, the LATCH pulse comes from U29B-4, to U30 pin 1. During the time of the active-high, about 70 microsecond-wide pulse at U30-1, the internal shift register bit values are transferred to, and latched at, the 8 parallel outputs.

Reminder: the clock control flip-flop (U32) is always held in the CLeaRed state by an 8-bit shift, since U32A-5 is always low anytime a (rising) edge at U32A-3 occurs.

Latch Pulses

Latch pulses occur one timing period after each timing interrupt that initiates the clock and data shifts. For example, the latch pulse for the second shift in a sequence of eight shifts occurs just before the data and clock are started for the third shift in the sequence.

For a counter function shift, the second latch pulse in a sequence does not immediately precede a clock and data shift.

See figure 5-29c. Figure 5-29c shows the 8 bit shift of clock and data for the second shift of a counter function. Note that there are 8 clock pulses. The shift registers and flip-flops respond to the ↑ edge of CLOCK. The rising edge of a CLOCK pulse is designed to be in the approximate middle of a data bit, so that there is no ambiguity.

Reading the photograph.

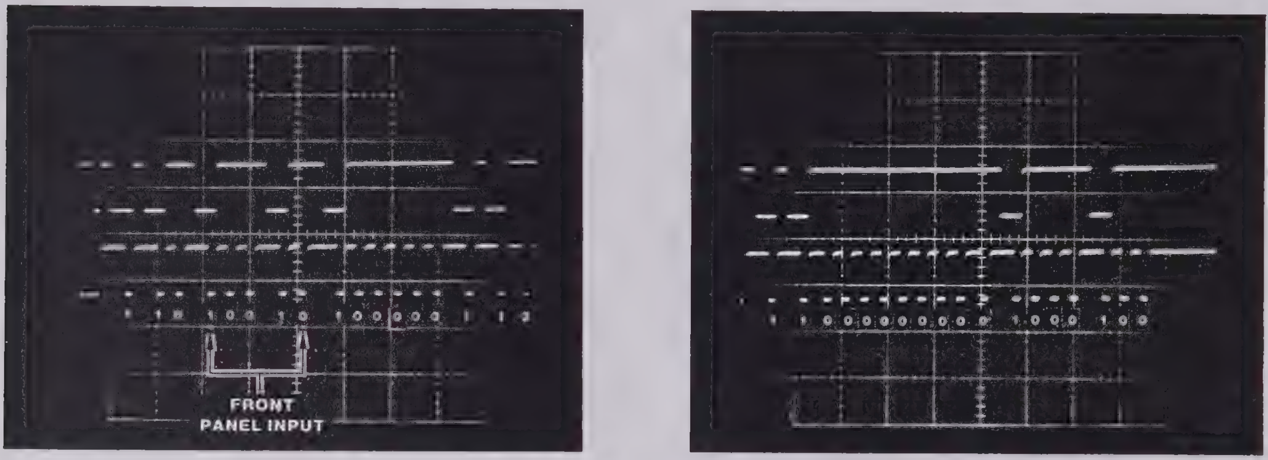
The rising edge of CLOCK would be the falling edge of a $\overline{\text{CLOCK}}$ pulse, in figure 5-29c. Also, when looking at $\overline{\text{DATA}}$ on the oscilloscope, the state of the $\overline{\text{DATA}}$ line during each falling edge of $\overline{\text{CLOCK}}$ must be mentally inverted to get the proper state of the data bit. Verify for yourself that the data content of the shift in the photograph is 0 0 0 0 0 1 0 0, with the right-most bit being the last in time. The left-most bit of the 8 bit shift would end up at U30-11, and the right-most bit would end up at U30-4. Not shown in the photo is the latch pulse.

5.4.2.3.3 "32-bit" Shifts

A 32-bit shift happens at least once before any measurement is made. Each time a different-type measurement is to be taken, a new complete shift, including a 32-bit shift, is sent. For DMM or channel list operation without a Program, and with no measurement delay, if the type measurement on that channel stays the same, the 32-bit serial shift is not repeated after the first time. (Exceptions to this are Wdc, VAac, and VAac + dc, which are compound functions.)

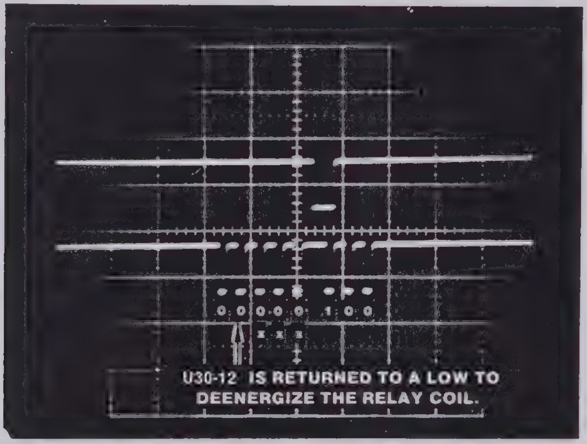
The Measurement Setup-data Transfer.

For a 32-bit shift, flip flop **U32A** is put into the **set** state. The special conditions that do this are the *first* CLOCK pulse not going back low before the data bit goes high.



a. First Half Of 32

b. Second Half Of 32



c. Second Cluster—8 bits

Figure 5-29. 32 And 8 Bit Shifts For FREQuency, Front Panel Input

Note that the CLOCK pulse goes to U32A-5, the D input. And, the DATA line also goes to U32A-3, the CLK input. While CLOCK at U32A-5 is high, the DATA line functions for one clock period as a clock line, and clocks the high at U32A-5 across to U32A-1.

With U32A-1, and thus U27D-13, high, the clocks on the input of U27D during the rest of the burst will feed across to U29E-10. These clocks go to pin 3 on each of the three lower shift registers, allowing them to shift in the data values on their DATA (pin 2) inputs. After a total of 33 clocks, the first data bit in the serial burst (started on clock number two) will have clocked all of the way through U30, U34, U13, and ended up at the Q8 position inside U10. Then, the LATCH pulse from U29B-4 occurs, latching the serial data into parallel form at the Q outputs of the shift registers.

Relay Inhibitor.

Any output bit from U10 that is high will cause a corresponding relay coil (reference paragraph 5.3.1.2) to be energized. This uses a significant amount of power, in terms of battery life. So, one software-interrupt timing period later (reference paragraph 5.2.8.5.2), the relay-controlling bits are turned back off, to save power.

This is done, not by sending another 32-bit pattern having lows for the relay bit positions, but by making

U10 tristate (high impedance) its parallel outputs. At the end of the next serial shift, the LATCH pulse clocks U28B into the CLeaR state (U28B-13 low). U28B-13 goes low, and inhibits U10 from sourcing any current from its parallel outputs. With no current into them, the darlington transistors in U9, and U8-1, will turn off, removing any current sinking from relay coils.

Note that U30, U34, and U13 all have their OE (Output Enable) pins always high. So, their internal data is always at the outputs, once latched.

How is U28B, the relay inhibitor, put into the relay-enabling (SET) state by a 32-bit shift? When the number two clock pulse of the 33 in a 32-bit shift occurs, it goes not only to the lower shift registers, but also to U28A-6. This causes U28A-1 to go high. This high goes to U28B-9... After the data shifting is complete, the U28B-9 high level gets clocked to U28B-13 when the LATCH pulse arrives at U28B-11. (The high also goes to U28A, clearing it. The next latch pulse at U28B-11 will find a low at U28B-9.)

In the case of a power on, U28B-10 comes up high. It stays high until C56 discharges after about 10 milliseconds. The high forces U28B into the CLeaR state, U28B-13 low. So, the relays (with the possible exception of K5) don't draw power before the first setup is sent to the measurement module.

Figure 5-30 shows $\overline{\text{DATA}}$ (top trace), and $\overline{\text{CLOCK}}$ bottom trace, for the 32 bit part of a FREQuency setup shift. 5-30a covers the first 16 bits, and 5-30b covers the last 16 bits of the cluster. In this case, the measurement module is being set up for a *back* panel signal input. You should be able to identify that the data pattern in 5-30a is

- 1 1 0 0 0 0 1 1 1 0 0 0 0 0 1 1

and that the data pattern in 5-30b is

1 1 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 .

The first two "1"s in figure 5-30b are the leftovers from figure 5-30a.

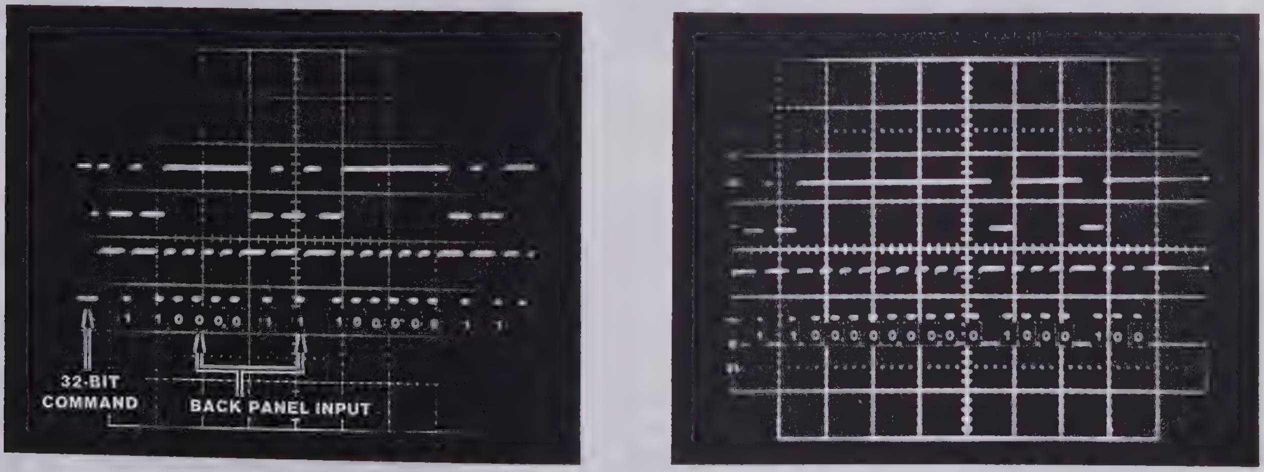
The 4th and the 8th bits in figure 5-30a are 0, 1, respectively. When latched, these two bits appear at U10-14 and U10-4. They control the state of K1, the front panel vs. rear panel relay. Compare these two bits with their state in figure 5-29a, which is for a front panel setup.

5.4.3 Module Type Checking During A Power-on

Recall that the power-up routine starts as soon as the MPU comes out of reset. The measurement module type checking (50-1 vs. 50-2) routine begins about 440 milliseconds after the start of the power-up routine. See figure 5-31a. After the module type checking, the motherboard turns off measurement module power if PWR SAVE is selected (UNIT STATUS menu).

During a segment of the power up routine, the software checks the state of the IN1A, IN2A, IN3A, and IN4A lines going to U27 on the motherboard (3C7). The INXA line on a channel connector comes from J5-8 on a measurement module. J5-8 is driven by U22-6, the output of the optoisolator.

As part of the power up routine, 8 shifts are sent to a measurement module.



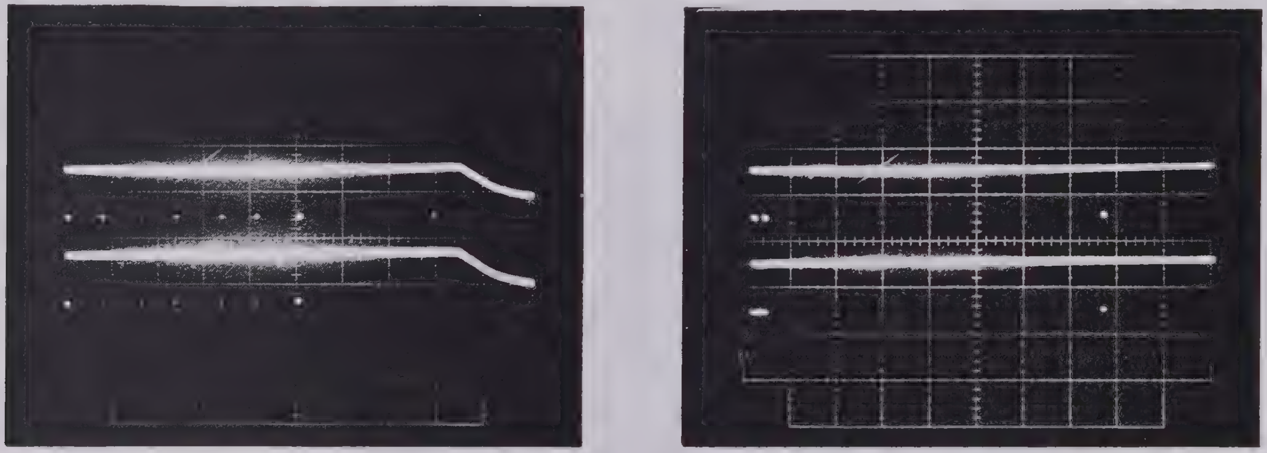
a. First Half Of 32

b. Second Half Of 32

Figure 5-30. 32 Bit Shift For FREQuency, Back Panel Input

Shift#																																
1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0
2																									0	1	1	1	1	1	0	0
3																									0	1	0	0	0	0	0	0
4																									0	1	0	0	0	1	0	0
5																									0	1	0	0	1	0	0	0
6																									0	1	0	0	1	1	0	0
7	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0
8																									0	0	1	1	1	0	1	0
				U10								**U13**								**U34**								**U30**				
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay:	4	2	3	1	4 S	2 S	3 S	1 S																	5 S	5						

Type Checking Patterns



Top Trace: $\overline{\text{DATA}}$ Bottom Trace: $\overline{\text{CLOCK}}$
Vert: 5V/Div. Horiz: 100ms/Div

a. Complete Type Checking routine

Horiz: 10 ms/Div.

b. First Two Bursts

Figure 5-31. Type Checking

Refer to measurement module schematic number 0103-00-1811, sheet 2 zone D, and sheet 3 column 1.

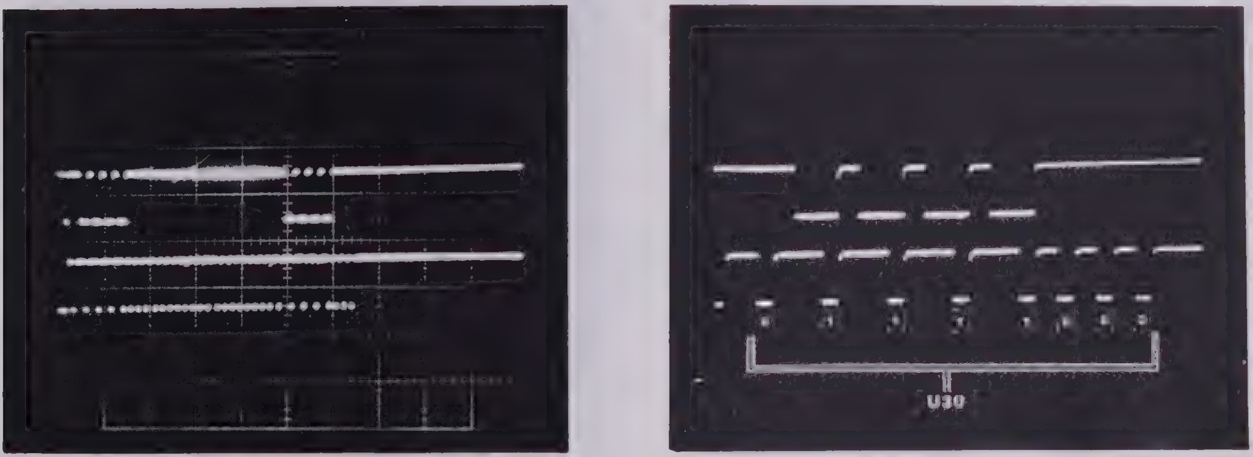
By varying some bits at the parallel outputs of U30, the software forces U22-6 to go low at times which depend of whether a 50-1, 50-2, or no measurement module, is plugged in.

The first shift is a 32 bit shift to initialize the states of U10, U13, U34, and U30. The LEDEN bit (LED ENable), U30-7, is low, ensuring that opto U22 is off (U22-6 high) regardless of the states of FOUT and OUT. (The corresponding level of the IN line for that channel, at gate array U27 on the motherboard, is a high.) See figures 5-31c, d, and e. A storage oscilloscope was used. Single sweep is used after the trigger level is adjusted. Delayed time base is also used.

See figures 5-31f, g, and h. The second shift, an 8 bit shift, sets LEDEN high, and keeps A/D-A, U30-4, low. A/D-A low, at U20A-2, forces U20B-5 to be high. If a 50-2, which has no PRESCALER, is installed on the channel, FOUT has nothing driving it, and is pulled up by R57 at the pin 4 input of U20B. If a 50-2, both inputs of U20B are high, U20C-10 is low, U20D-12 is high, and the LED in the opto is turned on by U20D-11 outputting a low. The photons from the opto LED cause the opto transistor to conduct, and U22-6 to go low.

So, at this point, the motherboard can determine if a 50-2 is installed. If a 50-2 is not installed, the following shifts are used to check for a 50-1.

The third shift, an 8 bit shift, turns off the LED enable bit, ensuring that the motherboard IN line goes high.

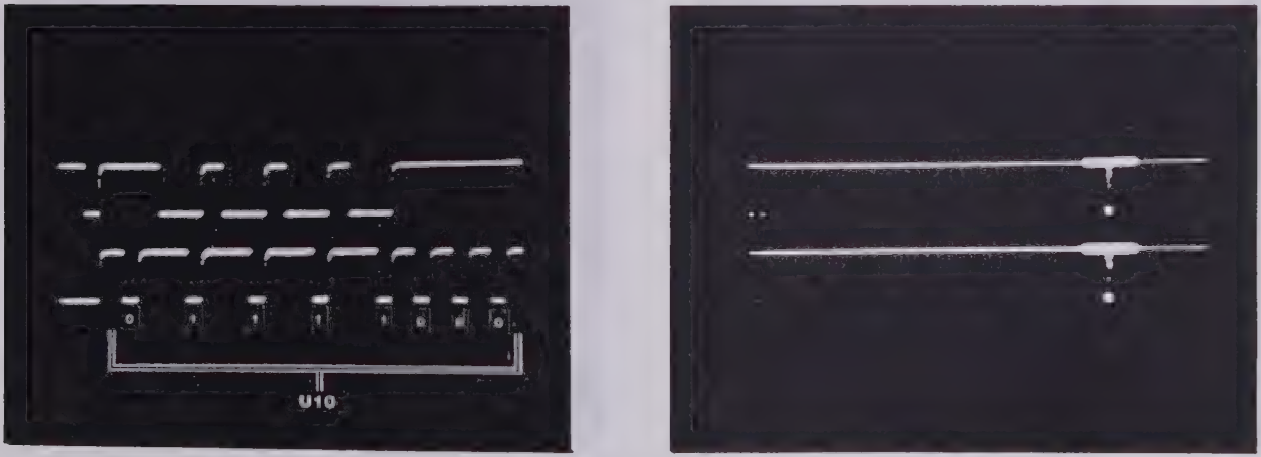


Horiz: 0.5 ms/Div.

c. First Burst

Horiz: 0.1 ms/Div. using X10 key

e. Last Part of First Burst



Horiz: 0.1 ms/Div.

d. First Part Of First Burst

Horiz: Main: 10 ms/Div.; delayed time
base: 1 ms/Div., "bug" at ≃ .75

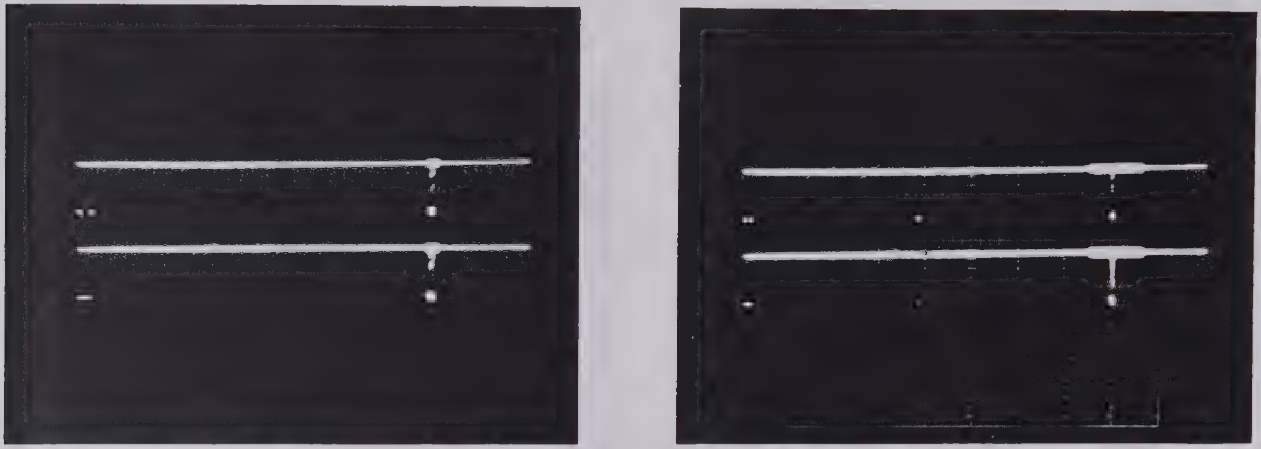
f. Burst #2 Intensified

Figure 5-31. Type Checking, continued

The fourth shift, an 8 bit shift, turns on the LED enable bit, and takes A/D-A, $\overline{FEN}$, low. This shift also selects the D0 input of U31 (3B1) by taking FOUTC, FOUTB, and FOUTA low. D0 (which is always the complement of D1 coming from the SCHMITT TRIGGER's flip-flop output) is routed to FOUT, and from there to the motherboard. This step alone can not tell with certainty that a 50-1 is installed, since the state of the SCHMITT TRIGGER can not be guaranteed. The motherboard firmware program notes the logic level on the IN line, on this step, and continues the routine.

The fifth shift, an 8 bit shift, turns off the LED enable bit (LEDEN low), ensuring that the motherboard IN line goes high.

The sixth shift, an 8 bit shift, turns on the LEDEN bit, and keeps A/D-A low. But this time, the FOUTC-FOUTB-FOUTA combination causes U31 to select its D1 input to be routed to FOUT. The state of the motherboard IN line will be *opposite in polarity* to what it was after the fourth shift, if a 50-1, with its PRESCALER, is installed.

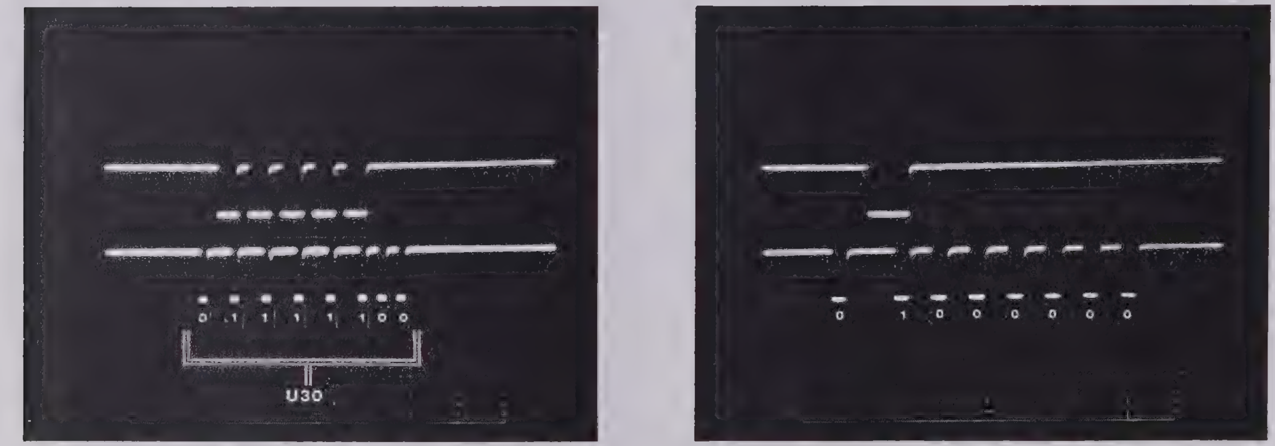


Main: 10 ms/Div; delayed time base: .2μs/Div., "bug" at ≃ .8

g. Burst #2 Intensified (intermediate setup)

Main: 20 ms/Div.; delayed time base: 2 ms/Div., "bug" at ≃ .74

i. Burst #3 Intensified



Horiz: .2 μs/Div.

h. Burst #2 Shown On Delayed Time Base

Horiz: Delayed time base: .1 ms/Div.

j. Burst #3

Figure 5-31. Type Checking, continued

The seventh shift, an 8 bit shift, turns off the LEDEN bit again, ensuring that the motherboard IN line is high.

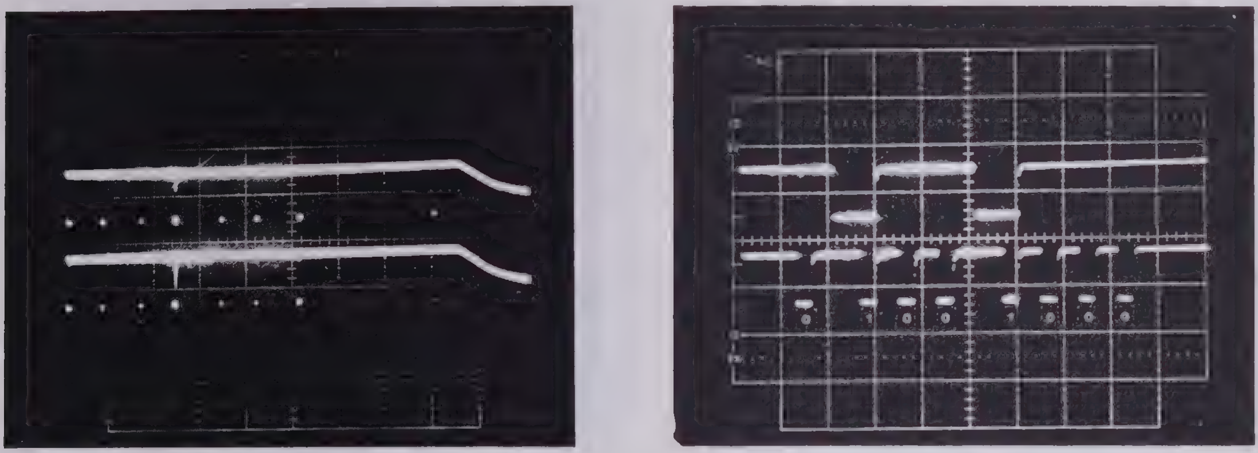
The eighth shift, a 32 bit shift, puts the A/D converter into the auto-zero mode, so that a large offset is not on the integrating capacitor prior to the start of an A/D measurement cycle, if and when it occurs. This is accomplished by setting A/D-B, U30-5, high and A/D-A, U30-4, low. LEDEN, U30-6, is low, disabling U22 from being driven.

If no measurement module is plugged into J12, J13, J14, J15, the corresponding IN line will be floating high all through the type test, and be sensed by the motherboard.

5.4.4 Sending Measurements To The Motherboard

5.4.4.1 Introduction

This section explains the time relationship between various control pattern shifts to the measurement mod-

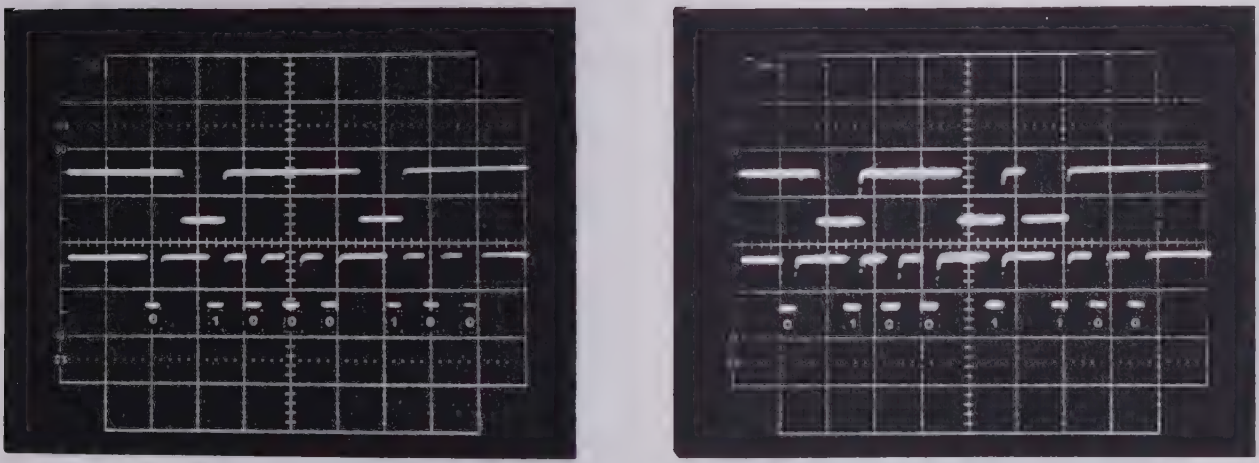


Main: 100 ms/Div.; delayed: 2 ms/Div.

k. Burst #4 Intensified

Main: 100 ms/Div.
Delayed: .1 ms/Div.

m. Burst #5



Main: 100 ms/Div.
Delayed: .1 ms/Div.

l. Burst #4

Main: 100 ms/Div.
Delayed: .1 ms/Div.

n. Burst #6

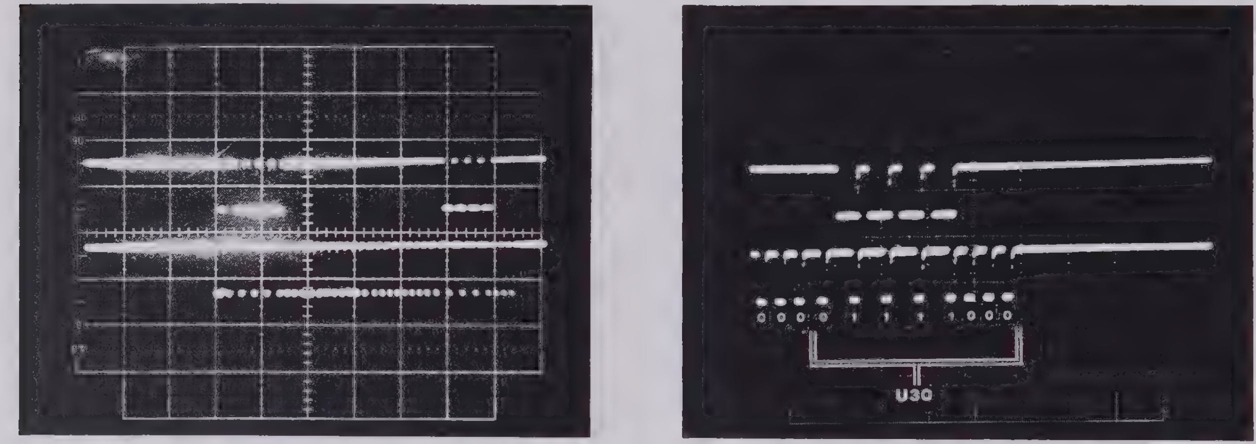
Figure 5-31. Type Checking, continued

ule, and when the U22 optoisolator sends a transition to the motherboard. This section assumes the reader has read preceding sections of paragraph 5.4, and paragraph 5.3.1.2. Also, if interested in one of the A/D measurement functions, the reader should be loosely acquainted with the A/D operation in paragraph 5.3.2.2.

See figure 5-27, measurement control.

There are two broad classes of measurements that a measurement module may do. In the first class, called **A/D functions,** the A/D CONVERTER is used to turn an analog signal amplitude into a time duration logic-level signal whose time duration is proportional to the analog amplitude. (Control patterns for this class are given in paragraphs 5.4.5.3 through 5.4.5.16.)

In the second class of measurements, called **counter functions,** a time-domain characteristic of the input signal is to be measured. The signal comes from the PRESCALER. (Control patterns for this class are given in paragraphs 5.4.5.17 through 5.4.5.18.)

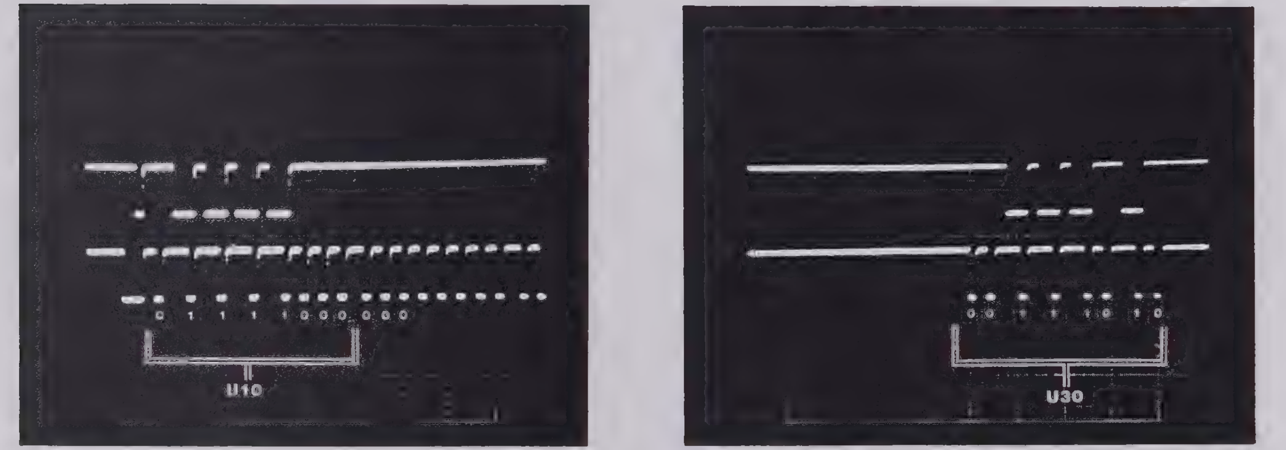


Main: 100ms/Div.
Delayed: .5 ms/Div.

o. Burst #7

Main: 100 ms/Div.
Delayed: .2 ms/Div.

q. Burst #7, last part (U30)



Main: 100 ms/Div.
Delayed: .2 ms/Div.

p. Burst #7, first part (U10)

Main: 100 ms/Div.
Delayed: .2 ms/Div.

r. Burst #8

Figure 5-31. Type Checking, continued

5.4.4.2 Review Of The Basics

Figure 5-27 shows three signals coming from the motherboard—$\overline{\text{CLOCK}}$, $\overline{\text{DATA}}$, and $\overline{\text{LATCH}}$. There is one signal (not named) going to the motherboard via U22. During a timed-interrupt software routine, the motherboard causes the MPU to send data to the gate array on the parallel MPU bus.

This data is converted into serial format, and sent to the measurement module via optoisolator U24, as serial shifts (bursts). For each shift (a sequence of DATA and CLOCK pulses), one timing period later the latch pulse for the shift is sent out on the TOUT line, directly by the MPU.

Upon receiving the latch pulse, the previously shifted data pattern appears at the parallel outputs of U10, U13, U34, and U30. The pattern controls signal routing in the module, gains, ranges, sensitivities, ac vs. dc coupling, front vs. back panel inputs, and, the phase of the A/D converter (if used on that type of measurement function).

5.4.4.3 A/D Functions

On the measurement functions that use the A/D CONVERTER, the measured value is not immediately passed to the motherboard as soon the control bits for the measurement setup arrive from the motherboard.

A/D functions all produce the time-duration signal called OUT, at U12-14. On A/D functions, the PRESCALER output is inhibited by $\overline{\text{FEN}}$ being high during the "time window" when the motherboard is looking for a transition (during the integrate and polarity-checking phase).

From the time of the latch pulse to the measurement module, commanding "start deintegration", the motherboard is looking for a low-going (↓) transition at J5-8. The duration of the time from the latch pulse, to the transition on J5-8, is proportional to the A/D input amplitude. FOUT is a solid high for an A/D converter function. A/D-A, and A/D-B must cycle to make the A/D converter (1C2) take a measurement. LEDEN stands for LED (in the optoisolator) ENable. LEDEN is high only during the polarity and deintegration phases of the A/D converter.

On an A/D function, when the MPU reads the contents of the gate array is not crucial. The reading resides as a latched number (of a time duration) in the gate array.

5.4.4.4 Vdc Example

The Initial Setup

Before actually taking the first measurement, the motherboard shifts over to the measurement module a 32-bit setup to set the function and range. It then shifts over a couple of ZI (A/D gross zero) command shifts. Then one AZ (A/D auto zero) command is shifted over. The A/D converter remains in the auto-zeroing state until the start of an actual measurement cycle is to begin.

See figure 5-32. 5-32 shows the integrator output pin (U12-1) of the A/D converter for a +3.0 volt input, and for a 0.75 volt input. Figure 5-32 also shows the latch pulses which "make official" the previously shifted data in a burst. 5-32a also shows, for a +0.75V input, the resulting states of the A/D-A and B control bits which put the converter into the different phases. Also shown is the resulting polarity/time-duration signal (U12-14) from the converter.

The Measurement Cycle

An A/D measurement cycle consists of eight shifts from the motherboard. An 8 bit shift signifying "start integration" is the first shift of a measurement cycle. During the integrate phase (paragraph 5.3.2.2), the second shift comes over, for enabling polarity checking of the input signal to the converter. Once it puts out the latch pulse for the second shift, the motherboard checks the polarity of the input signal by whether the OUT line (from U12-14) is high (input is +), or the OUT line is low (input is −). For reference, see table 5-6 in paragraph 5.3.2.2.

See figure 5-33, burst #2. When the second latch pulse is received, the same control bit pattern as from burst #1 is on the output of U30, with the exception of U30-6 which is now high (LEDEN).

(Figure 5-33 shows the states of the control bits within any one burst, relative to each other in time. Time moves "to the right", and the bits shift to the left, until at the end of the burst (shift), they are in the proper alignment with the parallel control bit positions they will become. Figure 5-33 does not show the relative time between each 8 or 32-bit burst in the whole measurement cycle. That is, each burst has been "stacked" vertically to show its ending position at the proper parallel control bit outputs.)

To complete the preset integration period, the third burst (8 bits) comes over, and its latch pulse puts the A/D converter into the deintegrate phase. During this phase, the A/D converter puts out the time-duration high level signal called OUT at U12-14, the duration of which is proportional to the input signal amplitude. The motherboard measures the time from when it sent the latch pulse, to when OUT goes low. In figure 5-32a, note that the time that OUT is high, between DEINTegrate, and OUT going low, is one-fourth the duration of the same parameter in figure 5-32b.

The rest of the bursts in the measurement cycle are for putting the A/D converter into gross-zero (ZI) and fine-zeroing (AZ) states. Note that the last burst in the sequence leaves the A/D converter in the autozero (AZ) state. This means that the first burst of the next measurement cycle can put the converter directly into the integrate phase. If there were any user-programmed measurement delay, it would come before the INTegrate for the next measurement cycle.

5.4.4.5 Counter Type Functions

For each serial burst (a cluster of DATA and CLOCK pulses), one timing period later the latch pulse for the burst is sent out on the TOUT line, directly by the MPU.

Upon receiving the latch pulse, the previously shifted data pattern appears at the parallel outputs of U10, U13, U34, and U30. The pattern controls signal routing in the module, gains, ranges, sensitivities, ac vs. dc coupling, and front vs. back panel inputs. The phase of the A/D converter (controlled by bits U30-6, -5 and -4) does not change.

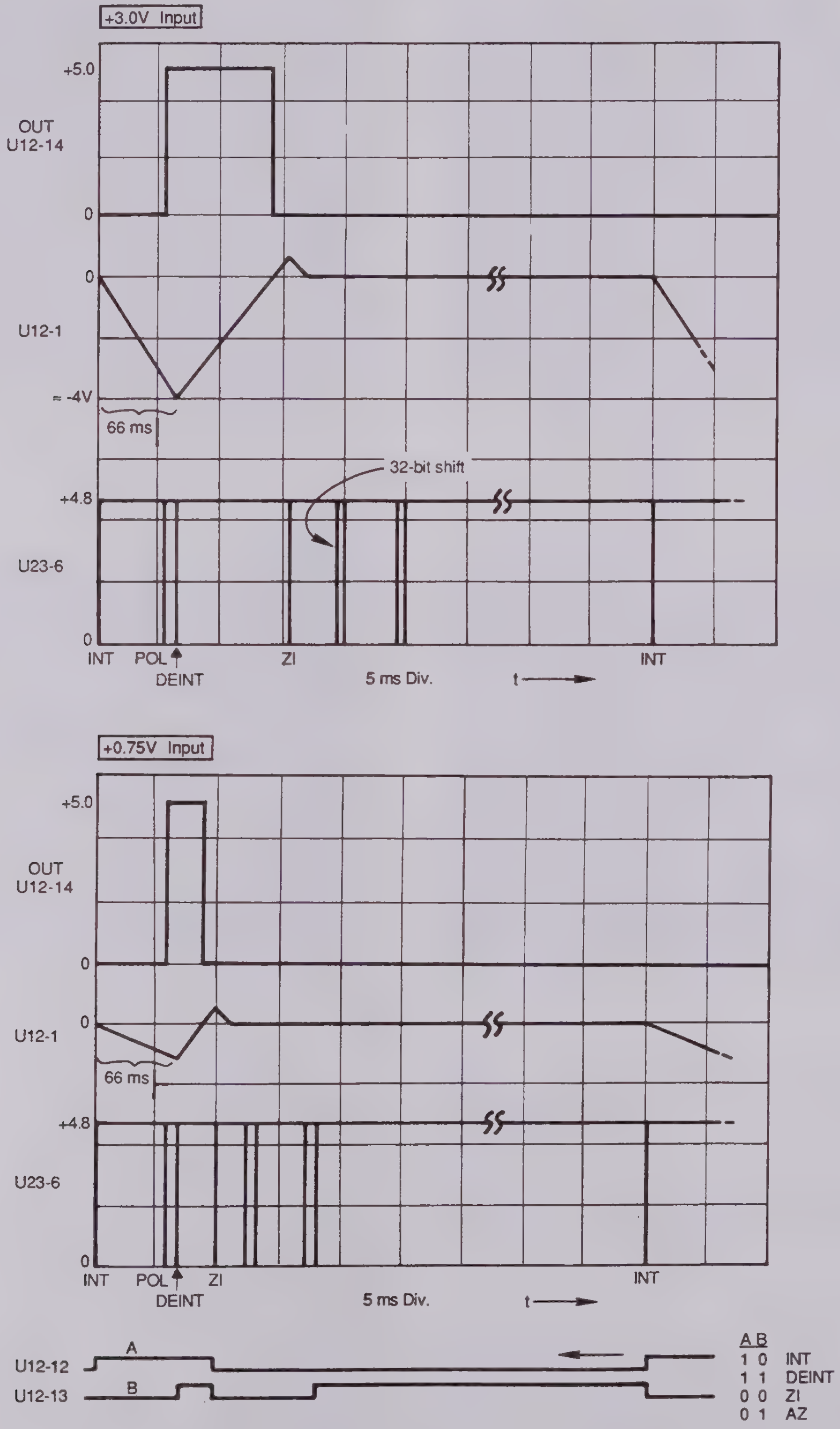

+3.0V Input
+5.0
OUT
U12-14
0
0
U12-1
≈ -4V
66 ms
32-bit shift
+4.8
U23-6
0
INT
POL
DEINT
ZI
5 ms Div.
INT
t
+0.75V Input
+5.0
OUT
U12-14
0
0
U12-1
66 ms
+4.8
U23-6
0
INT
POL
DEINT
ZI
5 ms Div.
INT
t
U12-12
A
U12-13
B
A B
1 0 INT
1 1 DEINT
0 0 ZI
0 1 AZ

Figure 5-32. The Timing Of The OUT Signal

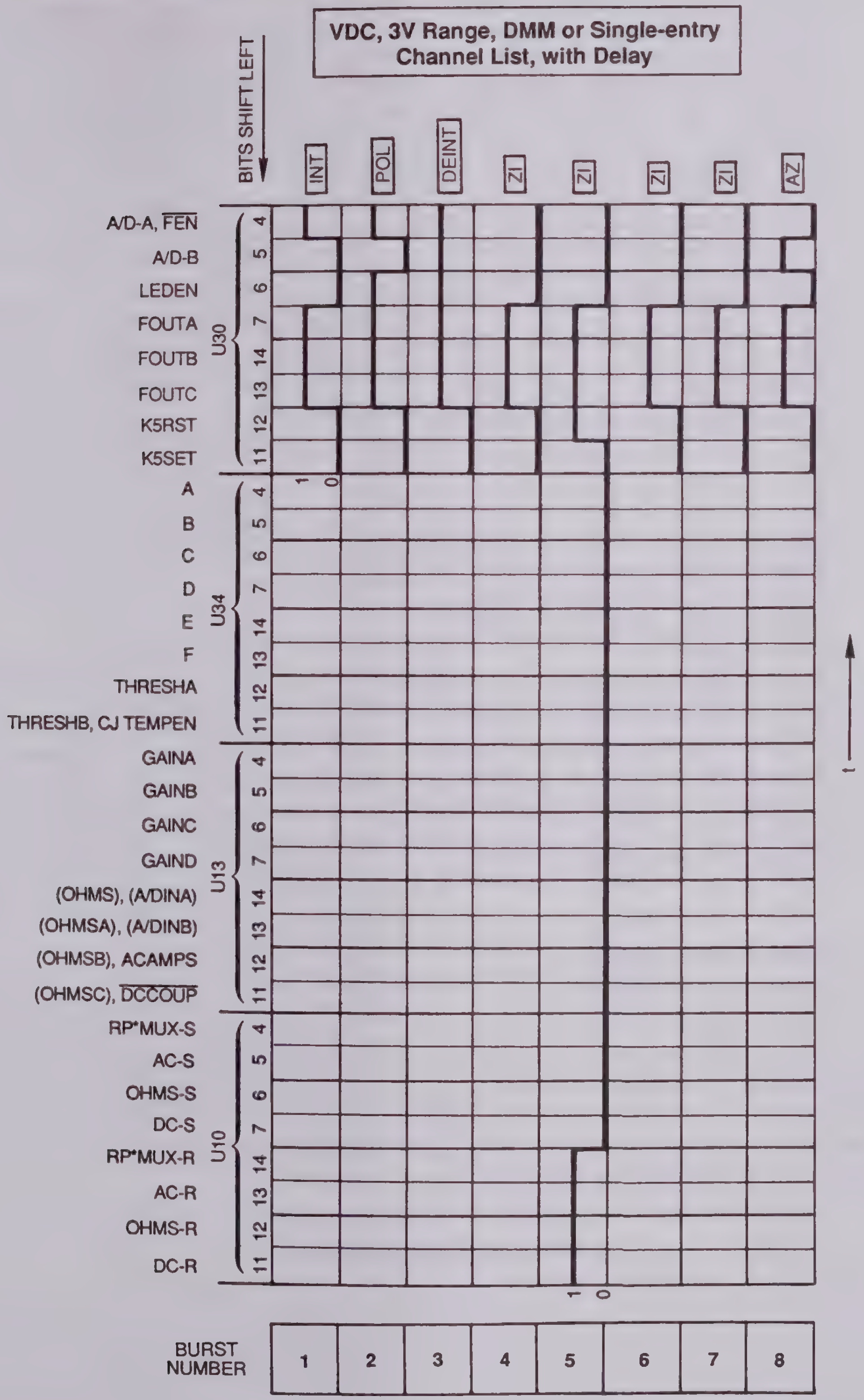

VDC, 3V Range, DMM or Single-entry Channel List, with Delay
BITS SHIFT LEFT
INT
POL
DEINT
ZI
ZI
ZI
ZI
AZ
A/D-A, $\overline{FEN}$
A/D-B
LEDEN
FOUTA
FOUTB
FOUTC
K5RST
K5SET
U30
4
5
6
7
14
13
12
11
A
B
C
D
E
F
THRESHA
THRESHB, CJ TEMPEN
U34
GAINA
GAINB
GAINC
GAIND
(OHMS), (A/DINA)
(OHMSA), (A/DINB)
(OHMSB), ACAMPS
(OHMSC), $\overline{DCCOUP}$
U13
RP*MUX-S
AC-S
OHMS-S
DC-S
RP*MUX-R
AC-R
OHMS-R
DC-R
U10
1
0
t
BURST NUMBER
1
2
3
4
5
6
7
8

Figure 5-33. The 8 Bursts For Vdc

As soon as the control bits for a counter function are shifted over, and become parallel, a frequency or time-duration signal from the prescaler, called FOUT, begins feeding to the motherboard. The FOUT signal continues feeding to the motherboard indefinitely — until either the measurement module power is turned off, or, the function is changed to one that does not use FOUT. Once a counter type measurement setup is passed to the measurement module, no further setup shifts will occur as long as there is no measurement delay, and as long as the type of measurement is not changed. The motherboard software defines the time period of a measurement cycle—there is no indication on the measurement module.

The gate array U27 on the motherboard, under control of the MPU, measures period, averaged period, pulse width, etc. (For frequency measurements, the period is measured — software converts to the equivalent frequency.)

On EVENTS measurements, the transitions pass undivided to the motherboard gate array. They are counted and stored there. Periodically, the MPU reads the gate array to get the latest count. For LOGIC measurements, the level is read.

On FREQuency or Pulse WidTH measurements, the period of the signal to the motherboard is long enough (in some cases having been divided down), that the motherboard gate array, by counting high frequency clocks (REFCLK), achieves good accuracy. A flag is set at the completion of each measurement time frame. Periodically the MPU polls the gate array and gets the "measurement".

5.4.5 The Measurement Control Patterns

5.4.5.1 How To Read The Control Patterns

Refer to sheet 2 of the measurement module schematic. Following are the setup shift patterns for the various measurement module functions, and their overall effect on the measurement module analog circuits.

There is a **general** control pattern for each Model 52 measurement function. Within a general measurement setup, a few bits are dependent upon the range, sensitivity, or, state of the A/D converter. Although there are 24 measurement functions, a particular general pattern may be used on more than one function, since many measurement functions use exactly the same measurement module circuit blocks (figure 5-11).

The general control bit pattern for most measurement functions will be specified individually, (paragraphs 5.4.5.3 through 5.4.5.18), for ease of reference.

The following hypothetical general pattern shows all possible variable bits, for purposes of explanation. Above each IC pin number, is a letter. Also, below some IC pin numbers, is the number of the associated relay.

There are two control bits associated with each latching relay. The S associated with a bit (for example, U10-7) means that the bit place is a "1" for one timing period, if the relay is Set. Conversely, if the S bit is never a 1, then the other bit associated with the relay is a 1 for one timing period, if the relay is reset.

Code

A	These bits control the routing of the signal to either the Ac, or the dc sections.
D	These bits control DC coupling if a counter-type measurement function, or Divide by 100, if an A/D-type measurement function.
d	These bits control divide by 100 in either the AC or DC circuits.
F	This bit is a 1 if Front panel input is specified.
B	This bit is a 1 if Back panel input is specified.
C	Controls whether the constant current source is internally Connected to the front panel and the "volts" input.
R	These bits set a constant current-generator Range, or A/D INPUT MUX signal Routing.
r	These bits set a Range on a counter function.
g	These bits control Gain in the AC section, which depends on the range or SENSITivity.
s	These bits also control SENSITivity, on counter functions.

Hypothetical General Pattern

	D	C	A	F	D	C	A	B
				U10				
Pin#	11	12	13	14	7	6	5	4
Relay:	4	2	3	1	4	2	3	1
					S	S	S	S

	R	R	R	R	g	g	G	G
				U13				
Pin#	11	12	13	14	7	6	5	4

	s	s	M	M	M	M	M	M
				U34				
Pin#	11	12	13	14	7	6	5	4

	d	d	r	r	r	E	P	P
				U30				
Pin#	11	12	13	14	7	6	5	4
Relay:	5	5						
	S							

G These bits set the Gain of the A/D GAIN circuit, which depends on the range.

M These bits control the Multiplexer subchannel selection.

E This bit Enables OUT to drive the LED in the U22 opto during a specific time in the A/D measurement cycle. It stays high during counter functions.

P These two bits control the Phase of the A/D converter.

S The relay associated with that bit place is Set, if there is a 1 in the bit place. Otherwise, the relay is reset.

5.4.5.2 Default Control Patterns By Function

The default 32-bit control pattern for each measurement function is given in table 5-12. The unit specifies some bits (default values) when the user does not specify range, sensitivity, etc. The default patterns for all functions are given together, so that the major differences between functions may be inspected. In troubleshooting, the default pattern is always tested first; then the range is changed, and just the bits for the changed range are checked.

Table 5-12 patterns are taken under the following conditions, unless noted: DMM mode, J1-J2 front panel input is shorted, and a measurement DELAY of 0.1 to 2.0 seconds. Specifying a measurement delay causes the control pattern to be repeatedly sent to the measurement module. The longer delays of 1 to 2 seconds are necessary, if using an oscilloscope, to prevent from randomly retracing. Scope sync is external, on the first clock of a measurement cycle. Use delayed time base on the scope to magnify a particular shift, on A/D functions. If interested in only the 32 bit shift, sync on the rising edge of U32-1, assuming 32-bit shifts are working.

A handheld logic probe does not need the longer measurement delays. Assuming the probe has a pulse-stretcher, it is not dependent on an involved syncing or delaying scheme to let you "see" the relay-driver "1"s. A logic probe is recommended, assuming 32-bit shifts are not inhibited by some malfunction.

Table 5-12

	U10**								U13								U34								U30							
	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Vdc	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
dBdc	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
CJ TEMP	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	E	P	P
TEMP	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
OHMS	1	0	1	1	0	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
CONT	1	0	1	1	0	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
▶| CHK	1	0	1	1	0	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
Vac	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
Vac+dc	0	1	0	1	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
dB	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
Adc	0	1	1	1	1	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
Aac	1	1	0	1	0	0	1	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
Aac+dc	0	1	0	1	1	0	1	0	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
* Wdc	0	1	1	1	1	0	0	0	0	0	0	1/0	0	0	1/0	0/1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
* VAac	1	1	0	1	0	0	1	0	1	1/0	0	1/0	1	1/0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
* VAac+dc	0	1	0	1	1	0	1	0	0	1/0	0	1/0	1	1/0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
EVENTS	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
FREQ	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
PERIOD	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
*** T-INT	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
T-INT. . 1-SHOT	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
P-WTH	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
P-WTH . 1SHOT	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
LOGIC	0	1	0	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

** All output bits on U10 shown as "1", hold the 1 for only one timing period (8.3 or 10.0 ms.). The same is true for U30-11 and U30-12.

* The DELAY modifier is not implemented on these functions.

*** T-INT, T-INT . .1SHOT, P-WTH, and P-WTH. . 1 SHOT should have TRIG (use Mods key) set to 2s.

Table 5-12. Measurement Module Default Control Patterns

Vdc

	U10								U13								U34								U30							
Default	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
General	D	1	1	F	D	0	0	B	0	0	0	0	0	0	G	G	0	0	M	M	M	M	M	M	d	d	1	1	1	E	P	P
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4	2	3	1	4 S	2 S	3 S	1 S																	5 S	5						

5.4.5.3 Vdc

U10, U13, and U34 are updated only from shift number 5.

Section 5.3 references: 5.3.2.2, 5.3.2.7, 5.3.2.8.

Default Pattern Explanation

(Refer to table 5-4, if desired.) K4 is RESET (U10-11 = 1). This means do not divide by 100, on schematic sheet 1. K2 is RESET, so the constant current source is not connected in. K3 is RESET, so the AC CONVERTER section power is turned off, and AC1 is connected directly to AC2. K1 is RESET, so the front panel terminals, J1 and J2, are selected. K5 is RESET, so there is no divide by 100.

U13-13 and U13-14 are both low, making A/DINA and A/DINB (1C5) high. U13-5 and U13-4 are both low, making GAINB and GAINA low (1C4), so U5 is at a gain of 1. (The default is the 3V range.)

THRESHA and THRESHB are low. The MUX CONTROL lines are low, their default state when the front panel terminals are selected.

U30-13, U30-14, and U30-7 are high, so U31-12 (3B1) is selected. U31-5 will therefore be low when $\overline{FEN}$ is low. And when $\overline{FEN}$ is high, this forces U31-5 low, regardless of the state of any inputs. So FOUT is always high, enabling the output of the A/D section at U20B-5 (2D5).

See paragraph 5.4.4.4 for the cycling of the E P P bits.

General Pattern Explanation

DC-R and DC-S reset or set relay K4. K4 is reset (U10-11 = 1) and K5 is reset (U30-12 = 1) on shift number 5 if the Range is 3V, 300mV, or 30mV. K1 is reset (U10-14 = 1) for a Front panel measurement, or set (U10-4 = 1) for a Back panel or multiplexer measurement.
U13-5 and U13-4, (A/DINA) and (A/DINB), set the gain of the DC amplifier U5 (schematic location 1D4).

Range	U10-11	U10-7	U30-11	U30-12	U13-5	U13-4
30mVdc	1	0	0	1	1	0
300mVdc	1	0	0	1	0	1
3Vdc	1	0	0	1	0	0
30Vdc	0	1	1	0	0	1
300Vdc	0	1	1	0	0	0

In the special case of Z=10MΩ, K5 is set, so the three lower ranges become:

Range	U10-11	U10-7	U30-11	U30-12	U13-5	U13-4
30mVdc	1	0	1	0	1	0
300mVdc	1	0	1	0	0	1
3Vdc	1	0	1	0	0	0

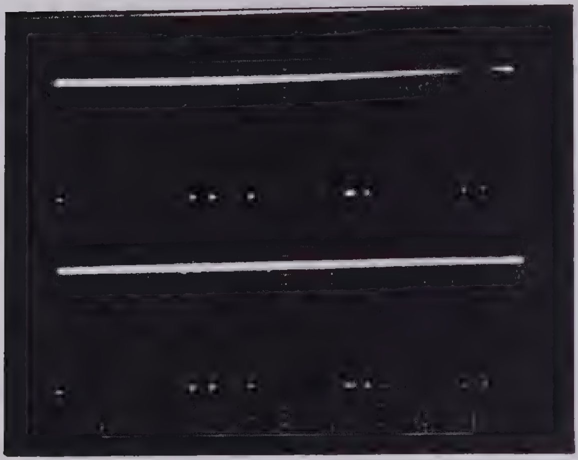
Three control bits on the parallel output of the SIPO's that cycle are LEDEN, A/D-A, and A/D-B. A/D-A, and A/D-B must cycle to make the A/D converter (1C2) take a measurement. LEDEN stands for LED (in optoisolator U22) ENable. LEDEN is high only during the polarity and deintegration phases of the A/D converter.

Before actually taking the first measurement, the motherboard shifts over to the measurement module a 32-bit setup to set the function and range. It then shifts over a couple of ZI (A/D gross zero) command shifts. Then one AZ (A/D auto zero) command is shifted over. The A/D converter remains in the auto-zeroing state until the start of an actual measurement cycle is to begin.

Vdc Measurement Cycle

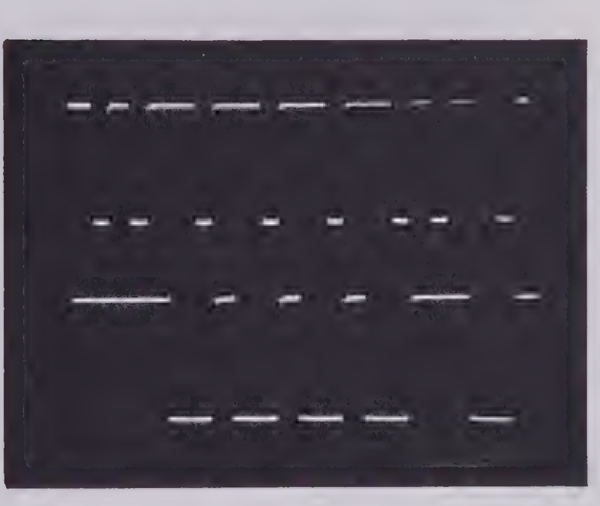
See figures 5-32 and 5-33. The format of all of the A/D measurement functions is basically the same. The deintegration times change, depending on the amplitude of the input signal.

1. An 8 bit shift signifying "start integration" is the first shift of the Vdc measurement cycle. A/D-A goes high, and A/D-B goes low.
2. During the integrate phase, the second shift, 8 bits, comes over, enabling polarity checking of the input



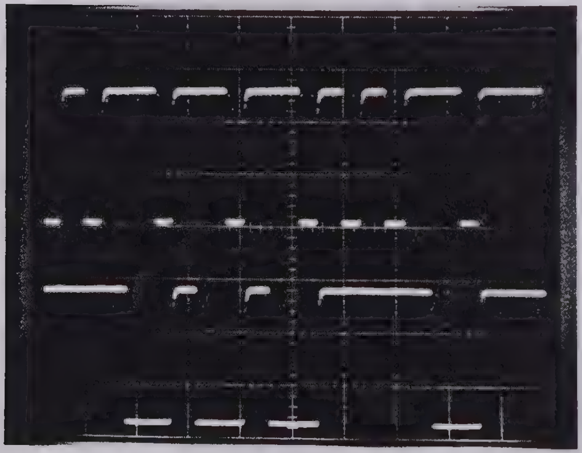
Horiz: Main: 20 ms/Div.

Figure 5-34. Vdc, 3V Range, All Bursts



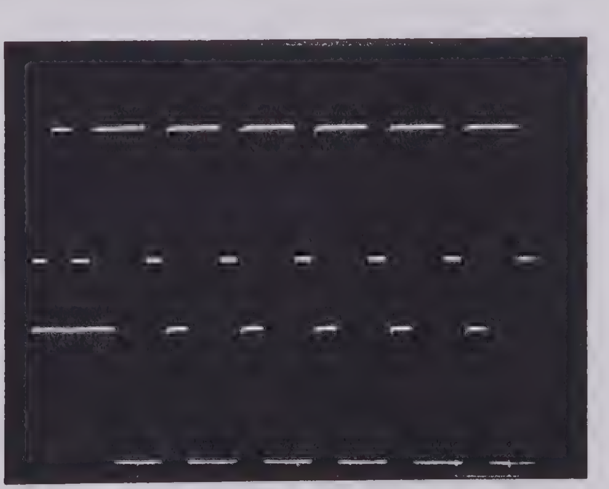
Main: 20 ms/Div.
Delayed: .1 ms/Div

Figure 5-36. Vdc, 3V Range, Burst #2



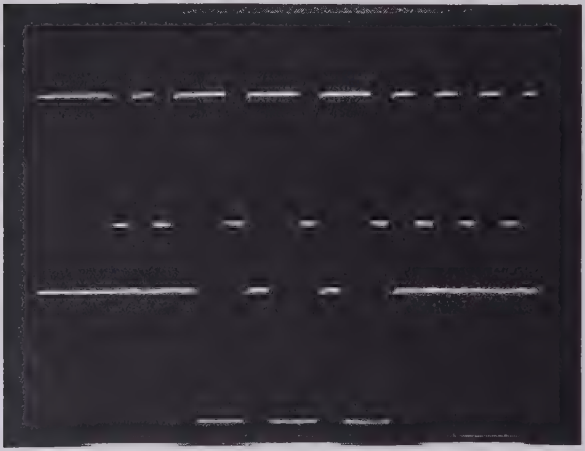
Main: .1 ms/Div. (single sweep, storage scope)

Figure 5-35. Vdc, 3V Range, Burst #1



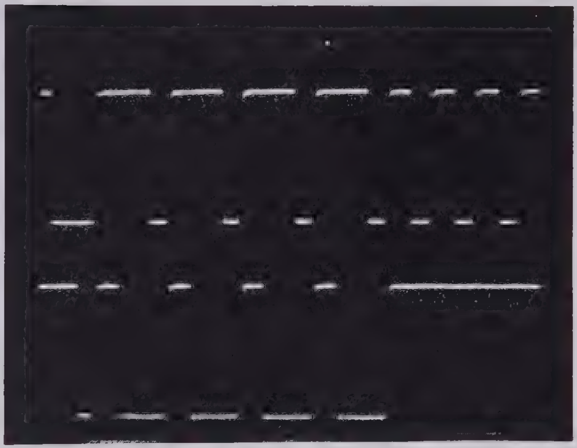
Main: 20 ms/Div.
Delayed: .1 ms/Div.

Figure 5-37. Vdc, 3V Range, Burst #3



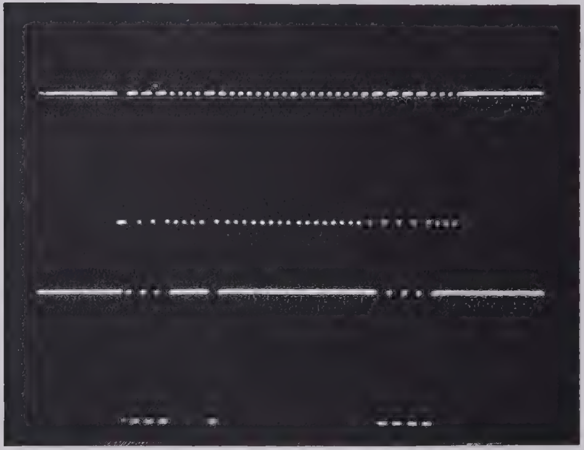
Horiz: Main: 20 ms/Div.
Delayed: .1 ms/Div.

Figure 5-38. Vdc, 3V Range, Burst #4



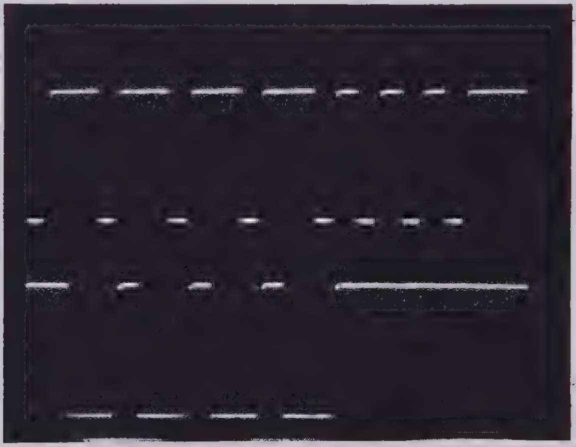
Horiz: Main: 20 ms/Div.
Delayed: .1 ms/Div.

Figure 5-40. Vdc, 3V Range, First Part of Burst #5



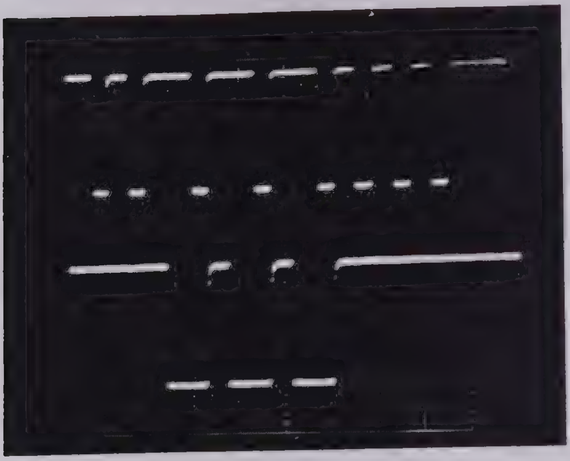
Main: 20 ms/Div.
Delayed: .5 ms/Div.

Figure 5-39. Vdc, 3V Range, Burst #5 Overall



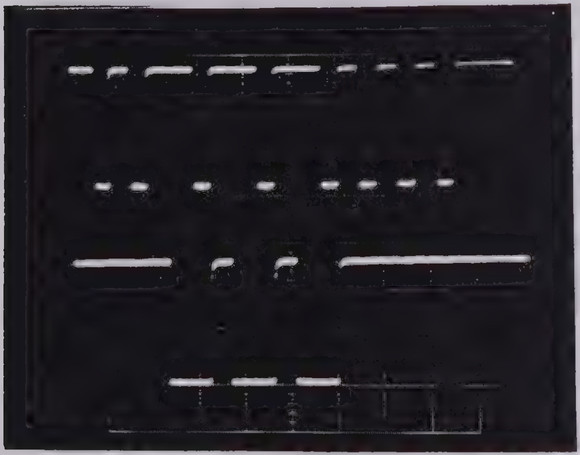
Main: 20 ms/Div.
Delayed: .1 ms/Div.

Figure 5-41. Vdc, 3V Range, Last Part Of Burst #5



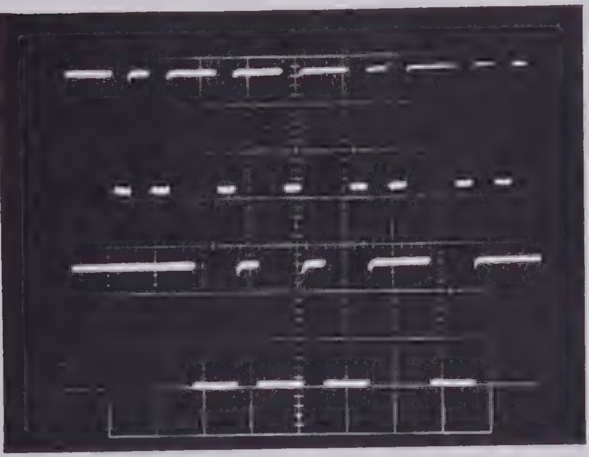
Horiz: Main: 20 ms/Div.
Delayed: .1 ms/Div.

Figure 5-42. **Vdc, 3V Range, Burst #6**



Main: 20 ms/Div.
Delayed: .1 ms/Div.

Figure 5-43. **Vdc, 3V Range, Burst #7**



Main: 20 ms/Div.
Delayed: .1 ms/Div.

Figure 5-44. **Vdc, 3V Range, Burst #8**

signal to the converter. The only difference between this and the preceding pattern is that LEDEN goes high, enabling the U20D nand gate.

If the OUT signal from the A/D converter is high, meaning a positive A/D analog input signal polarity, U20A-3 will go low. This causes U20B-6 to be high, U20C-8 to be low, and U20D-11 to be high. This turns off the U22 optoisolator's LED, which turns off the phototransistor. J5-8 is high, and the corresponding -8 pin on the motherboard connector is high. See the motherboard schematic, 0103-00-1808. After being inverted twice by the gate array input board, the signal (high) goes to the channel's input on gate array U27.

If the OUT signal from the A/D converter is low, meaning a negative A/D analog input signal polarity, U20A-3 is high, U20B-6 is low, U20C-8 is high, and U20D-11 is low. The U22 LED is on, J5-8 is low, etc.

3. After the preset integration period is complete, the third shift (8 bits) comes over, followed by its latch pulse, which puts the converter into the deintegrate phase. During this phase, the A/D converter puts out the time-duration high level signal called OUT at U12-14, which duration is proportional to the input signal amplitude. LEDEN, A/D-B, and A/D-A are high. During this duration while OUT is high, the channel's input pin on the motherboard U27 IC is high. Note that the motherboard measures the time from when it sent the latch pulse, to when OUT goes low.
4. Shortly thereafter, the fourth shift, 8 bits, comes over. This puts the converter into the gross-zero phase (ZI).

5. The fifth shift is a 32 bit shift, containing the setup information for the next measurement that the module is to do. It also contains a repeat of the ZI command to the A/D converter.
6. The sixth shift, 8 bits, is another repeat of the ZI command to the A/D converter.
7. The seventh shift is another repeat of the ZI command to the A/D converter.
8. The eighth shift is a fine auto-zero (AZ) command to the A/D converter. The converter will continuously auto-zero itself until the next shift comes over.

   Then the program asks the question "Is there a measurement delay?" If there is, it comes at this point. After any delay, the first shift for the next measurement cycle will occur.

Figures 5-34 through 5-44 show what the 8 bursts for the **Vdc** measurement cycle look like on an oscilloscope. In each photo, $\overline{\text{CLOCK}}$ (U24A-7) is on the top, and $\overline{\text{DATA}}$ (U24B-6) is on the bottom. DMM mode, or a single-measurement channel list is run. Vertical sensitivity is 2V/division. Triggering is normal, on the first ↓ edge of $\overline{\text{CLOCK}}$ in the measurement cycle. Some measurement delay (approximately 1 second) must be used to prevent random scope retracing. To see each burst in the measurement cycle after the first, either X10 horizontal, or delayed time base must be used. From these pictures you should be able to derive the data bit values in figure 5-33. If you are uncertain what the intermediate oscilloscope setups for these pictures could be, compare with the sequence in figure 5-31, board type checking.

5.4.5.4 dBdc

Section 5.3 references: 5.3.2.2, 5.3.2.7, 5.3.2.8.

dBdc does eight shifts per measurement cycle. The fifth shift is the 32-bit shift.

U10, U13, and U34 are updated only on shift number 5.

Default and General Pattern Explanation

The dBdc default range is 3V. Although the default modifiers are dBm, and Z=600, this affects how the software processes the return value from the measurement module, and not the control pattern. So, the default control pattern, and the available ranges, are the same as VDC, paragraph 5.4.5.3.

The A/D converter is cycled through the same phases, in the same order, as for Vdc (paragraph 5.4.4.4), although timing is slightly different.

5.4.5.5 CJTEMP

Section 5.3 references: 5.3.2.2, 5.3.2.7, 5.3.2.8.

Cold junction temperature does eight shifts per measurement cycle. The fifth shift is the 32-bit shift.

U10, U13, and U34 are updated only on shift number 5.

Aside from the channel specification, there are no modifiers to this function, so there is only one pattern. The setup pattern is the same as 3Vdc, except the following:

U30-11 is low and U30-7 is high. With K4 set, the A/D gain stage (1C4) can receive the output of the U7B selector.

dBdc

Default	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
General	D	1	1	F	D	0	0	B	0	0	0	0	0	0	G	G	0	0	M	M	M	M	M	M	d	d	1	1	1	E	P	P
	U10								**U13**								**U34**								**U30**							
Pin#	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay#	4	2	3	1	4	2	3	1																	5	5						
					S	S	S	S																	S							

CJTEMP

General	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	M	M	M	M	M	M	0	1	1	1	1	E	P	P
	U10								**U13**								**U34**								**U30**							
Pin#	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay#	4	2	3	1	4	2	3	1																	5	5						
					S	S	S	S																	S							

U13-13 is high. With (A/DINB) high, $\overline{\text{A/DINB}}$ is low. Since $\overline{\text{A/DINB}}$ is low, and $\overline{\text{A/DINA}}$ is high ((A/DINA), U13-14, is low), U7B selects the Y2 input from U1.

Also, U34-12, CJTEMPEN (Cold Junction TEMPerature ENable), is high. This causes any remote multiplexer that is connected to J6 to send its cold junction value into the rear panel J101-J201 terminals. This has no effect, since K4 is set.

If the cold junction reading specified by the user is on a multiplexer connected to the rear panel input, K4 would be reset in that case.

5.4.5.6 TEMP

Section 5.3 references: 5.3.2.2, 5.3.2.7, 5.3.2.8.

Temperature has the same basic 32-bit setup pattern as Vdc, except that U13-5, GAINB, is high. This causes U5, at 1C4, to be set to a gain of 100, instead of 1. At high levels of thermocouple input, U5 would put out more than 3.0 volts, so the U5 gain is automatically reduced to 10. To do this, GAINB is low, and GAINA (U13-4) is high.

Temperature does eight shifts per measurement cycle. The fifth shift is the 32-bit shift.

A selection of a rear panel J101-J102 channel input, such as for a multiplexer subchannel measurement, will cause the bits from U34-13, -14, -7, -6, -5, and -4 to represent the channel *subscript number* on their static lines.

5.4.5.7 OHMS, CONT, -▶|-CHK

Section 5.3 references: 5.3.2.2, 5.3.2.7, 5.3.2.8, 5.3.2.9, 5.3.2.10.

These (constant-current) functions all do eight shifts per measurement cycle. The fifth shift is the 32-bit shift.

U10, U13, and U34 are updated only on shift number 5.

Default Pattern Explanation

The dc gain path for the voltage that is developed across the resistance or diode under test is the same as for the Vdc measurement function.

Refer to table 5-4, if desired. K4 is RESET (U10-11 = 1). This means do not divide by 100, on schematic sheet 1. K2 is SET, so the constant current source is connected. K3 is RESET, so the AC CONVERTER section power is turned off, and AC1 is connected directly to AC2. K1 is RESET, so the front panel terminals, J1 and J2, are selected. K5 is RESET, so there is no divide by 100.

U13-11 ((OHMSC)) and U13-12 ((OHMSB)) are both high, making $\overline{\text{OHMSC}}$ and $\overline{\text{OHMSB}}$ both low (see schematic locations 2B7 and 4B3). U13-13 ((OHMSA)) and U13-14 ((OHMS)) are both high, making $\overline{\text{OHMSA}}$ and $\overline{\text{OHMS}}$ both low (see schematic locations 2B7 and 4D4). This produces a constant output current of 1.0 mA. This assumes that the resistance across the input terminals is less than 30Ω. See table 5-11 in paragraph 5.3.2.9. The default OHMS range is AUTO, which means that with the input terminals shorted, the unit will shift to the highest output current range (1.0mA), since it is attempting to develope an output voltage. The default CONTinuity range is 30Ω (1mA). The default -▶|-CHK (diode check) range is 1mA.

U13-5 (GAINB) is high, and U13-4 (GAINA) is low, making U5 have a gain of 100.

The MUX CONTROL lines are low, their default state, when the front panel terminals are selected.

U30-13, U30-14, and U30-7 are high, so U31-12 (3B1) is selected. U31-5 will therefore be low when $\overline{\text{FEN}}$ is low. And when $\overline{\text{FEN}}$ is high, this forces U31-5 low, regardless of the state of any inputs. So FOUT is always high, enabling the output of the A/D section at U20B-5 (2D5).

See paragraph 5.4.4.4 for the cycling of the E P P bits.

OHMS, CONT, -▶|-CHK

Default	1	0	1	1	0	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
General	D	1	1	F	D	0	0	B	0	0	0	0	0	0	G	G	0	0	M	M	M	M	M	M	d	d	1	1	1	E	P	P
	U10								U13								U34								U30							
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4	2	3	1	4 S	2 S	3 S	1 S																	5 S	5						

OHMS, CONT, AND —▶|— CHK Control Bits

	Range			Control Bits							
				U13 Pin #						U30 Pin #	
Iout	Ohms	Continuity	Diode Check	−11	−12	−13	−14	−5	−4	−11	−12
1mA	30 Ω	30 Ω	1 mA	1	1	1	1	1	0	1	0
1 mA	300 Ω	300 Ω		1	1	1	1	0	1	1	0
1 mA	3 KΩ	3 KΩ		1	1	1	1	0	0	1	0
100uA	30 KΩ	30 KΩ	100 uA	1	0	1	1	0	0	1	0
10 uA	300 KΩ	300 KΩ	10 uA	1	0	0	1	0	0	1	0
1 uA	3 MΩ	3 MΩ	1 uA	0	1	1	1	0	0	1	0
.1 uA	30 MΩ	30 MΩ	.1 uA	0	1	0	1	0	0	1	0
.1 uA	300 MΩ	300 MΩ		0	1	0	1	0	0	0	1
.1 uA	3000 MΩ	3000 MΩ		0	1	0	1	0	0	0	1

General Pattern Explanation

DC-R and DC-S reset or set relay K4. K4 is reset (U10-11 = 1) and K5 is reset (U30-12 = 1) on shift number 5. The exception to this is the 300MΩ and 3000MΩ ranges: K5 is set, causing the 10mΩ RN2 (1C6) to be placed in parallel with the unknown resistance. K1 is reset (U10-14 = 1) for a Front panel measurement, or set (U10-4 = 1) for a Back panel or multiplexer measurement.

U30-11 and -12 control whether K5 is set or reset.

U13-5 and U13-4, GAINB and GAINA, set the gain of the DC amplifier U5 (schematic location 1D4).

5.4.5.8 Vac

Volts ac does eight shifts per measurement cycle. The fifth shift is the 32-bit shift. The sequencing of the A/D converter is the same as for Vdc.

Section 5.3 references: 5.3.2.2, 5.3.2.3, 5.3.2.4, 5.3.2.10.

U10, U13, and U34 are updated only from shift number 5.

K4 is always reset (U10-11 = 1), since the the AC CONVERTER is not dc coupled. K2 is always reset, since the constant current source is not connected. K3 is always set, since the input signal must be routed to the ac section (schematic sheet 3); and, the ac section power (+12VSW) must be on. K1 is reset (U10-14 = 1) for a Front panel input; or set (U10-4 = 1) for a Back panel input. K5 is reset (U30-12 = 1), when there is no dividing of the amplitude by 100.

U13-11, $\overline{\text{DCCOUP}}$, is high, when the ac section is ac coupled. U13-12, ACAMPS, is always low, since the current shunt signals are not allowed into the ac section. U13-13 and U13-14 are always low.

U13-5 and U13-4 are always high. This causes U6A (1D3) to select the ACOUT input from location 3C1.

Along with K5, control bits U13-7, GAIND, and U13-6, GAINC set the AC CONVERTER gain, according to the following:

Range	U30-11	U30-12	U13-7	U13-6
30mVac	0	1	1	1
300mVac	0	1	1	0
3Vac	0	1	0	0
30Vac	1	0	1	0
300Vac	1	0	0	0

Vac

Default	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	E	P	P
General	1	1	1	F	0	0	0	B	R	R	0	0	g	g	1	1	0	0	M	M	M	M	M	M	d	d	1	1	1	E	P	P
	U10								U13								U34								U30							
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4	2	3	1	4 S	2 S	3 S	1 S																	5 S	5						

U34-11 and U34-12 are always low; the SCHMITT TRIGGER is not used. If a multiplexer is being used, U34-13, -14, -7, -6, -5, and -4 are the subchannel selection bits; otherwise they are low.

U30-13, -14, and -7 are always high on A/D functions.

U30-6, -5, and -4 cycle according to paragraph 5.4.4.4.

5.4.5.9 Vac+dc

Volts ac+dc does eight shifts per measurement cycle. The fifth shift is the 32-bit shift. The sequencing of the A/D converter is the same as for Vdc.

Section 5.3 references: 5.3.2.2, 5.3.2.3, 5.3.2.4, 5.3.2.10.

Vac+dc functions exactly the same as Vac (paragraph 5.4.5.8), except the AC CONVERTER is dc coupled. K4 is set (U10-7 = 1), and U13-11, $\overline{\text{DCCOUP}}$, is low.

5.4.5.10 dB

dB (ac) functions exactly the same as Vac on the measurement module (paragraph 5.4.5.8). The difference is in how software causes the measured quantity to be displayed.

Section 5.3 references: 5.3.2.2, 5.3.2.7, 5.3.2.8, 5.3.2.10.

5.4.5.11 Adc

Amperes dc does eight shifts per measurement cycle. The fifth shift is the 32-bit shift. U10, U13, and U34 are updated only from shift number 5. The sequencing of the A/D converter is the same as for Vdc.

Note the similarity in the control pattern to the CJTEMP control pattern (paragraph 5.4.5.5). Section 5.3 references: 5.3.2.2, 5.3.2.7, 5.3.2.8, 5.3.2.10.

K2 is always reset, so the constant current source isn't connected. K3 is always reset, so ac section power is off. K1 is always reset, so the front panel input is selected and J2 serves as the signal low side (see 1B6).

U30-11 is low and U30-7 is high. With K4 always set, the A/D GAIN stage (1C4) can receive the output of the U7B selector.

Default: U13-13 is high. With (A/DINB) high, $\overline{\text{A/DINB}}$ is low. (A/DINA), U13-14, is high), causing $\overline{\text{A/DINA}}$ to be low. So U7B selects the Y0 input from U1. This is the MA-IN signal which comes from R14, F1, and J3 (location 4B2).

General: At U7B, location 1C5, the most significant control input is pin 9, $\overline{\text{A/DINA}}$, which is an inversion of U13-14. U13-14 is always high, $\overline{\text{A/DINA}}$ is always low, so U7B always selects either its Y0 or Y1 input. The least significant control input of U7B is pin 10, $\overline{\text{A/DINB}}$, which is inverted from U13-13. U30-13 controls whether the high current shunt, J4-J3, or the low current shunt, J3-J2 is selected. A low at U13-13 indirectly causes U7B to select its Y1 input. The gain of U5 is directly controlled by U13-5 and U13-4.

Range	(A/DINB) U13-14	(A/DINA) U13-13	GAINB U13-5	GAINA U13-4
30mA	1	1	1	0
300mA	1	1	0	1
3A	1	0	1	0
10A	1	0	0	1

See paragraph 5.4.4.4 for the cycling of the E P P bits.

Vac + dc

				U10								U13								U34								U30				
Default	0	1	0	1	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
General	0	1	0	F	1	0	1	B	0	R	0	0	g	g	1	1	0	0	M	M	M	M	M	M	d	d	1	1	1	E	P	P
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4 S	2 S	3 S	1 S	4	2	3	1																	5 S	5						

Adc

				U10								U13								U34								U30				
Default	0	1	1	1	1	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
General	0	1	1	1	1	0	0	0	0	0	R	R	0	0	G	G	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4	2	3	1	4 S	2 S	3 S	1 S																	5 S	5						

Aac

	U10								U13								U34								U30							
Default	1	1	0	1	0	0	1	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
General	1	1	1	1	0	0	0	0	R	R	0	0	g	g	1	1	0	0	M	M	M	M	M	M	d	d	1	1	1	E	P	P
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4	2	3	1	4	2	3	1																	5	5						
					S	S	S	S																	S							

5.4.5.12 Aac

Amperes ac does eight shifts per measurement cycle. The fifth shift is the 32-bit shift. U10, U13, and U34 are updated only from shift number 5.

The sequencing of the A/D converter is the same as for Vdc.

Section 5.3 references: 5.3.2.2, 5.3.2.3, 5.3.2.4, 5.3.2.8, 5.3.2.10.

Amperes ac uses the same shunts and signal selecting (MA-IN vs. A-IN) as Adc, but then the U7B selector output on the A/DMUX line is taken by U17B-6 (3C6), instead of by R65 and K4 on sheet 1.

K4 is always reset (U10-11 = 1), since the input of the AC CONVERTER is not dc coupled. U13-11, $\overline{\text{DCCOUP}}$ is always high, so the output of the AC CONVERTER is ac coupled. K2 is always reset, since the constant current source is not connected. K3 is always set (3B8), since the ac section power (+12VSW) must be on. K1 is reset (U10-14 = 1) since it is a Front panel input. K5 is set (U30-11 = 1); however, the output of U15D is not used.

U13-12, ACAMPS, is always high, since the current shunt signals on the A/DMUX line must be routed into the ac section by U17B (3C6).

U13-5 and U13-4 are always high. This causes U6A (1D3) to select the ACOUT input from location 3C1.

U13-14, and U13-13 indirectly select which current shunt is used, and control bits U13-7, GAIND, and U13-6, GAINC set the AC CONVERTER gain, according to the following:

Range	(A/DINB) U13-14	(A/DINA) U13-13	GAIND U13-7	GAINC U13-6
30mA	1	1	1	1
300mA	1	1	1	0
3A	1	0	1	1
10A	1	0	1	0

U34-11 and U34-12 are always low; the SCHMITT TRIGGER is not used.

U30-13, -14, and -7 are always high on A/D functions.

U30-6, -5, and -4 cycle according to paragraph 5.4.4.4.

5.4.5.13 Aac + dc

Amperes ac + dc does eight shifts per measurement cycle. The fifth shift is the 32-bit shift. The sequencing of the A/D converter is the same as for Vdc.

Section 5.3 references: 5.3.2.2, 5.3.2.3, 5.3.2.4, 5.3.2.8, 5.3.2.10.

Amperes ac uses the same shunts and signal selecting (MA-IN vs. A-IN) as Adc, but then the U7B selector output on the A/DMUX line is taken by U17B-6 (3C6), instead of by R65 and K4 on sheet 1.

Amperes ac + dc functions exactly the same as Aac, except the AC CONVERTER is dc coupled. K4 is set (U10-7 = 1), and U13-11, $\overline{\text{DCCOUP}}$, is low.

K2 is always reset, since the constant current source is not connected. K3 is always set (3B8), since the ac section power (+12VSW) must be on. K1 is reset

Aac + dc

	U10								U13								U34								U30							
Default	0	1	0	1	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
General	0	1	0	F	1	0	1	B	0	R	0	0	g	g	1	1	0	0	M	M	M	M	M	M	d	d	1	1	1	E	P	P
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4	2	3	1	4	2	3	1																	5	5						
	S	S	S	S																					S							

(U10-14 = 1) since it is a Front panel input. K5 is set (U30-11 = 1); however, the output of U15D is not used.

U13-12, ACAMPS, is always high, since the current shunt signals on the A/DMUX line must be routed into the ac section by U17B (3C6).

U13-5 and U13-4 are always high. This causes U6A (1D3) to select the ACOUT input from location 3C1.

U13-14, and U13-13 indirectly select which current shunt is used, and control bits U13-7, GAIND, and U13-6, GAINC set the AC CONVERTER gain, according to the following:

Range	(A/DINB) U13-14	(A/DINA) U13-13	GAIND U13-7	GAINC U13-6
30mA	1	1	1	1
300mA	1	1	1	0
3A	1	0	1	1
10A	1	0	1	0

U34-11 and U34-12 are always low; the SCHMITT TRIGGER is not used.

U30-13, -14, and -7 are always high on A/D functions.

U30-6, -5, and -4 cycle according to paragraph 5.4.4.4.

5.4.5.14 Wdc

Section 5.3 references: 5.3.2.2, 5.3.2.7, 5.3.2.8, 5.3.2.10.

For Watts dc, the Model 52 or 51 automatically does alternate measurements of dc voltage (Vdc, paragraph 5.4.5.3) and dc amperes (Adc, paragraph 5.4.5.11); software multiplies the readings together to obtain one value.

There are eight shifts on each measurement cycle. The fifth shift of each is the 32-bit shift.

On a given function, the sequencing of the A/D converter is similar to what it is on Vdc.

Both Current And Voltage

K2 is always reset — constant current source is not connected. K3 is always reset — input signal is routed to dc section (sheet 1). K1 is always reset — front panel is selected.

K4 is always set, so the dc amplifier U5 is always fed by the output of U7B. On the voltage measurement, the signal is always divided by 100. K5 is set.

U13-12, ACAMPS, is low, so the A/DMUX signal (1C5) is not admitted into the ac section (3C6).

U13-7 and U13-6 are always low.

U34-11 and U34-12 are always low; the SCHMITT TRIGGER is not used.

U30-13, -14, and -7 are always high on A/D functions.

U30-6, -5, and -4 cycle according to paragraph 5.4.4.4.

Current

U13-14 is high. This signifies that current is being measured. U13-14 is inverted by U8 (2B7); then $\overline{\text{A/DINA}}$, low, goes to U7B-9 (1C5). This commands U7B to select either the Y0 or Y1 input, depending (indirectly) on the state of $\overline{\text{A/DINB}}$.

Control bits U13-5, GAINB, and U13-4, GAINA, directly set the A/D GAIN gain, according to the following:

Range	(A/DINB) U13-14	(A/DINA) U13-13	GAINB U13-5	GAINA U13-4
300mA	1	1	0	1
3A	1	0	1	0
10A	1	0	0	1

Wdc

	U10								U13								U34								U30							
Default	0	1	1	1	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
General	0	1	1	1	1	0	0	0	0	0	R	1	0	0	G	G	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
Default	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
General	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	G	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4	2	3	1	4	2	3	1																	5	5						
				S	S	S	S																		S							

In the control patterns above, the first two patterns describe dc current, and the second two patterns describe dc voltage.

Voltage

U13-13 and U13-14 are both low. This signifies that divided by 100 voltage is being selected by U7B.

K5 is always set — divide by 100. Control bits U13-5, GAINB, and U13-4, GAINA, directly set the A/D GAIN gain, according to the following:

Range	U13-5	U13-4
30Vdc	0	1
300Vdc	0	0

5.4.5.15 VAac

For Volt-amperes ac, the unit automatically does alternate measurements of ac voltage (Vac, paragraph 5.4.5.8) and ac amperes (Aac, paragraph 5.4.5.12); software multiplies the readings together to obtain one value.

Section 5.3 references: 5.3.2.2, 5.3.2.3, 5.3.2.4, 5.3.2.8, 5.3.2.10.

There are eight shifts on one measurement cycle; the fifth shift is the 32-bit shift. There are ten shifts on the other measurement cycle; the fifth and seventh shifts are 32-bit shifts.

In the control patterns below, the first two patterns describe ac current, and the second two patterns describe ac voltage.

Both Current And Voltage

K2 is always reset — constant current source is not connected. K3 is always set — the J1 voltage input signal is routed to the ac section (point AC1 on sheet 1). K1 is always reset — front panel is selected.

K4 is reset, so the input of U15D (3D8) is ac coupled. K5 is set, so on the voltage measurement, the signal is always divided by 100 by U15D.

U13-5 and U13-4 are always high. This causes U6A (1D3) to select the ACOUT input from location 3C1.

U34-11 and U34-12 are always low; the SCHMITT TRIGGER is not used.

U30-13, -14, and -7 are always high on A/D functions.

U30-6, -5, and -4 cycle according to paragraph 5.4.4.4.

U13-11, $\overline{\text{DCCOUP}}$, is always high (ac coupling), on the VAac function.

Current

U13-12, ACAMPS, is high, so the A/DMUX signal (1C5) is admitted into the ac section by U17B (3C6).

U13-14 is high. This signifies that current is being measured. U13-14 is inverted by U8 (2B7); then $\overline{\text{A/DINA}}$, low, goes to U7B-9 (1C5). This commands U7B to select either the Y0 or Y1 input, depending (indirectly) on the state of $\overline{\text{A/DINB}}$.

Control bits U13-7, GAIND, and U13-6, GAINC, directly set the AC CONVERTER gain, according to the following:

Range	(A/DINB) U13-14	(A/DINA) U13-13	GAIND U13-7	GAINC U13-6
300mA	1	1	1	0
3A	1	0	1	1
10A	1	0	1	0

Voltage

U13-12, ACAMPS, is low, so the A/DMUX signal (1C5) is not admitted into the ac section by U17B (3C6).

U13-13 and U13-14 are both low. This signifies that divided by 100 voltage is being selected by U7B; however, the output of U7B is not used.

K5 is always set — divide by 100 (3C7). Control bits U13-7, GAIND, and U13-6, GAINC, directly set the AC CONVERTER gain, according to the following:

Range	U13-7	U13-6
30Vdc	1	0
300Vdc	0	0

VAac

Default	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
General	1	1	0	1	0	0	1	0	1	0	R	1	1	g	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
Default	1	1	0	1	0	0	1	0	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
General	1	1	0	1	0	0	1	0	1	0	0	0	g	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
	U10								U13								U34								U30							
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4	2	3	1	4	2	3	1																	5	5						
					S	S	S	S																	S							

VAac + dc

Default	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
General	1	1	0	1	0	0	1	0	1	0	R	1	1	g	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
Default	1	1	0	1	0	0	1	0	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
General	1	1	0	1	0	0	1	0	1	0	0	0	g	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	E	P	P
	U10								**U13**								**U34**								**U30**							
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4	2	3	1	4 S	2 S	3 S	1 S																	5 S	5						

5.4.5.16 VAac + dc

Volt-amperes ac + dc does two different types of measurement cycles. There are eight shifts on one measurement cycle; the fifth shift is the 32-bit shift. There are ten shifts on the other measurement cycle; the fifth and seventh shifts are 32-bit shifts.

VAac + dc functions exactly the same as VAac (paragraph 5.4.5.15), except the AC converter is dc coupled on the volts function. K4 is set (U10-7 = 1), and U13-11, $\overline{\text{DCCOUP}}$, is low.

In the control patterns above, the first two patterns describe ac current, and the second two patterns describe ac voltage.

5.4.5.17 Counter Functions

5.4.5.17.1 General

Counter functions have a different arrangement of shift, since unlike A/D functions, the A/D CONVERTER doesn't have to be cycled. See figures 5-28 and 5-29. The shift format for all counter functions is one 32-bit burst followed by one 8-bit burst.

Section 5.3 references: 5.3.2.10. 5.3.2.4, 5.3.2.5, 5.3.2.6.

The measurement functions in paragraphs 5.4.5.17.2 through 5.4.5.18 have the same default control pattern. It is given below.

U10, U13, U34, and U30 are updated on the first of the two shifts. The second shift occurs after one timing period, and is an 8 bit shift, used only to take U30-12 back low. This deenergizes the K5 reset coil. Recall from paragraph 5.4.2.3.3, that the control bits of U10 that are made high on the 32 bit shift, automatically go back low after one timing period (8.3 or 10.0ms).

U13-11 is high on all counter functions, except for LOGIC.

Default Pattern Explanation

(Refer to table 5-4, if desired.) K4 is RESET (U10-11 = 1).In conjunction with $\overline{\text{DCCOUP}}$ (U13-11) being high, this provides for ac coupling on the input and output of the AC CONVERTER section. K2 is RESET, so the constant current source is not connected in. K3 is SET, so the AC CONVERTER section power (3B8) is turned on. Also, **AC1 (3D7) is connected by K3 to K3-9**, which feeds C2 and K4. K1 is RESET, so the front panel terminals, J1 and J2, are selected. K5 is RESET, by U30-12 being (pulsed) high, so U15D does not divide the amplitude by 100.

U13-12 (ACAMPS) is low, so U17B (3C6) does not pass the A/DMUX signal into the AC CONVERTER.

U13-13 and U13-14 are both low, making $\overline{\text{A/DINA}}$ and $\overline{\text{A/DINB}}$ (1C5) high. (U7B connects pin 13 to pin 11,

Counter Functions

Default	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
General	D	1	1	F	D	0	0	B	1	0	0	0	g	g	1	1	0	0	M	M	M	M	M	M	d	d	r	r	r	1	0	0
	U10								**U13**								**U34**								**U30**							
Pin #	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
Relay #	4	2	3	1	4 S	2 S	3 S	1 S																	5 S	5						

which is pulled to ground by the bottom part of RN2.) U13-5 and U13-4 are both high, making GAINB and GAINA high (1C4). U5 is at a gain of 1, and U6A selects the ACOUT input. However, the A/D CONVERTER input is irrelevant.

U13-7, GAIND, and U13-6, GAINC, are both low. In conjunction with K5 being reset, this causes an overall gain in the AC CONVERTER of 1 (reference paragraph 5.3.2.4.). The gain of U15C and U15B is bypassed. U34-11, THRESHB, and U34-12, THRESHA, are both low. This makes the inputs to the comparators in the PROGRAMMABLE SCHMITT TRIGGER, +.4V to U21-4, and −.4V to U21-10.

The six MUX CONTROL lines are low, their default state when the front panel terminals are selected.

U30-13, U30-14, and U30-7 are low, so U31-4 (3B1) is selected. $\overline{\text{FEN}}$ (U30-4) is low, enabling U31. This means that whatever signal is coming from the SCHMITT TRIGGER output at U27-6, passes out through U31-6 to the FOUT line, without being divided. If the signal is overrange, the motherboard will shift over a slightly different pattern to change the divide ratio, etc., assuming AUTO is the default selection for range on the measurement function of interest. FOUT goes to U20B-4 (2D5).

Besides enabling U31 (3B1), $\overline{\text{FEN}}$ goes to U20A-2 (2D5). At U20A, FEN inhibits the OUT signal from the A/D converter.

General Pattern Explanation

(Refer to table 5-4 as necessary.) The DC-R and DC-S lines are used to reset or set relay K4. K4 is reset (U10-11 = 1) if ac coupling is wanted on ac or counter functions. K2 is always reset (constant current source disconnected). K3 is always set (U10-13 low, U10-5 pulsed high), so the input signal is routed to "sheet 3" of the schematic. K1 is reset (U10-14 = 1) for a Front panel measurement, or set (U10-4 = 1) for a Back panel or multiplexer measurement. (Examples of Back panel channel numbers are 100, 101, 204, 364, and 464.) K5 would be reset (U30-12 = 1), if the input signal amplitude is small enough that U15D doesn't have to divide by 100. If the input signal is above 3 volts, K5 would be set (U30-11 = 1), and U15D would divide by 100.

U13-13 and U13-14 are always low, making $\overline{\text{A/DINA}}$ and $\overline{\text{A/DINB}}$ (1C5) always high. (U7B connects pin 13 to pin 11, which is pulled to ground by the bottom part of RN2.) U13-5 and U13-4 are always high, making GAINB and GAINA always high (1C4). (U5 is at a gain of 1.)

On counter functions, the gain choices are not called *ranges*. The circuit gain on schematic sheet 3 is set by the SENSITivity menu, in conjunction with an AC/DC menu choice. (Once the **Func**tion is selected, press the **Mods** button, then select SENSIT.) The term *range* is reserved for frequency division ratios.

U13-7, GAIND, and U13-6, GAINC, depend on the sensitivity. In conjunction with K5 (U30-11 high, or U30-12 high), they control the gain of the ac amplification ahead of the SCHMITT TRIGGER (reference paragraph 5.3.2.4.).

The SENSITivity selection also generates the state of U34-11, THRESHB, and U34-12, THRESHA, to the SCHMITT TRIGGER. Different sensitivity selections are applicable, depending on whether ac coupling or dc coupling is selected. The default sensitivity (for ac or dc) is shown below followed by an asterisk (*).

Counter Function Sensitivities

SENSITivity		/100 U30-11	U30-12	U13-7	U13-6	Total Gain	U34-11	U34-12	U21-10	U21-4
ac	3mV	0	1	1	1	X100	0	0	−.4V	+.4V
	30mV	0	1	1	0	X10	0	0	−.4V	+.4V
	300mV*	0	1	0	0	X1	0	0	−.4V	+.4V
	3V	1	0	1	0	X.1(−)	0	0	−.4V	+.4V
	30V	1	0	0	0	X.01(−)	0	0	−.4V	+.4V
dc	±40mV	0	1	1	0	X10	0	0	−.4V	+.4V
	±.4V	0	1	0	0	X1	0	0	−.4V	+.4V
	CMOS5V	0	1	0	0	X1	0	1	+1.5V	+3.5
	TTL*	0	1	0	0	X1	1	0	+.8V	+2.0V
	CMOS12V	1	0	1	0	X.1	1	1	−.8V	−.4V
	+80V	1	0	0	0	X.01(−)	1	1	−.8V	−.4V

U13-12 (ACAMPS) is always low, so U17B (3C6) does not pass the A/DMUX signal into the AC CONVERTER. (On mAac and Aac, which are A/D functions, the A/DMUX signal is passed into the AC CONVERTER; but no provision is made in firmware for directly measuring the *frequency* of a current.)

The six MUX CONTROL lines reflect the subchannel address, if any is specified. A channel specification of X00 or X01 causes the six lines to all be low. A channel specification of X64 causes all six lines to be high, and so on. U34-13 is the MSB, and U34-4 is the LSB.

U30-13, U30-14, and U30-7 set the divide ratio of the PRESCALER (U33, U32, and U31, at 3B2). The Range selection generates these bits. (For the state of the control bits on a particular range, see the particular counter function in one of the following numbered paragraphs.

$\overline{\text{FEN}}$ (U30-4) is always low, enabling U31. This means that whatever signal is coming from the SCHMITT TRIGGER output at U27-6, passes out through U31-6 to the FOUT line, after being divided by 1, 4, 32, 256, 2048, or 16384. If the signal is overrange, the motherboard will shift over a slightly different pattern to change the divide ratio, etc., assuming AUTO is the default selection for range on the measurement function of interest. FOUT goes to U20B-4 (2D5).

Besides enabling U31 (3B1), $\overline{\text{FEN}}$ goes to U20A-2 (2D5). At U20A, FEN inhibits the OUT signal from the A/D converter.

Assuming the same measurement is being repeated, LEDEN, U30-6, stays high continuously.

5.4.5.17.2 EVENTS

EVENTS is set up by a 32 bit shift, followed by an 8 bit shift one timing period later. The "window" to the motherboard stays open as long as the measurement is being repeated. LEDEN is high, and $\overline{\text{FEN}}$ is low.

Events has no range choices that modify the default pattern. The input frequency passes through the PRESCALER without being divided.

For the default pattern, signal routing, and the SENSITivity selections along with their control bits, see paragraph 5.4.5.17.1.

Section 5.3 references: 5.3.2.10. 5.3.2.4, 5.3.2.5, 5.3.2.6.

5.4.5.17.3 FREQ

FREQ is set up by a 32 bit shift, followed by an 8 bit shift one timing period later. The "window" to the motherboard stays open as long as the measurement is being repeated (LEDEN stays high).

Section 5.3 references: 5.3.2.10. 5.3.2.4, 5.3.2.5, 5.3.2.6.

FREQ has 7 range choices (aside from AUTO) that may modify the default pattern. The PRESCALER input frequency is divided by the PRESCALER depending on the pattern of the FOUTC, FOUTB, and FOUTA control bits. **Disp**lay **RES**olution modifies the pattern according to whether the digits of resolution (the choice is accessed by the **Disp**lay modifier key) is 99999, 999999, or 9999999.

If the input frequency is above 30% of the selected range, (but not over 100% of range), the motherboard will shift over control bits for the next higher frequency range. The displayed range selection will remain the same.

Three other choices on the range menu, X10, X100, and X1000, do not modify the control bits. One of these choices may be used if an external prescaler is used ahead of the Model 52 input — the choice affects only how the frequency is displayed.

Choosing either of the bargraph selections on the RESolution menu does not affect the control bits.

For the default pattern, signal routing, and the SENSITivity selections along with their control bits, see paragraph 5.4.5.17.1.

FREQ Range Control Bits

RES	99999				999999				9999999			
	FOUTC	FOUTB	FOUTA		FOUTC	FOUTB	FOUTA		FOUTC	FOUTB	FOUTA	
Range	U30-13	U30-14	U30-7	U31-6	U30-13	U30-14	U30-7	U31-6	U30-13	U30-14	U30-7	U31-6
10Hz	0	0	0	/1	0	0	0	/1	0	1	0	/4
100Hz	0	0	0	/1	0	1	0	/4	0	1	1	/32
1kHz	0	1	0	/4	0	1	1	/32	1	0	0	/256
10kHz	0	1	1	/32	1	0	0	/256	1	0	1	/2048
100kHz	1	0	0	/256	1	0	1	/2048	1	0	1	/2048
1MHz	1	0	1	/2048	1	0	1	/2048	1	1	0	/16384
4+MHz	1	0	1	/2048	1	1	0	/16384	1	1	0	/16384

PERIOD Range Control Bits

RES	99999				999999				9999999			
	FOUTC	FOUTB	FOUTA		FOUTC	FOUTB	FOUTA		FOUTC	FOUTB	FOUTA	
Range	U30-13	U30-14	U30-7	U31-6	U30-13	U30-14	U30-7	U31-6	U30-13	U30-14	U30-7	U31-6
100us	1	0	0	/256	1	0	1	/2048	1	0	1	/2048
1000us	0	1	1	/32	1	0	0	/256	1	0	1	/2048
10ms	0	1	0	/4	0	1	1	/32	1	0	0	/256
100ms	0	1	0	/4	0	1	0	/4	0	1	1	/32
1000ms	0	0	0	/1	0	0	0	/1	0	1	0	/4

5.4.5.17.4 PERIOD

PERIOD is set up by a 32 bit shift, followed by an 8 bit shift one timing period later. The "window" to the motherboard stays open as long as the measurement is being repeated. LEDEN is high, and $\overline{\text{FEN}}$ is low.

Section 5.3 references: 5.3.2.10. 5.3.2.4, 5.3.2.5, 5.3.2.6.

The input frequency is divided by the PRESCALER depending on the pattern of the FOUTC, FOUTB, and FOUTA control bits. **Disp**lay **RES**olution modifies the pattern according to whether the digits of resolution (accessed by the **Disp**lay modifier button) is 99999, 999999, or 9999999.

PERIOD has 5 ranges, and 3 choices of display resolution.

Choosing either of the bargraph selections on the RESolution menu does not affect the control bits.

For the default pattern, signal routing, and the SENSITivity selections along with their control bits, see paragraph 5.4.5.17.1.

5.4.5.17.5 T-INT, T-INT..1SHOT

T-INT and T-INT..1SHOT are set up by a 32 bit shift, followed by an 8 bit shift one timing period later. LEDEN is high, and $\overline{\text{FEN}}$ is low.

Section 5.3 references: 5.3.2.10. 5.3.2.4, 5.3.2.5, 5.3.2.6.

The input frequency is not divided by the PRESCALER. The pattern of the FOUTC, FOUTB, and FOUTA control bits is 0, 0, 0, regardless of the range or **Disp**lay **RES**olution. Ranges are 100ms, 1000ms, 10s, 100s, and 360s. **Disp**lay **RES**olution choices are 99999, 999999, and 9999999.

Choosing either of the bargraph selections on the RESolution menu does not affect the control bits.

For the (default) pattern, signal routing, and the SENSITivity selections along with their control bits, see paragraph 5.4.5.17.1.

5.4.5.17.6 P-WTH, P-WTH..1SHOT

P-WTH and P-WTH..1SHOT are set up by a 32 bit shift, followed by an 8 bit shift one timing period later. LEDEN is high, and $\overline{\text{FEN}}$ is low.

Section 5.3 references: 5.3.2.10. 5.3.2.4, 5.3.2.5, 5.3.2.6.

The input frequency is not divided by the PRESCALER. The pattern of the FOUTC, FOUTB, and FOUTA control bits is 0, 0, 0, regardless of the range or **Disp**lay **RES**olution. Ranges are 100ms, 1000ms, 10s, 100s, and 360s. **Disp**lay **RES**olution choices are 99999, 999999, and 9999999.

Choosing either of the bargraph selections on the RESolution menu does not affect the control bits.

For the (default) pattern, signal routing, and the SENSITivity selections along with their control bits, see paragraph 5.4.5.17.1.

5.4.18 LOGIC

LOGIC is set up by a 32 bit shift, followed by an 8 bit shift one timing period later. LEDEN is high, and $\overline{\text{FEN}}$ is low.

LOGIC has no range choices. LOGIC has only the dc SENSITivity selections.

For the (default) pattern, signal routing, and the SENSITivity selections along with their control bits, see paragraph 5.4.5.17.1.

5.5 MODEL 52 KEYPAD CIRCUITRY

The keyboard is scanned during the power-on routine to see if any special key combinations, such as a power-on clear, are pressed.

Once the unit is displaying menus, or is running a channel list or program, the keyboard is scanned once per periodic interrupt (paragraph 5.2.8.5.2). The exception to this is when the program is timing a key debounce interval — it doesn't bother scanning the keyboard then.

See motherboard drawing number 0103-00-1808, sheet 1, zone B2, and keypad board drawing number 0103-00-2414. U10B and U11 are the means by which the software reads the keyboard.

First, the MPU reads address 0600_H, since this detects whether *any* key is currently pressed. When a keypress is detected, the software delays about four more interrupt periods, then checks 0600_H once more to verify that a key is still pressed. If so, the following sequence is executed.

The MPU reads addresses 0606_H, 0605_H, 0603_H sequentially. This puts the patterns in table 5-13 out.

Table 5-13. Keyboard Stimulation Pattern

A2	A1	A0
1	1	0
1	0	1
0	1	1

(Not shown are the state of the other address lines, which don't affect which column in the keyboard is scanned.)

Each time it puts one of the table 5-13 patterns out, the microprocessor is also examining AD0 through AD7 (during the data time of the cycle) to see where a low comes through. Each key in a group of (up to) eight has its own bit in a 8-bit byte. A key that is pressed will connect the LOW that they are all being driven with to an input on the HC244 that is normally pulled high. So, the software reads three groups of up to eight keys each.

Normally the U10B outputs are tristate. This allows U11's enable inputs (pins 19 and 1) to be pulled high by R39, causing the output of U11 on the left side to be tristate.

When the MPU reads an 06XX address, this causes the $\overline{\text{KEYBD}}$ signal to go low.

Remember from figure 5-9 that A0, A1, and A2 at the U10B input are latched and keep the address until the end of the cycle. At approximately the midpoint of the cycle, E at the input and output of U10B goes low. This makes U11 buffer the keypress (a low bit) across to the MPU bus, where AD0-AD7 are now acting as data lines to the MPU. A software routine then correlates the position of the low bit with the read address (0606_H, 0605_H, 0603_H) to determine which key was pressed.

(E comes from inverter output U19D-8, location 2A6.)

5.6 MODEL 52 DISPLAY ASSEMBLY

The dot matrix liquid crystal display (LCD) module is an Epson number EG-Y84320AT. The entire display module is replaceable as a unit. Section 5.6 will provide enough theory of operation to allow fault isolation to either the motherboard or the display module.

The display module has a resolution of 32 X 84 pixels, which is divided into quadrants for addressing purposes. The module has its own LCD driver. It also has a controller chip which contains enough static RAM to store the pixel pattern for one display. Each bit in the RAM corresponds to a unique pixel on the screen.

See sheet 1 of the motherboard schematic, zone A4. J4 is the 26-pin connector providing power and signals to the display module. There are two busses into the module: an 8 bit data bus (AD0-AD7), and a 7 bit address bus (A0-A6).

The $512\text{-}1535_{10}$ (200_H-$5FF_H$) area in motherboard RAM is pixel on-off storage for the Model 52 LCD display. Four of the 256-each decode lines from U23 to the display module are required to cover this area. DISP1-DISP4 (one low at a time) enable one of the four quadrants of the LCD display to be written to. $\overline{\text{DISP1}}$ enables the upper left quadrant, and $\overline{\text{DISP2}}$ enables the upper right quadrant. $\overline{\text{DISP3}}$ enables the lower left quadrant, and $\overline{\text{DISP4}}$ enables the lower right quadrant.

The MPU sends characters and messages to the screen as a complex dot matrix pattern. A low for a write data bit means that the pixel (point on the screen) corresponding to that bit will be off. Conversely, a high for a write data bit means that the pixel corresponding to that bit will be dark.

As part of the Model 52 power up routine, the display module is initialized. To put it into the correct modes, the following sequence is sent to each quadrant:

Table 5-14. Display Module Initialization Sequence

ADDRESS								DATA							
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
A7							A0	D7							D0

Format For Writing Data To Display Positions

See figure 5-45. Each quadrant is 16 dots vertically by 42 dots horizontally. The MPU sends out patterns as 8-bit bytes. A "vertical" data byte from the MPU represents the state (on or off) of either the top 8 pixels in a quadrant's column, or the lower 8 bits in the quadrant's column. There are a total of 84 byte locations in one quadrant; 336 byte locations for the whole display.

Recall from paragraph 5.2.8.5.7 (device address decoding), that only A15-A8 are required to generate a $\overline{\text{DISPx}}$ line, which serves as the quadrant-enable. This leaves A7-A0 available for determining pixel addresses.

If A6 is low, the data byte defines the state of the top 8 bits of a column. If A6 is high, the data byte defines the state of the bottom 8 bits of a column. A5 through A0 define which column in the quadrant the data byte is to go to. From the left, the columns are numbered 0 through 41_{10} (29_H).

Within the top half or lower half of a quadrant (8 vertical bits), D7 is the lowest pixel, D0 is the highest pixel, etc.

Write Operation Timing

One of the $\overline{\text{DISP}}$ lines goes low near the beginning of a MPU cycle. The address lines stabilize in the first half of the cycle, and remain solid throughout the cycle. $\overline{\text{WR}}$ goes low at the start of the data half of the cycle. The MPU puts the data byte on the AD7-AD0 bus. At the end of the cycle, $\overline{\text{WR}}$ goes high, causing the display module to latch the data.

The $\overline{\text{RD}}$ line goes low only when the cursor is blinking. The motherboard MPU does a read-write operation, toggling the contents of the display RAM locations corresponding to the present cursor location.

Viewing Angle

In a Model 52, P12-P14 (LCD1,2,and 3) are used to adjust the viewing angle of the front panel liquid crystal display. See the motherboard schematic, sheet 1, zone B4. U9, the 4051, is a one-of-eight analog switch. It functions here as a software settable selector switch. Every time the operator presses the **5 LCD** button on the front panel, the count on the three Sx lines is incremented. Depending on the states of P12-P14, U9 connects multiples of 6.8 Kohms between VR1 and VR2 on the display module.

The P10-P17 lines were discussed in paragraph 5.2.6.5.

5.7 DIGITAL INPUT/OUTPUT BOARD

5.7.1 General Description

The Digital Input/Output and Analog Output board (Option 50-14) provides eight bits of digital input (read), eight bits of digital output (write) and an analog output voltage. This board also routes the four external trigger signals to the trigger processing circuitry on the Motherboard.

The Digital I/O board is fully isolated from the measurement module channels and common to chassis ground. A Digital I/O board may plug into any or all of slots J7, J8, J9, and J10 on the Motherboard.

Figure 5-46 shows the five circuit blocks of the Digital I/O board and the relationship of the blocks to each other. The schematic 0103-00-1814 illustrates the digital I/O circuit in greater details.

The Digital I/O board consists of five circuit blocks (Control, Analog Output, Digital Output, Digital Input, and Board Identification). Control enables each of the other blocks. The analog output block produces an analog output voltage that supplies a specific voltage or

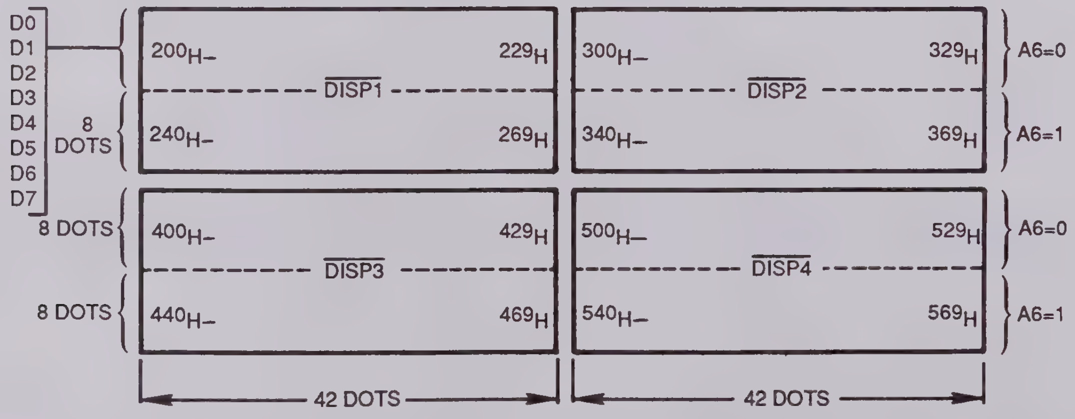


Figure 5-45. Display Addresses

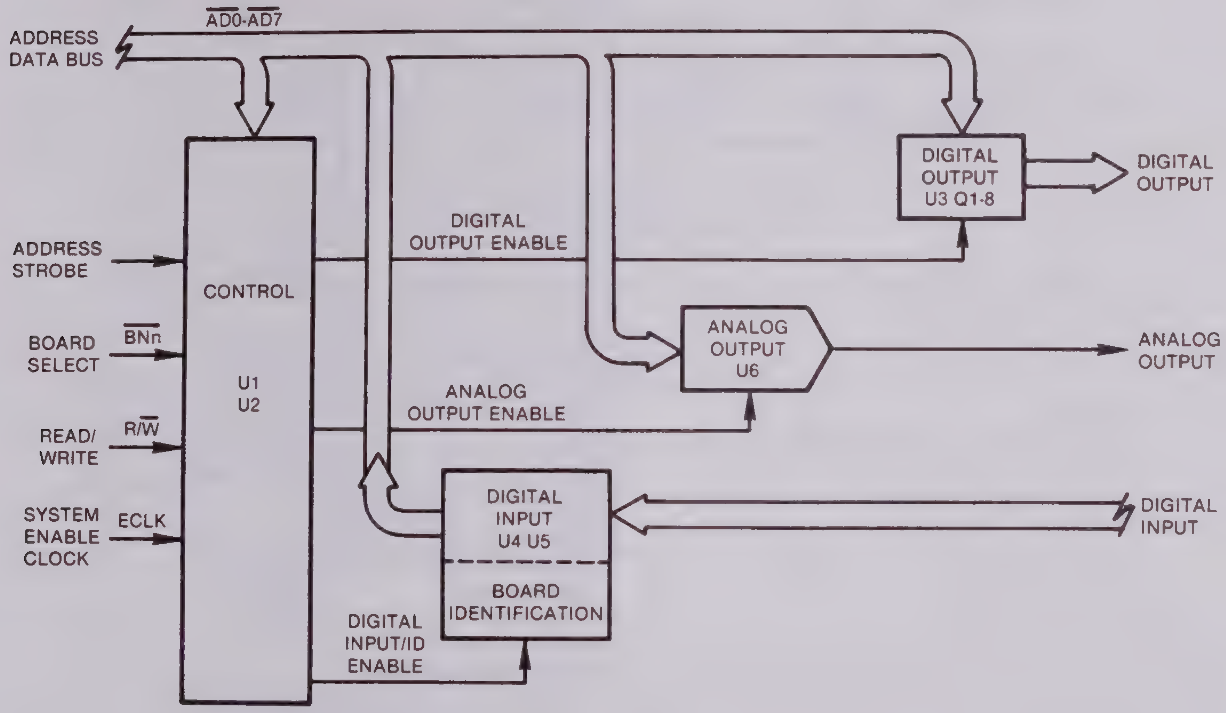

ADDRESS DATA BUS
AD0-AD7
CONTROL
U1
U2
ADDRESS STROBE
BOARD SELECT
BNn
READ/ WRITE
R/W
SYSTEM ENABLE CLOCK
ECLK
DIGITAL OUTPUT ENABLE
ANALOG OUTPUT ENABLE
DIGITAL INPUT/ID ENABLE
DIGITAL OUTPUT U3 Q1-8
DIGITAL OUTPUT
ANALOG OUTPUT U6
ANALOG OUTPUT
DIGITAL INPUT U4 U5
BOARD IDENTIFICATION
DIGITAL INPUT

Figure 5-46. Digital I/O Board Block Diagram

or tracking voltage. The Digital Output produces eight bits of digital output (write) that supplies a specific output bit or byte or tracking byte output. Digital Input reads a single bit or an entire byte which the multimeter can convert to various formats. Board Identification tells the instrument a Digital I/O board is installed.

5.7.2 Control

Control decodes information from the multimeter and enables each of the other blocks. Control, as shown in figure 5-47, consists of the Address Latch U2 and Address Decoder U1. Schematic 0103-00-1814 illustrates the Control block in greater detail.

The Address Latch U2 demultiplexes address lines (A0 and A1) from the multimeter's Address/Data bus using the Address Strobe (AS). A1 provides an input for the Address Decoder. A0 selects either of two inputs from the Digital Input block. The Address Latch U2 transfers addresses present at its inputs (AD1 and AD0) to its outputs when the address strobe (AS) line is high and latches these inputs on the negative going edge (↓) of AS; see figure 5-48 and table 5-15.

Table 5-15. Control

AD1 (U2-2)	AS (U2-13)	A1 (U2-16)
0	1	0
1	1	1
X	0	Q_0 (level of A1 before AS ↓ transition)

The Address Decoder U1 provides $\overline{RD}$ and $\overline{WR}$ lines to the other Digital I/O blocks. The decoder demultiplexes the three inputs (A1, R/$\overline{W}$, and ground) when the E clock is high and Board Enable ($BD_{(N)}$) is low; see figure 5-49 and table 5-16. The Y0 output enables the Digital Output, the Y1 output enables the Analog Output, and the Y2 output enables the Digital Input.

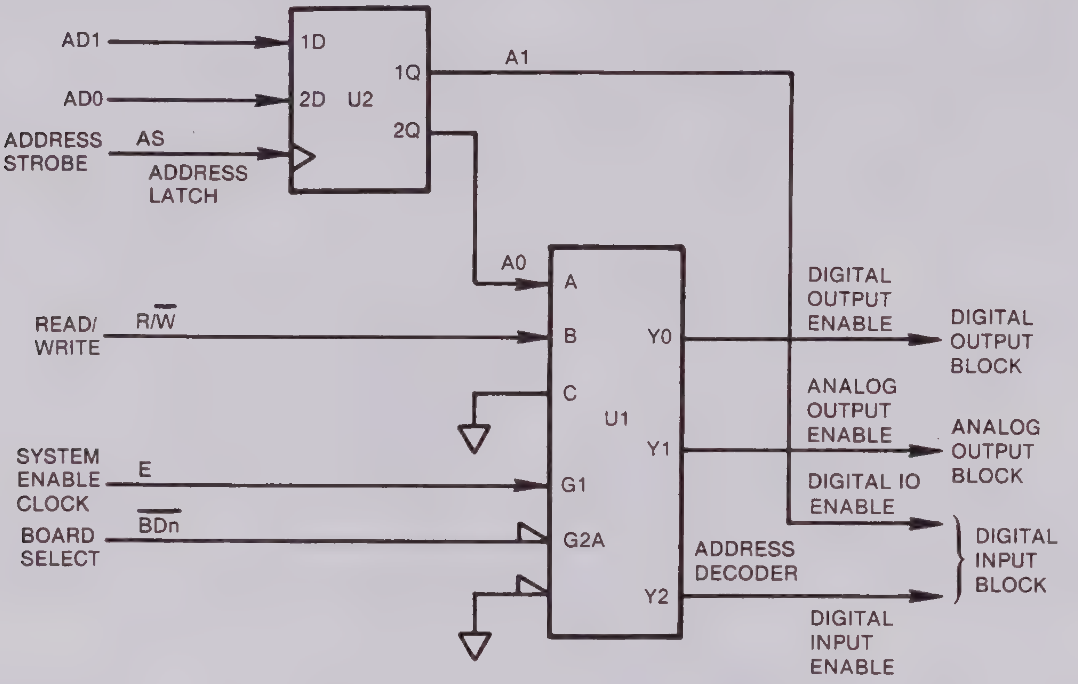

AD1
AD0
ADDRESS STROBE
AS
ADDRESS LATCH
1D
2D
U2
1Q
2Q
A1
A0
READ/ WRITE
$R/\overline{W}$
SYSTEM ENABLE CLOCK
E
BOARD SELECT
$\overline{BDn}$
A
B
C
G1
G2A
U1
Y0
Y1
Y2
ADDRESS DECODER
DIGITAL OUTPUT ENABLE
ANALOG OUTPUT ENABLE
DIGITAL IO ENABLE
DIGITAL INPUT ENABLE
DIGITAL OUTPUT BLOCK
ANALOG OUTPUT BLOCK
DIGITAL INPUT BLOCK

Figure 5-47. Control Block Diagram

5.7.3 Digital Output

Digital Output supplies the digital bit output or byte output to the Digital I/O connector. Digital Output consists of the Data Latch U3 and the output Field Effect Transistors (FETs) Q1 through Q8; see figure 5-50 and table 5-17. Table 5-17 shows only one output line; all other lines are functionally identical.

The Data Latch receives its data via the Address/Data lines AD0 – AD7 from the motherboard. The data at the inputs (U3 pins 3, 4, 7, 8, 13, 14, 17, 18) is latched when the digital latch line (U3 pin 11) returns high; see insert A of figure 5-50. The digital output remains unchanged until the next time the latch is clocked.

The "Q" output from the latch (1Q through 8Q) drives the gate of a FET. When the "Q" output goes low (0.1V maximum), the FET turns off to produce a logic high (1) output; see insert B of figure 5-50. When the "Q" output goes high (approximately 5V), the FET turns on to produce a logic low (0) output; see insert C of figure 5-50.

The open drain output can switch up to 50Vdc at 250mA. The outputs are lightly pulled up to +5Vdc through 100kΩ resistors.

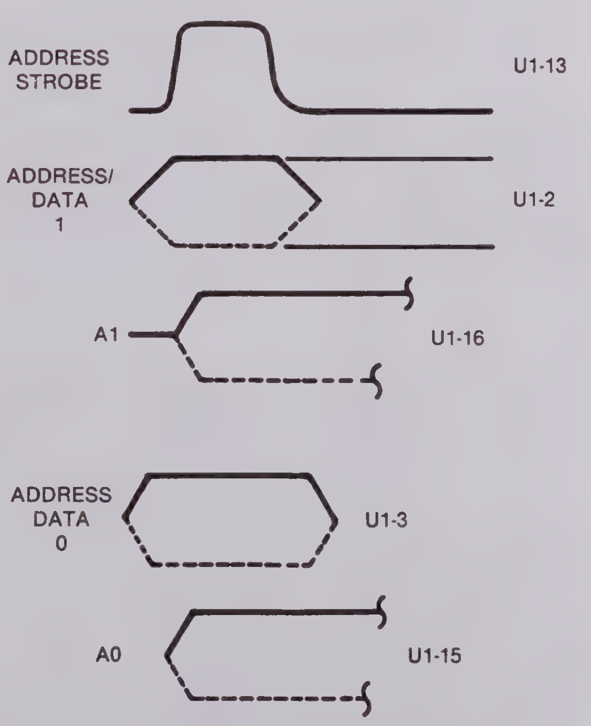

ADDRESS STROBE
U1-13
ADDRESS/ DATA 1
U1-2
A1
U1-16
ADDRESS DATA 0
U1-3
A0
U1-15

Figure 5-48. Latch Timing

Table 5-16. Decoder

Enable Inputs			Select Inputs			Outputs		
G1 (E)	**G2A (BDn)**	**G2B (Gnd)**	**C (Gnd)**	**B (R/W)**	**A (AD1)**	**Y0 (DigOut)**	**Y1 (AnaOut)**	**Y2 (DigIn)**
X	H	L	X	X	X	H	H	H
L	X	L	X	X	X	H	H	H
H	L	L	L	L	L	L	H	H
H	L	L	L	L	H	H	L	H
H	L	L	L	H	L	H	H	L

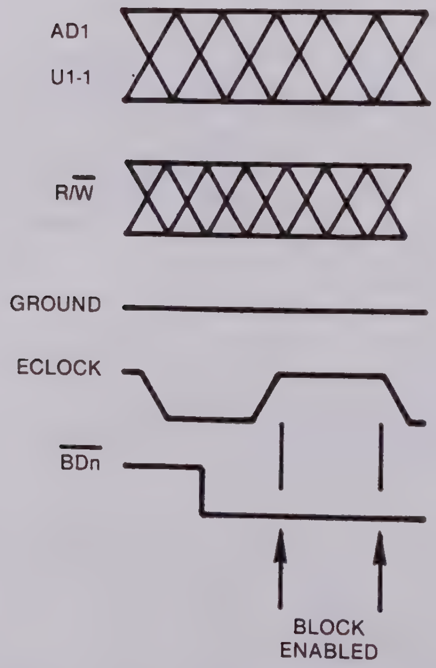


Figure 5-49. Decoder Timing

Table 5-17. Digital Output Logic

	Latch		FET		
CLK (U3 pin 11)	**AD Address/ Data Bus**	**Q Output**	**V_{GS}**	**Drain**	**State**
	Low (0V)	Low (0V)	0.1V max	+ 5V (High)	Off
	High 5V	High 5V	+ 4V (typ)	0.1V	On

5.7.4 Analog Output

The Analog Output produces an analog output voltage that can be set between 0.00V and + 2.55V with 0.01V resolution and represents a fixed value or proportional to a measurement module input.

The Analog Output U6 (see figure 5-51) is an eight-bit digital to analog converter (DAC) with voltage output. The DAC is enabled when the analog output enable line (U1 pin 14 – Y1) from the control block goes low. Once the DAC is enabled (see figure 5-52), each data line (AD0 through AD7) affects the DAC output. When the analog output enable line is high, the DAC output remains at the last value before it was latched. Table 5-18 gives several examples of the relationship between the data lines and the DAC output. The DAC is a positive true, binary weighted logic.

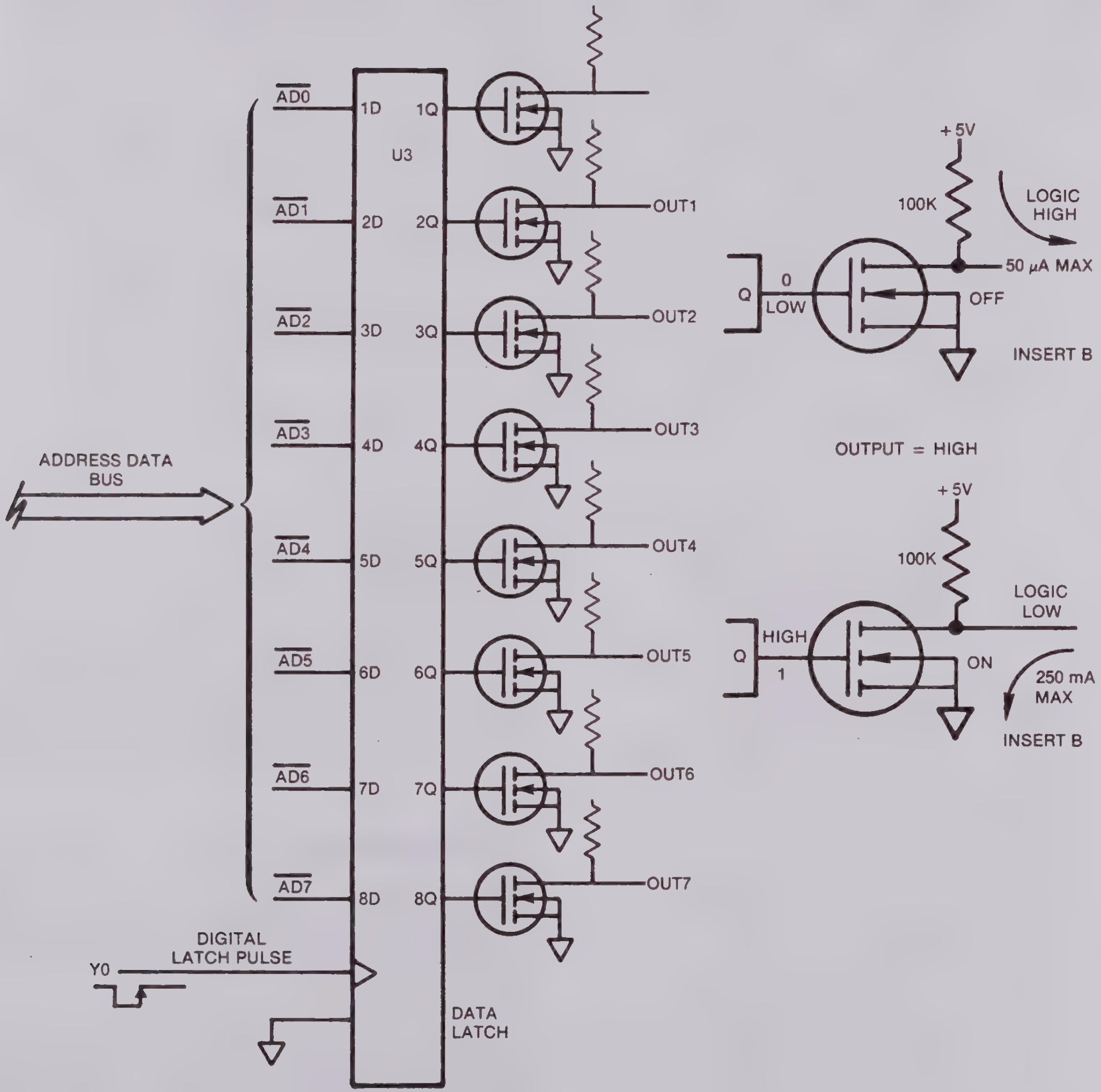

ADDRESS DATA BUS
$\overline{AD0}$
$\overline{AD1}$
$\overline{AD2}$
$\overline{AD3}$
$\overline{AD4}$
$\overline{AD5}$
$\overline{AD6}$
$\overline{AD7}$
1D
2D
3D
4D
5D
6D
7D
8D
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
U3
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
DIGITAL LATCH PULSE
Y0
DATA LATCH
+5V
100K
LOGIC HIGH
50 μA MAX
Q
0
LOW
OFF
INSERT B
OUTPUT = HIGH
+5V
100K
LOGIC LOW
HIGH
Q
1
ON
250 mA MAX
INSERT B

Figure 5-50. Digital Output

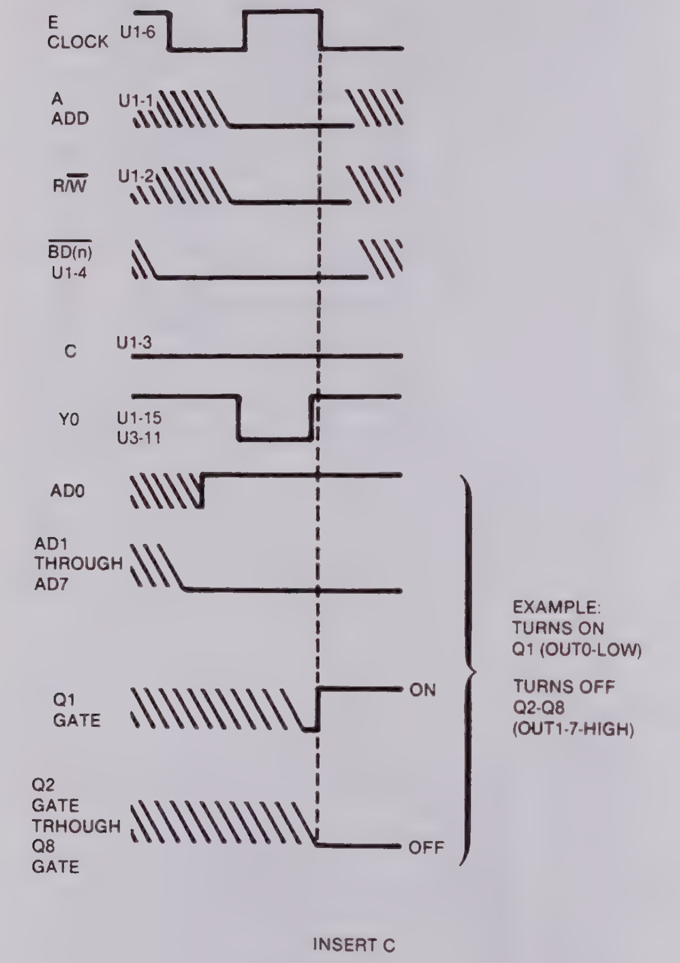

E CLOCK
U1-6
A ADD
U1-1
R/W
U1-2
BD(n) U1-4
C
U1-3
Y0
U1-15
U3-11
AD0
AD1 THROUGH AD7
Q1 GATE
ON
Q2 GATE TRHOUGH Q8 GATE
OFF
EXAMPLE: TURNS ON Q1 (OUT0-LOW)
TURNS OFF Q2-Q8 (OUT1-7-HIGH)
INSERT C

Figure 5-50a. Digital Output II

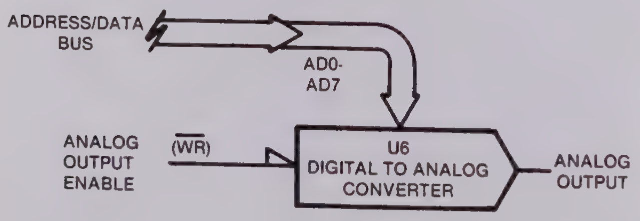

ADDRESS/DATA BUS
AD0-AD7
ANALOG OUTPUT ENABLE
(WR)
U6
DIGITAL TO ANALOG CONVERTER
ANALOG OUTPUT

Figure 5-51. Analog Output Block Diagram

5.7.5 Digital Input Block

The Digital Input reads eight bits at the Digital I/O connector. The multimeter can read an individual bit or all eight bits. The byte is read as a binary number and converted into user-selected formats.

Digital Input, figure 5-53, consists of two Data Selectors U4 and U5 that function as an eight-pole, double-throw switch. One "position" of the switch reads the input connections, and the other "position" supplies the multimeter with its board identification code (see paragraph 5.7.6).

To read the Digital Input connector, Control enables the Data Selector (U4 and U5, Enable goes low); see figure 5-54. Also, Control sets the A/B line high which allows the digital inputs to be read by the multimeter. Each digital input is pulled up through 100 kΩ resistors to the V+ supply. This allows the digital inputs to detect contact closures as inputs. In addition, digital inputs are protected by 100 kΩ flame proof resistors (R9 – R12 and R17 – R20) in series with each input. These resistors protect the inputs from excessive voltages. Figure 5-55 illustrates the conditions the multimeter recognizes as valid logic inputs.

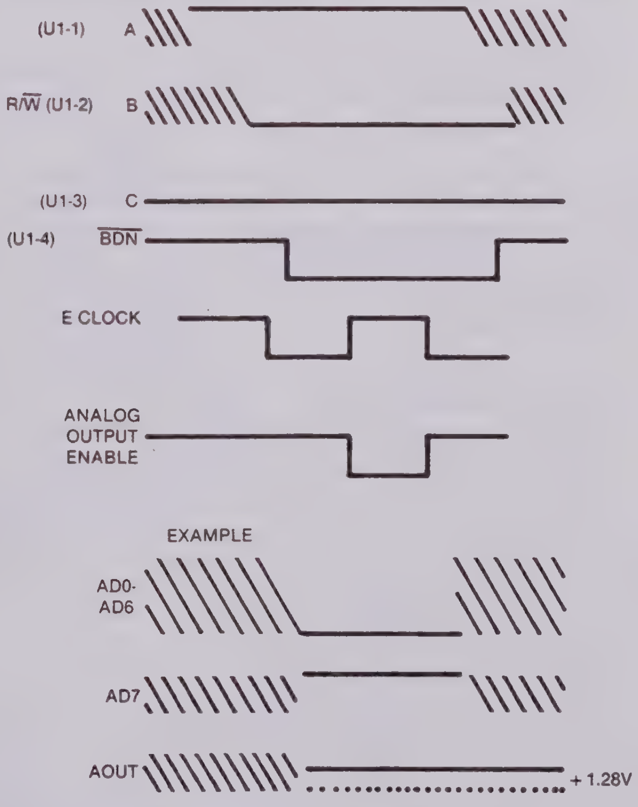

(U1-1) A
R/W (U1-2) B
(U1-3) C
(U1-4) BDN
E CLOCK
ANALOG OUTPUT ENABLE
EXAMPLE
AD0-AD6
AD7
AOUT
+1.28V

Figure 5-52. Analog Output Timing

Table 5-18. Analog Output Examples

Output Level U6-16	AD7 U6-8	AD6 U6-7	AD5 U6-6	AD4 U6-5	AD3 U6-4	AD2 U6-3	AD1 U6-2	AD0 U6-1
Weight	(1.28)	(.64)	(.32)	(.16)	(.08)	(.04)	(.02)	(.01)
0.00V	0	0	0	0	0	0	0	0
0.01V	0	0	0	0	0	0	0	1
0.02V	0	0	0	0	0	0	1	0
0.04V	0	0	0	0	0	1	0	0
0.08V	0	0	0	0	1	0	0	0
0.10V	0	0	0	0	1	0	1	0
1.00V	0	1	1	0	0	1	0	0
1.28V	1	0	0	0	0	0	0	0
1.53V	1	0	0	1	1	0	0	1
2.00V	1	1	0	0	1	0	0	0
2.55V	1	1	1	1	1	1	1	1

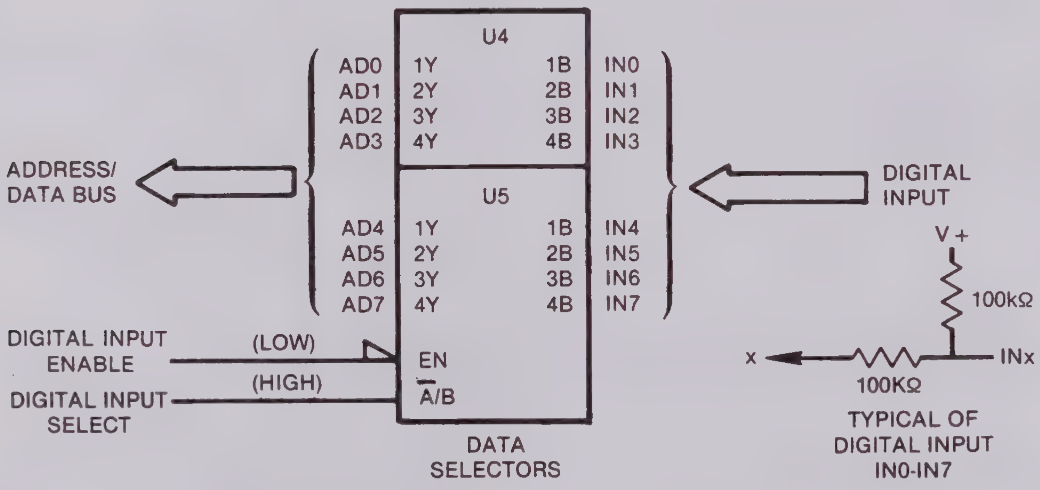

U4
AD0 1Y 1B IN0
AD1 2Y 2B IN1
AD2 3Y 3B IN2
AD3 4Y 4B IN3
ADDRESS/ DATA BUS
DIGITAL INPUT
U5
AD4 1Y 1B IN4
AD5 2Y 2B IN5
AD6 3Y 3B IN6
AD7 4Y 4B IN7
V+
100kΩ
DIGITAL INPUT ENABLE
(LOW)
EN
DIGITAL INPUT SELECT
(HIGH)
A/B
x
INx
100KΩ
TYPICAL OF DIGITAL INPUT IN0-IN7
DATA SELECTORS

Figure 5-53. Digital Input

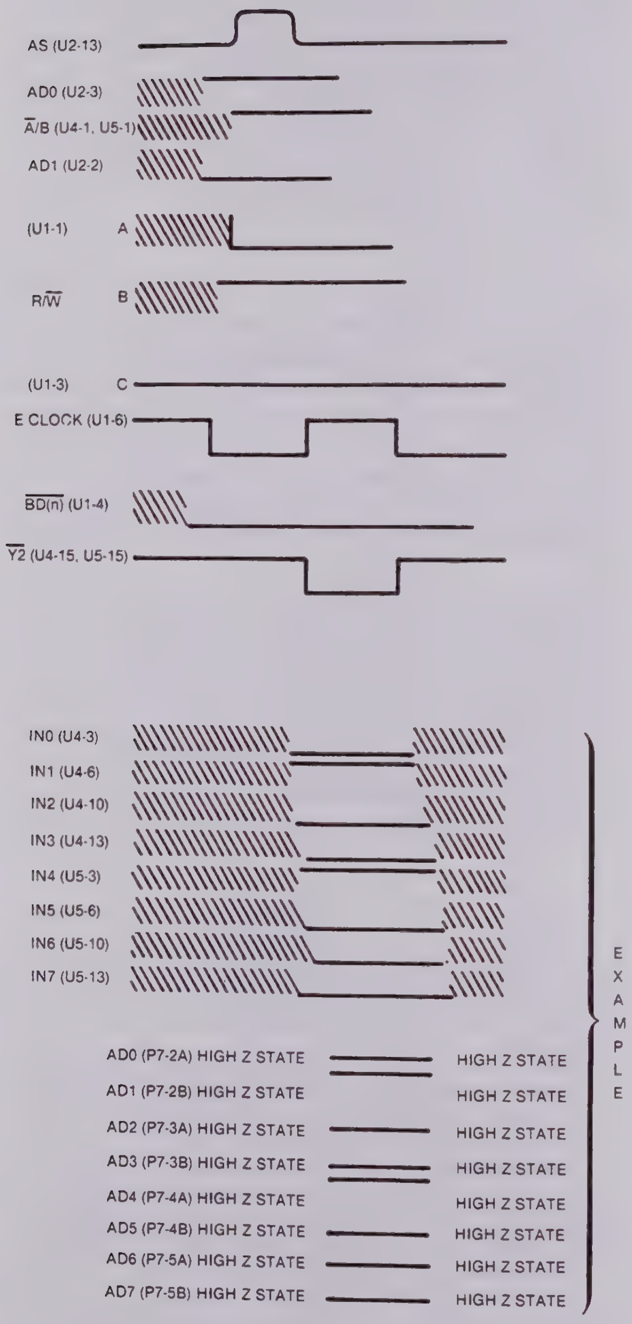

AS (U2-13)
AD0 (U2-3)
A/B (U4-1, U5-1)
AD1 (U2-2)
(U1-1)
A
R/W
B
(U1-3)
C
E CLOCK (U1-6)
BD(n) (U1-4)
Y2 (U4-15, U5-15)
IN0 (U4-3)
IN1 (U4-6)
IN2 (U4-10)
IN3 (U4-13)
IN4 (U5-3)
IN5 (U5-6)
IN6 (U5-10)
IN7 (U5-13)
AD0 (P7-2A) HIGH Z STATE
AD1 (P7-2B) HIGH Z STATE
AD2 (P7-3A) HIGH Z STATE
AD3 (P7-3B) HIGH Z STATE
AD4 (P7-4A) HIGH Z STATE
AD5 (P7-4B) HIGH Z STATE
AD6 (P7-5A) HIGH Z STATE
AD7 (P7-5B) HIGH Z STATE
HIGH Z STATE
HIGH Z STATE
HIGH Z STATE
HIGH Z STATE
HIGH Z STATE
HIGH Z STATE
HIGH Z STATE
HIGH Z STATE
EXAMPLE

Figure 5-54. Digital Input Timing

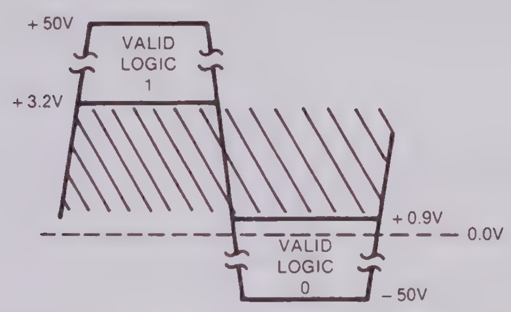

+50V
VALID LOGIC 1
+3.2V
+0.9V
0.0V
VALID LOGIC 0
-50V

Figure 5-55. Digital Input Logic Levels

Four separate inputs on the Digital I/O connector (EXT1 – EXT4) allow an external source to start and stop programs and stop time interval measurements. Each external trigger input is protected by 33 kΩ flame proof resistors (R25 – R28) in series with each input. The Digital I/O board does not process the external trigger but passes the trigger on to the multimeter (see figure 5-56).

5.7.6 Board Identification

Board Identification tells the multimeter a Digital I/O board is plugged into a specific option card connector. Board Identification is part of the DigitalInput U4 and U5 (paragraph 5.7.6). See figure 5-57.

To read the board identification code, the multimeter sets the data selector line low; see figure 5-58. Next, Control enables (Digital Input Enable: low) the Data Selectors. The Data Selectors place the fixed code ($0000\ 0001_{bin}$ or 01_H) on the multimeter's Address/Data bus (AD0 – AD1) which identifies the Digital I/O board.

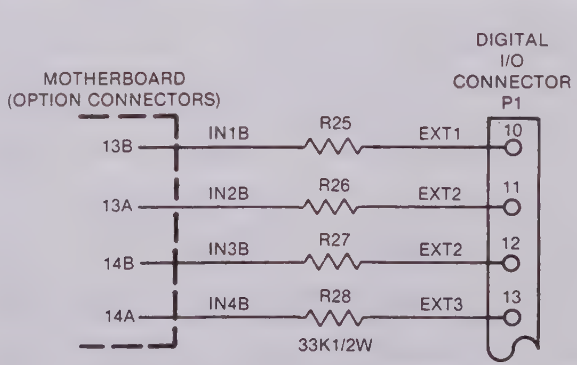

MOTHERBOARD (OPTION CONNECTORS)
DIGITAL I/O CONNECTOR P1
13B
13A
14B
14A
IN1B
IN2B
IN3B
IN4B
R25
R26
R27
R28
33K1/2W
EXT1
EXT2
EXT2
EXT3
10
11
12
13

Figure 5-56. External Trigger Input

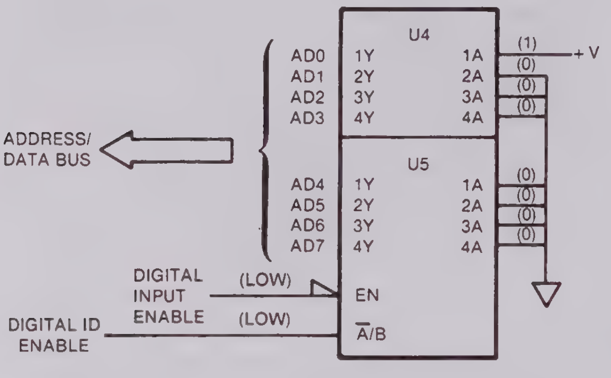

U4
AD0
AD1
AD2
AD3
1Y
2Y
3Y
4Y
1A
2A
3A
4A
(1)
(0)
(0)
(0)
+ V
ADDRESS/
DATA BUS
U5
AD4
AD5
AD6
AD7
1Y
2Y
3Y
4Y
1A
2A
3A
4A
(0)
(0)
(0)
(0)
DIGITAL
INPUT
ENABLE
(LOW)
EN
DIGITAL ID
ENABLE
(LOW)
$\overline{A}$/B

Figure 5-57. Board Identification Block

5.8 EXPANSION RAM BOARDS

5.8.1 Expansion RAM Overview

The 50-12 board has no backup battery on it, and no ROM. The 50-12A board has a backup battery, and a ROM socket in the U6 space. The 50-12 has four 64K memory modules. The 50-12A has two 128K memory modules. 50-12 users may skip paragraph 5.8.3. 50-12A users may skip paragraph 5.8.2. See also paragraphs 5.2.8.5.9 and 5.2.8.5.10, which deal with board-select address decoding, and plug-in socket bus buffering.

The motherboard memory map has an 8K space, or "window", from 24 to 32K, allotted for expansion RAM. Since an expansion RAM has several times 8K of memory on it, one block of 8K at a time is selected to be placed against this window, so the MPU can access a byte location. The motherboard uses an address in the HEX 0700's to pass the block select information to the expansion memory board. A term that is often used in place of block is "bank".

Each type of board has the same general architecture: there is circuitry for latching bank select data from the motherboard; latches for the address lines; and the RAMs.

5.8.2 50-12 Board

5.8.2.1 Bank Selection For The MPU 24-32K Window

During an initialization routine the software determines which slots have expansion memory, and how much.

See the RAM board schematic, drawing number 0103-00-1817.

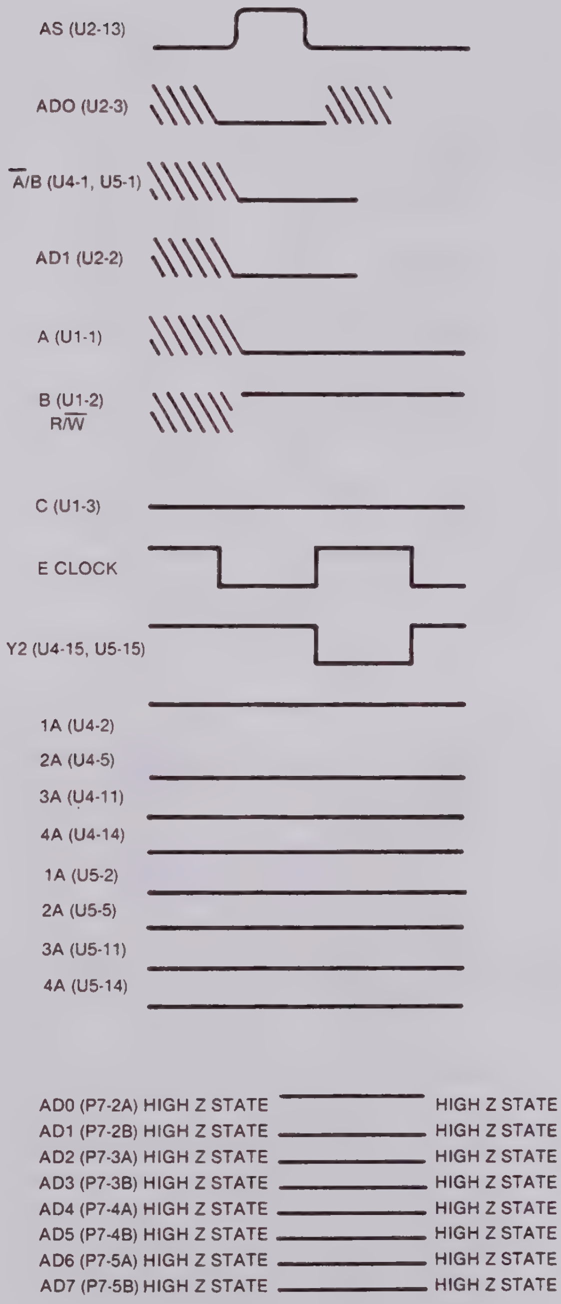


Figure 5-58. Board Identification Timing

Overview

Before the MPU can do an expansion RAM data read or write, it must ensure that the appropriate 8K block is accessible. So, the MPU sends out a partial data byte during the data portion of the E cycle, that is not data, but the bank selection specification. This partial data byte (AD0-AD5) is latched into RAM board IC U2, and contains the five bits (U2 pins 2, 5, 7, 12, and 15) required to specify which of the 32 blocks on a 256K board are to be accessible to the MPU.

The address the MPU uses for this step is in the HEX 0700's.

Board Selection

The MPU must ensure that this bank switching byte gets only to the appropriate board, since more than one RAM board may be installed. The exact address the MPU sends out for the bank switching step determines which RAM board will latch the bank switching data byte. See the motherboard schematic, sheet 2, zone B5. The $\overline{\text{BD(n)}}$ board-enable (which goes to board n) is generated by setting up an address 072X through 07AX (table 5-4).

The motherboard U24 address decoder IC feeds the correct plug-in board slot with the enabling pulse. On the motherboard, the enabling pulse names are that of the slot they go to: BD1 through BD5, with BD1 going to motherboard slot J7 (closest to the channel 1 measurement module area). On a RAM board, this pulse always comes in on the same pin number (1B), and is simply called BD(n), where (n) means the slot number from 1 to 5.

How is the "data" latched?

See the schematic of the RAM board. A BD(n) pulse is approximately 0.8 microseconds long. The low-active BD(n) pulse goes low soon after the start of the E cycle when the address lines are stabilized, and lasts through the end of the cycle. R/W\ is low during the cycle, because the MPU is doing a write. This makes U4-3 high.

At the midpoint of the cycle, E\ goes high, signifying the start of the data half of the cycle. The MPU puts the "data" on the AD0-AD5 lines. Buffered, these become AD0\-AD5\ to the RAM board.

U2 needs a positive edge on pin 9 (WR * E * BD(n)) in order to latch the data lines on its input. First, U1-10 must be made to go low. U1 is a 1-of-4 low output decoder. Which output is low depends on the combination on the A and B inputs. U1-15 is low-enabled on a bank-switching step. U4-4 and U1-13 are high from U4-3. On the first half of the cycle, U4-6 is high. On the second half of the cycle, U4-6 goes low, from both U4-4, and now U4-5, being high. So, U1-14 from U4-6 is low, and U1-13 is high. This combination causes the Y2 output of U1 to go low.

At the very end of the cycle, E\ goes low, causing U4-6 to instantly go high. With U1 pins 14 and 15 both high, this causes U1-9 to go low, and U1-10 to return high. This positive edge goes to U2-9 and latches the current state of the data lines from the MPU into RAM board IC U2. The positive edge happens before the AD0\-AD5\ lines have time to change state for the next MPU cycle. Now U2 contains the information to divide the board's memory up into modules, and each module up into 8K blocks.

What were **AD5** and **AD4** on the input of U2 become the information (via U1) to select which of the four 64K modules on a 256K board is selected. U1-Y0 active low enables the U5 module; Y1 active low enables the U6 module. Y2 active low enables the U7 module; Y3 active low enables the U8 module.

What was **AD3** on the input of U2 becomes a common memory protection bit that goes to all four memory modules.

What were **AD2**, **AD1**, and **AD0**, become A15, A14, and A13 to the modules on the expansion RAM board. These three lines contain the information to divide a 64K module into 8 banks of **8K each**.

U2 holds the bank selection indefinitely — until the MPU sends over a new bank selection.

The motherboard's A15, A14, and A13 are not used by expansion RAM boards.

5.8.2.2 Byte-level Decoding

The 24-32K (6000_H-$7FFF_H$) address space of the motherboard MPU is allotted for (the currently-switched-in) Bank (of) RAM. In this address space, A12-A0 decode the individual byte addresses. (Thirteen address lines can specify one location out of 8K.)

U3, an octal transparent latch, is the low-order address latch. Recall that the address from the motherboard MPU is on its bus only during the first half of a cycle. U3 latches this address pattern and stretches it until the end of a cycle. U3 buffers address information from input to output as soon as AS\ goes high, and remembers the bit states when AS\ goes low.

Now that A12\-A0\ are buffered and latched, they go to RAM modules U5, U6, U7, and U8.

5.8.2.3 Expansion RAM Reading And Writing

Assuming the appropriate bank selection data has been latched onto the RAM board, the 8K segment can be used.

MPU Write

Pin 2, WR, on a 64K module is low during the data time of a cycle, for a write from the MPU to the RAM. OE to the memory module stays high, keeping the RAM's output drivers off. Soon after the start of the data half of the cycle, the MPU puts the data on the bus. The data from the MPU is latched on the trailing (rising) edge of WR.

MPU Read

Pin 2, WR, on a 64K module stays high throughout a read cycle. OE to the memory module goes low during the data half of the cycle. OE low turns on the RAM's output drivers. The data to the MPU is latched by it on the trailing (falling) edge of its E clock.

The firmware program keeps track of which bank is currently switched in. At the time of the next write or read to the expansion RAM board, if it is in the same 8K bank, the MPU will not repeat the bank selection step.

5.8.2.4 Summary Of 5.8.2

Step 1 — Bank Select Information Transfer:

A. AD0-AD7 addresses are latched during the address latch part of the cycle. (Address needed by motherboard U24). BD(n) stabilizes at the RAM board. R/W is already stabilized at RAM board.

B. E clock pulse to RAM board goes high. **AD0 – AD7** data lines stabilize. The E down (↓) edge latches the AD0-AD7 data into U3 during the data part of the cycle. U3 and U1 decode this bank selection byte into the chip select and high order addressing lines needed to make the correct 8K memory segment accessible.

Step 2 — RAM Data Read or Write:

On some succeeding cycle, the MPU Writes or Reads directly to an address in the 8k block, using only A0 through A12.

5.8.3 50-12A Board

5.8.3.1 Bank Selection For The MPU 24-32K Window

During an initialization routine the software determines which slots have expansion memory, and how much.

See the RAM board schematic, drawing number 0103-00-2947.

Overview

Before the MPU can do an expansion RAM data read or write, it must ensure that the appropriate 8K block is accessible. So, the MPU sends out a partial data byte during the data portion of the E cycle, that is not data, but the bank selection specification. This partial data byte (AD0-AD5) is latched into RAM board IC U3, and contains the five bits (U3 pins 2, 5, 7, 12, and 15) required to specify which of the 32 blocks on a 256K board are to be accessible to the MPU.

The address the MPU uses for this step is in the HEX 0700's.

Board Selection

The MPU must ensure that this bank switching byte gets only to the appropriate board, since more than one RAM board may be installed. The exact address the MPU sends out for the bank switching step determines which RAM board will latch the bank switching data byte. See the motherboard schematic, sheet 2, zone B5. The BD(n) board-enable (which goes to board n) is generated by setting up an address 072X through 07AX (table 5-3 in paragraph 5.2.8.5.9).

The motherboard U24 address decoder IC feeds the correct plug-in board slot with the enabling pulse. On the motherboard, the enabling pulse names are that of the slot they go to: BD1 through BD5, with BD1 going to motherboard slot J7 (closest to the channel 1 measurement module area). On a RAM board, this pulse always comes in on the same pin number (1B), and is simply called BD(n), where (n) means the slot number from 1 to 5.

How is the "data" latched?

See the schematic of the RAM board. A BD(n) pulse is approximately 0.8 microseconds long. The low-active BD(n) pulse goes low soon after the start of the E cycle when the address lines are stabilized, and lasts through the end of the cycle. R/W\ is low during the cycle, because the MPU is doing a write. This makes U2-3 high.

At the midpoint of the cycle, E\ goes high, signifying the start of the data half of the cycle. The MPU puts the "data" on the AD0\-AD5\ lines. Buffered, these become AD0-AD5 to the RAM board.

U3 needs a positive edge on pin 9 (WR*BDN) in order to latch the data lines on its input. First, U1-10 must be made to go low. U1 is a 1-of-4 low output decoder. Which output is low depends on the combination on the A and B inputs. U1-15 is low-enabled on a bank-switching step. U2-4 and U1-13 are high from U2-3. On the first half of the cycle, U2-6 is high. On the second half of the cycle, U2-6 goes low, from both U2-4, and now U2-5, being high. So, U1-14 from U2-6 is low, and U1-13 is high. This combination causes the Y2 output of U1 to go low.

At the very end of the cycle, E\ goes low, causing U2-6 to instantly go high. With U1 pins 14 and 15 both high, this causes U1-9 to go low, and U1-10 to return high. This positive edge goes to U3-9 and latches the current state of the data lines from the MPU into RAM board U3. The positive edge happens before the AD0\-AD5\ lines have time to change state for the next MPU cycle. Now U3 contains the information to divide the board's memory up into modules, and each module up into 8K blocks.

What were **AD5** and **AD3** on the input of U3 become the information (via U1) to select which of the two 128K modules on a 256K board is selected. CS1 active low enables the U7 module; CS2 active low enables the U8 module . (If MEMPROT is low, U1-4 or U1-5 are active, causing non-existent modules to be selected. MEMPROT means MEMory-PROTect.)

What were **AD4**, **AD2**, **AD1**, and **AD0**, become A16, A15, A14, and A13 to the modules on the expansion RAM board. These four lines contain the information to divide a 128K module into 16 banks of **8K each**. This holds true despite the fact that the physical division is four 32K chips on a module.

U3 holds the bank selection indefinitely — until the MPU sends over a new bank selection.

The motherboard's A15, A14, and A13 are not used by expansion RAM boards.

5.8.3.2 Byte-level Decoding

RAM

The 24-32K (6000_H-$7FFF_H$) address space of the motherboard MPU is allotted for (the currently-switched-in) Bank (of) RAM. In this address space, A12-A0 decode the individual byte addresses. (Thirteen address lines can specify one location out of 8K.)

U5, an octal transparent latch, is the low-order address latch. Recall that the address from the motherboard MPU is on its bus only during the first half of a cycle. U5 latches this address pattern and stretches it until the end of a cycle. U5 buffers address information from input to output as soon as AS\ goes high, and remembers the bit states when AS\ goes low.

U4 is a hex D flip-flop. Its purpose here is that of a buffer. U4 latches the A12\-A8\ address information on the trailing (falling) edge of AS. AS\ (U2-10) is just a buffered version of AS. U2 inverts the signal.

Now that A12*-A0\ are buffered and latched, they go to RAM modules U7 and U8, and ROM U6 if installed.

ROM

The U6 expansion ROM (if installed) on the RAM board uses the same A12*-A0\ lines as the RAM modules. However, this expansion ROM has only a 6K window to the MPU (the addresses from 2K to 8K in the motherboard memory map). The lowest 2K is unused.

5.8.3.3 Expansion RAM Reading And Writing

Assuming the appropriate bank selection data has been latched onto the RAM board, the 8K segment can be used.

MPU Write

Pin 29, WR, on a 128K module is low during the data time of a cycle, for a write from the MPU to the RAM. OE to the memory module stays high, keeping the RAM's output drivers off. Soon after the start of the data half of the cycle, the MPU puts the data on the bus. The data from the MPU is latched on the trailing (rising) edge of WR.

MPU Read

Pin 29, WR, on a 128K module stays high throughout a read cycle. OE to the memory module goes low during the data half of the cycle. OE low turns on the RAM's output drivers. The data to the MPU is latched by it on the trailing (falling) edge of its E clock.

The firmware program keeps track of which bank is currently switched in. At the time of the next write or read to the expansion RAM board, if it is in the same 8K bank, the MPU will not repeat the bank selection step.

5.8.3.4 Summary Of 5.8.3

Step 1 — Bank Select Information Transfer:

A. AD0-AD7 addresses are latched during the address latch part of the cycle. (Address needed by motherboard U24). BD(n) stabilizes at the RAM board. R/W is already stabilized at RAM board.

B. E clock pulse to RAM board goes high. **AD0-AD7** data lines stabilize. The E down (↓) edge latches the AD0-AD7 data into U3 during the data part of the cycle. U3 and U1 decode this bank selection byte into the chip select and high order addressing lines needed to make the correct 8K memory segment accessible.

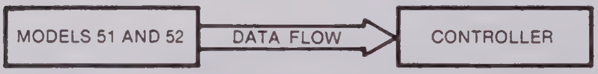
Step 2 — RAM Data Read or Write:

On some succeeding cycle, the MPU Writes or Reads directly to an address in the 8k block, using only A0 through A12.

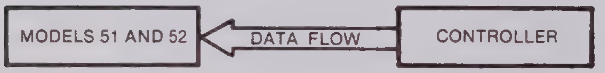
5.9 THE GENERAL PURPOSE INTERFACE BUS (GPIB)

5.9.1 The Bus

The General Purpose Interface Bus (GPIB), the implementation of the IEEE-488 (1978) standard, is a bit-parallel, byte-serial bus that communicates data between the Model 51 or 52 and the controller. A GPIB bus controller orchestrates the role of Models 51 and 52 by addressing them as talkers or listeners and controlling the transfer of data. The Models 51 and 52 function as talkers when they transmit measurements and as listeners when they receive commands and setup data; see figure 5-59.



MODELS 51 AND 52 AS A TALKER



MODELS 51 AND 52 AS A LISTENER

Figure 5-59. Talker/Listener

5.9.1.1 The Bus Lines

The bus lines provide the communications route between the the Models 51 and 52 and the controller. The GPIB bus (see figure 5-60) contains data bus lines, data transfer control (handshaking) lines, and interface management lines.

The eight bidirectional data bus lines (DIO1 through DIO8) transfer data, addresses, commands, and status bytes. Data is transferred a byte at a time until all the data is transferred.

The three data transfer control lines (NRFD, DAV, and NDAC) control the data flow (handshaking) over the bus to the instruments.

Listeners use the "Not Ready For Data" (NRFD) line to signal the talkers it is unable to receive data.

Talkers use the "Data Available" (DAV) line to signal the listener that valid data is on the bus.

Listeners use the "No Data Accepted" (NDAC) line to signal the talker data has not been accepted.

The five interface management lines (EOI, SRQ, REN, IFC, and ATN) control the orderly flow of data between the controller and the instrument.

The Attention (ATN) line, which originate from the controller, signals the instruments on the bus the controller is sending address or universal commands (ATN: low) or data (ATN: high).

The Interface Clear (IFC) line from the controller places all the units on the bus to a predefined state.

The Service Request (SRQ) line signals the controller an instrument on the bus needs attention. When an instrument asserts (low) the SRQ line, the controller polls all units on the bus to determine who needs service.

The Remote Enable (REN) line from the controller inhibits the instruments front panel keys; this means only the controller can run the instrument.

The End Or Identify (EOI) line from any talker tells the listener it has finished the data transfer.

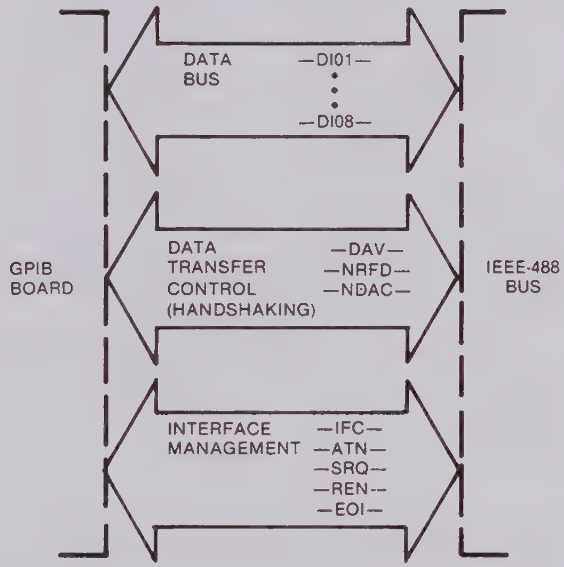


Figure 5-60. GPIB Bus Lines

5.9.1.2 The Models 51 and 52 as a Talker

When the controller wants the Models 51 and 52 to talk, the controller must assert (low) the attention (ATN) line telling the Models 51 and 52 a talker address is on the data bus. The talker address will be in the form X 1 0 A5 A4 A3 A2 A1; where X indicates an ignored bit and A5, A4, A3, A2, and A1 are the Models 51 and 52 GPIB address. This routine places the multimeter in the talker mode. The following list describes the talker sequence; the number in the list refer to the circled items in figure 5-61.

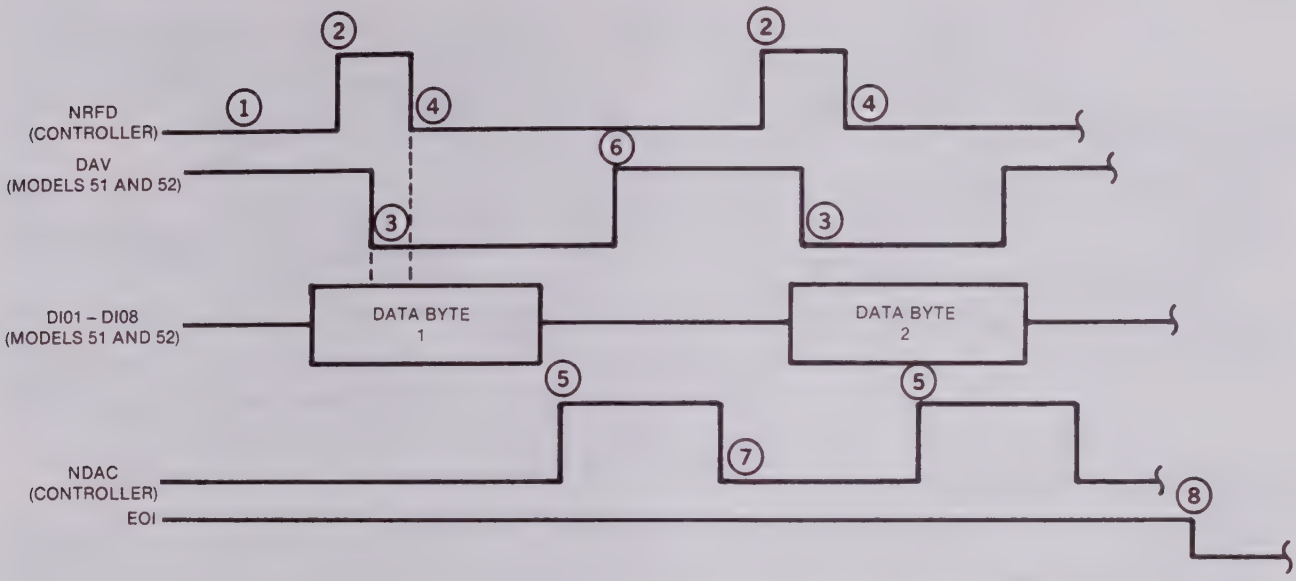


Figure 5-61. Talker Timing

1. The controller (listener) holds the NRFD line low to indicate the controller is not ready to receive data.
2. The controller releases (high) the NRFD line telling the Models 51 and 52 it can send data.
3. The Models 51 and 52 assert (low) the DAV line to tell the controller the bus contains valid data.
4. The controller pulls the NRFD line low and starts accepting the data.
5. When all the data has been accepted by the controller, the controller unasserts (high) the NDAC line telling the Model 51 or 52 the controller has received all the data byte.
6. The Models 51 and 52 senses a high on the NDAC line and unasserts (high) the DAV line.
7. Then, the controller asserts the NDAC line once again repeating the sequence until all the data bytes are sent.
8. When the Model 51 or 52 completes the data bytes transfer sequence, the Model 51 or 52 pulls the EOI line low telling the controller all the data has been sent.
9. Finally, the controller asserts the ATN line (low) and sends an untalk command: X 1 0 1 1 1 1 1 (X means the Model 51 or 52 ignores that bit).

5.9.1.3 The Models 51 and 52 As A Listener

When the controller wants the Model 51 or 52 to listen, the controller asserts (low) the attention ATN line telling the Model 51 or 52 a listen address is on the data bus. A listener address will be in the form X 0 1 A5 A4 A3 A2 A1; where X means an ignored bit and A5, A4, A3, A2, and A1 represents the address bits. This sequence places the multimeter in the listener mode. The following list describes the talker sequence; the numbers in the list refer to the circled items in figure 5-62.

1. The Models 51 and 52 hold the NRFD line low to indicate the Models 51 and 52 are not ready to receive data.
2. The Models 51 and 52 release (high) the NRFD line telling the controller to send data.
3. The controller asserts (low) the DAV line to tell the Model 51 or 52 the bus contains valid data.
4. The Models 51 and 52 pulls the NRFD line low and starts accepting the data.
5. When all the data has been accepted by the Models 51 and 52, they unassert (high) the NDAC line telling the controller they received the data byte.
6. The Models 51 and 52 senses a high on the NDAC line and unasserts (high) the DAV line.

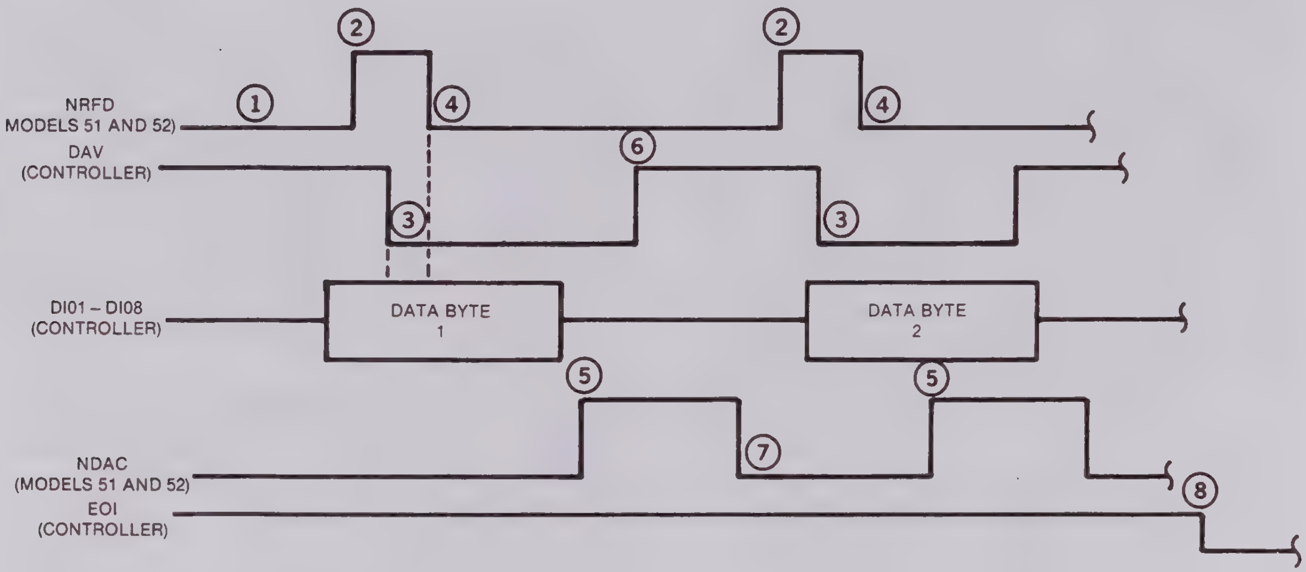


Figure 5-62. Listener Timing

7. Then, the controller asserts the NDAC line once again repeating the sequence until all the data bytes are sent.
8. When the controller completes the data bytes transfer sequence, the controller pulls the EOI line low which tells the Models 51 and 52 all the data has been sent.
9. Finally, the controller asserts the ATN line (low) and sends an untalk command (X 1 0 1 1 1 1 1, where X means an ignored bit).

5.9.1.4 The Service Request and the Models 51 and 52

Service request allows a unit on the bus to signal the control the unit needs to talk to the controller. Units on the bus use a single, common service request SRQ line (one of the Interface Management lines) to signal the controller. The Model 51 or 52 will assert the SRQ line only when they have an error message or data transmission.

When the controller detects an asserted line, the controller must poll all the units on the bus. If the Model 51 or 52 did not request service, they respond with 00_H when polled. However, if the Model 51 or 52 did request service, they respond with 41_H when polled. To read the actual message, the controller must address the Model 51 or 52 as a talker (see paragraph 5.9.1.2). If the controller does not read the message within five seconds, the Model 51 or 52 will reassert the SRQ line, repeating the sequence until the message is read by the controller. Servicing the service request does not cancel the SRQ line. To cancel the SRQ line, the multimeter must be addressed as a talker to cancel the SRQ assertion.

5.9.2 The General Purpose Interface Bus (GPIB) Board

The General Purpose Interface Bus (GPIB) board (Option 50-13) controls the data transfer and handling between the Model 51 or 52 and GPIB controller. Data is transfered over the GPIB using the sequence defined by the IEEE-488 standard (see paragraph 5.9.1).

The GPIB board (see figure 5-63) consists of the General Purpose Interface Adapter (GPIA) U7, the GPIB Transceivers U8 and U9, Buffer U3 and U2, the GPIB Address Switch and Board Identification U6 and S1, GPIA Transceiver U5, and Power Initializer U1B, U1C, U1A, Q1.

How The Board Works

The following paragraphs describe the simplified operating sequence of the GPIB board. Paragraphs 5.9.1.7 describe the data transfer sequence between the Model 51 or 52 and the controller. In reality, that transfer

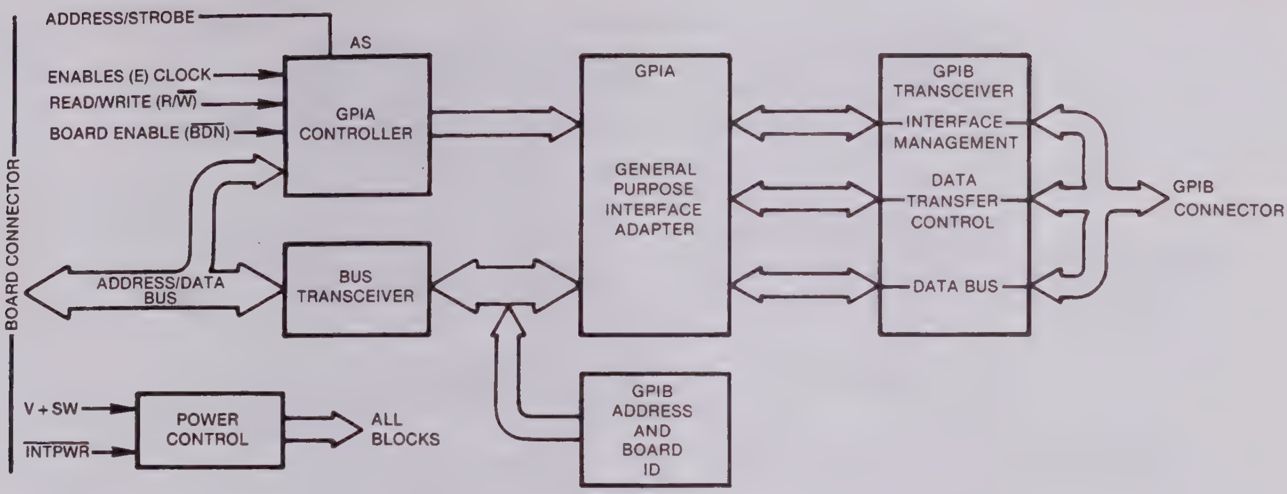


Figure 5-63. GPIB Board Block Diagram

sequence takes place between the GPIA and GPIB controller.

Power On — The GPIB board can operate only when the multimeter is connected to an external power source ($\overline{INTPWR}$ — high) and when the rear panel DIP switch is set to IEEE On (V+SW). At power on the Power Initializer provides power (IEEEV+) to the GPIA, GPIB Transceiver, GPIB Address Switch and Board Identification; enables the GPIA Transceiver and Buffer; and resets the GPIA. Right after power on, the multimeter enables the GPIB board and reads the GPIB address and board identification code.

Approximately every 25 ms, the multimeter enables the GPIB board ($\overline{BD}_{(N)}$ goes Low) and checks the GPIB board status. If the Model 51 or 52 needs to talk (error messages or data) to the controller, it will assert the SRQ line and the controller must use the SRQ/Talker sequence to read the message (paragraph 5.9.1.4). When the controller addresses the multimeter to talk, the multimeter will send the entire message, interrupting the measurements.

If the controller needs to talk to the Model 51 or 52, the controller address the Model 51 or 52 as a listener (paragraph 5.9.1.3) and sends the first byte which the GPIA stores in its internal register. When the multimeter enables the GPIB board ($\overline{BD}_{(N)}$ goes low), it reads the stored byte and transfers the byte on to the multimeter. The GPIA can now accept another byte and the multimeter reads the next byte when it enables the GPIB board. This sequence continues until the controller sends a termination character. All characters sent to the multimeter are executed as a group.

5.9.2.1 General Purpose Interface Adapter

The General Purpose Interface Adapter (GPIA) U7 handles the data transfer and bus protocol between the multimeter and the GPIB controller; refer to figure 5-64. The GPIA contains a data input register, a data output register and control registers by strobing the three least significant address lines AD0, AD1, and AD2 which drives the GPIA's register select lines RS0, RS1, and RS2 (U7 pins 37, 38, and 39). These registers contain information that is transferred between the registers and the multimeter via the GPIA's data bus DB0 through DB7 (U7 pins 7 through 14). The GPIA is enabled when the chip enable (CS) line (derived from the board enable BD(n) line) goes low. The microprocessor's E clock (1.2288MHz) synchronizes the data transfer between the GPIA and multimeter. The Read/Write control line (R/W) controls register access and data flow between the multimeter and GPIA; a Read (high) sends data from one of the eight GPIA internal read only registers to the multimeter, and a Write (low) sends data from the multimeter to one of seven GPIA internal write only registers.

The GPIA's RS488 (reset) line U7 pin 19 forces the GPIA into a reset condition. The RS488 line is normally high except for a short time when power is first turned on, when the power is shut off, and if the external power source is disconnected or drops too low. Resetting the GPIA resets the Interrupt Mask register, Status Condition, and Parallel and Serial Poll register, Data In and Data Out registers. Also, it resets the stored conditions in the Auxiliary Command register, places the device in Untalk/Unlisten states, clears the Address and Address

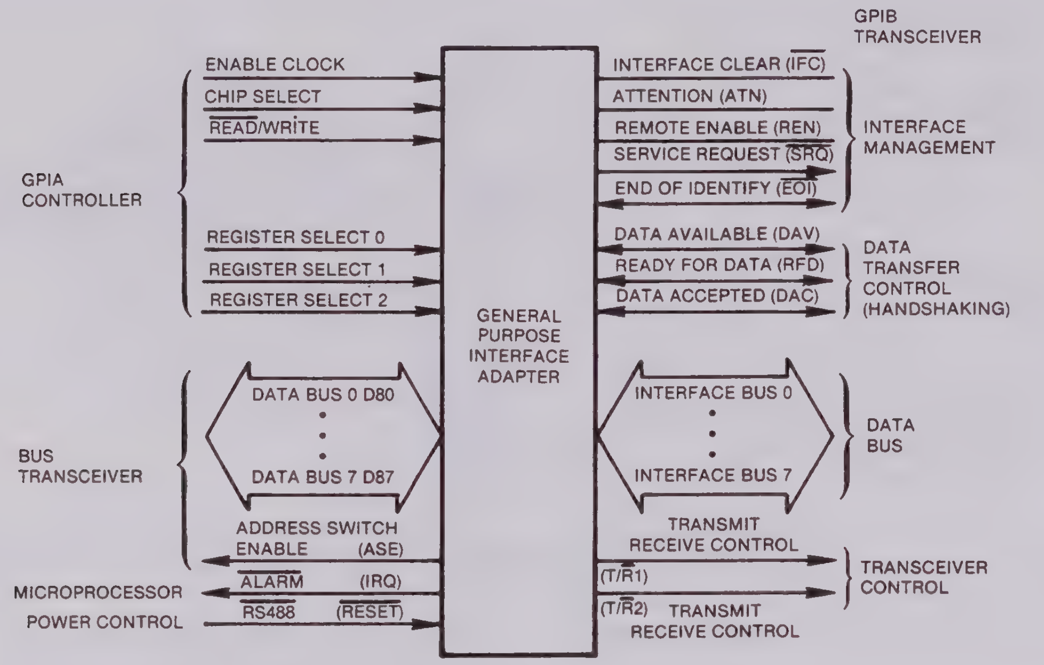

GPIB TRANSCEIVER
ENABLE CLOCK
CHIP SELECT
READ/WRITE
GPIA CONTROLLER
REGISTER SELECT 0
REGISTER SELECT 1
REGISTER SELECT 2
INTERFACE CLEAR (IFC)
ATTENTION (ATN)
REMOTE ENABLE (REN)
SERVICE REQUEST (SRQ)
END OF IDENTIFY (EOI)
INTERFACE MANAGEMENT
DATA AVAILABLE (DAV)
READY FOR DATA (RFD)
DATA ACCEPTED (DAC)
DATA TRANSFER CONTROL (HANDSHAKING)
GENERAL PURPOSE INTERFACE ADAPTER
DATA BUS 0 D80
DATA BUS 7 D87
BUS TRANSCEIVER
INTERFACE BUS 0
INTERFACE BUS 7
DATA BUS
ADDRESS SWITCH ENABLE (ASE)
ALARM (IRQ)
MICROPROCESSOR
RS488 (RESET)
POWER CONTROL
TRANSMIT RECEIVE CONTROL
(T/R1)
(T/R2) TRANSMIT RECEIVE CONTROL
TRANSCEIVER CONTROL

Figure 5-64. General Purpose Interface Adapter

Mode registers, plus forces low the Transmit/Receive T/R1 and T/R2 lines.

The GPIB bus lines from the GPIA (shown on the right side in figure 5-64) are controlled by the GPIB Transceivers. Paragraph 5.9.1 describes the function of these lines. Two lines T/R1 and T/R2 (Transmit/Receive Control) from the GPIA select the direction of data flow through the GPIB Transceivers.

5.9.2.2 GPIB Transceiver

The GPIB Transceivers U8 and U9 (see figure 5-65) provide the high current driving capability and line terminations required to drive the GPIB lines. In addition, they control the flow of data between the GPIA and the GPIB controller. The GPIA Transceiver is bidirectional depending on the GPIB mode: talker or listener. The transceiver transmits during the talk mode and receives during the listen mode (see insert in figure 5-65). The direction of data flow is controlled by switching different buffers in the transceiver. Some portions of the transceiver are hardwired to transmit while others are hardwired to receive in both modes. The GPIB Transceiver lines are actually divided between two separate transceivers; for simplification of data and command flow figure 5-65 shows the transceiver as one device.

Transceiver Direction Control

The direction of data flow through the transceiver is controlled by the two transmit/receive T/R2 and T/R1 lines from the GPIA.

The T/R2 line controls the direction of data flow for the data lines (DI0 – DI07) between the GPIA and the GPIB controller. When T/R2 is low, the GPIA receives data from the GPIB controller. When T/R2 is high, the GPIA sends data to the GPIB controller. T/R2 also controls the data flow direction for the Data Transfer Control lines DAV, NRFD, and NDAC; see table 5-19.

Table 5-19. DAV, NRFD, NDAC Control

	T/R2 Line	
	High	**Low**
DAV	GPIA←Controller	GPIA→Controller
NRFD	GPIA→Controller	GPIA←Controller
NDAC	GPIA→Controller	GPIA←Controller

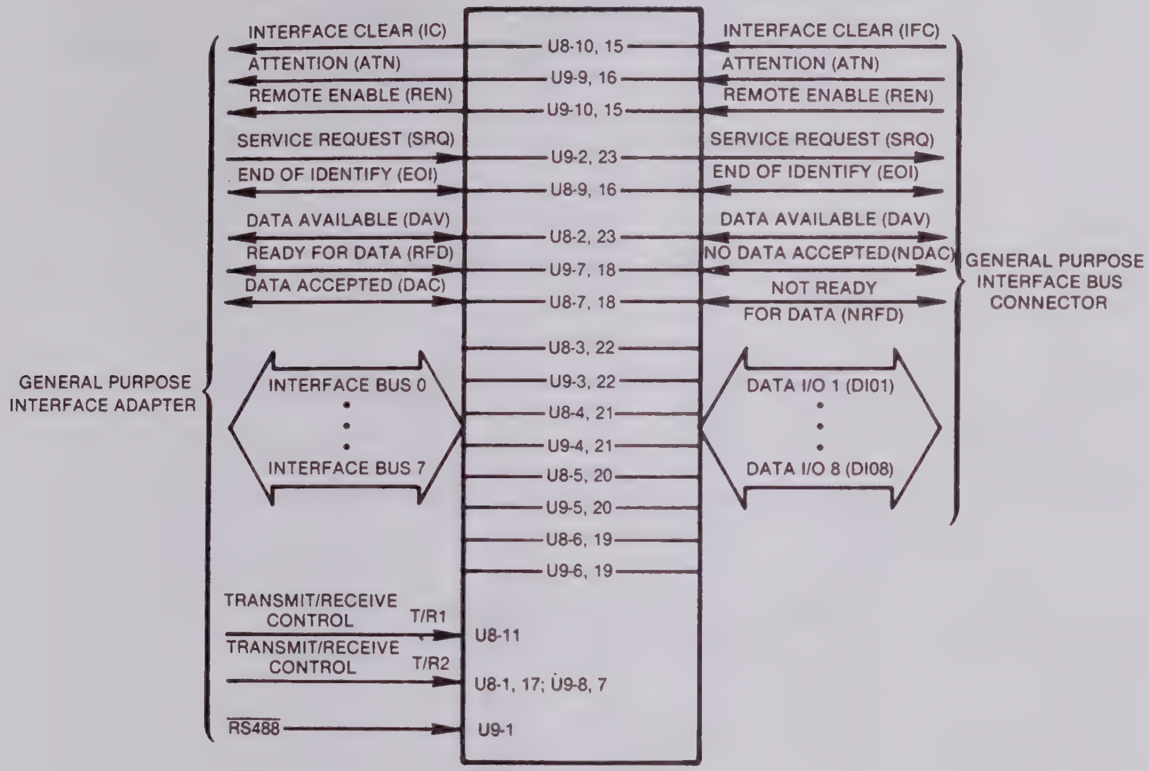

INTERFACE CLEAR (IC)
ATTENTION (ATN)
REMOTE ENABLE (REN)
SERVICE REQUEST (SRQ)
END OF IDENTIFY (EOI)
DATA AVAILABLE (DAV)
READY FOR DATA (RFD)
DATA ACCEPTED (DAC)
GENERAL PURPOSE INTERFACE ADAPTER
INTERFACE BUS 0
INTERFACE BUS 7
TRANSMIT/RECEIVE CONTROL T/R1
TRANSMIT/RECEIVE CONTROL T/R2
RS488
U8-10, 15
U9-9, 16
U9-10, 15
U9-2, 23
U8-9, 16
U8-2, 23
U9-7, 18
U8-7, 18
U8-3, 22
U9-3, 22
U8-4, 21
U9-4, 21
U8-5, 20
U9-5, 20
U8-6, 19
U9-6, 19
U8-11
U8-1, 17; U9-8, 7
U9-1
INTERFACE CLEAR (IFC)
ATTENTION (ATN)
REMOTE ENABLE (REN)
SERVICE REQUEST (SRQ)
END OF IDENTIFY (EOI)
DATA AVAILABLE (DAV)
NO DATA ACCEPTED(NDAC)
NOT READY FOR DATA (NRFD)
DATA I/O 1 (DI01)
DATA I/O 8 (DI08)
GENERAL PURPOSE INTERFACE BUS CONNECTOR

Figure 5-65. GPIB Transceiver

The T/R1 line controls a single transceiver line — End of Identify (EOI). When T/R1 is low, the GPIA receives a EOI from the controller. When T/R1 is high the GPIA sends an EOI to the controller.

Several lines, Interface Clear (IFC), Attention (ATN), and Remote Enable (REN) are hardwired to receive.

The SRQ line normally sends a SRQ generated by the GPIA to the GPIB controller, however when the RS488 line goes low, the GPIA could receive an SRQ from the controller.

5.9.2.3 GPIB Address Switch and Board Identification

The GPIB Address Switch and Board Identification circuit (see figure 5-66) allows the setting the Model 51 or 52's GPIB address. This circuit also identifies to the multimeter the board type. The actual circuit consists of an address switch S1 and tristate line driver U6.

The address switch S1 sets up the GPIB address. Valid addresses are the binary equivalent of the decimal numbers 0 through 30. The GPIB address forms the five lower order bits of the address/Identification byte. The three higher order bits are hardwired as 1 1 0 to three driver inputs. Together this byte looks like 0 1 1 A5 A4 A3 A2 A1; where A5 through A1 represent the GPIB address.

To read the address/Identification byte, the GPIA enables the line drivers by setting it's ASE line low when the multimeter sends to the GPIB board the following pattern:

AD0 0
AD1 0
AD2 1
R/W 1
$BD_{(N)}$ 0

This pattern selects the address switch register R4R of the GPIA which forces the ASE line low for one cycle of the E clock. The multimeter reads the GPIB address at power up.

5.9.2.4 GPIA Transceiver

The GPIA Transceiver (see figure 5-67) controls the data flow between the multimeter and the GPIA U7. This cir-

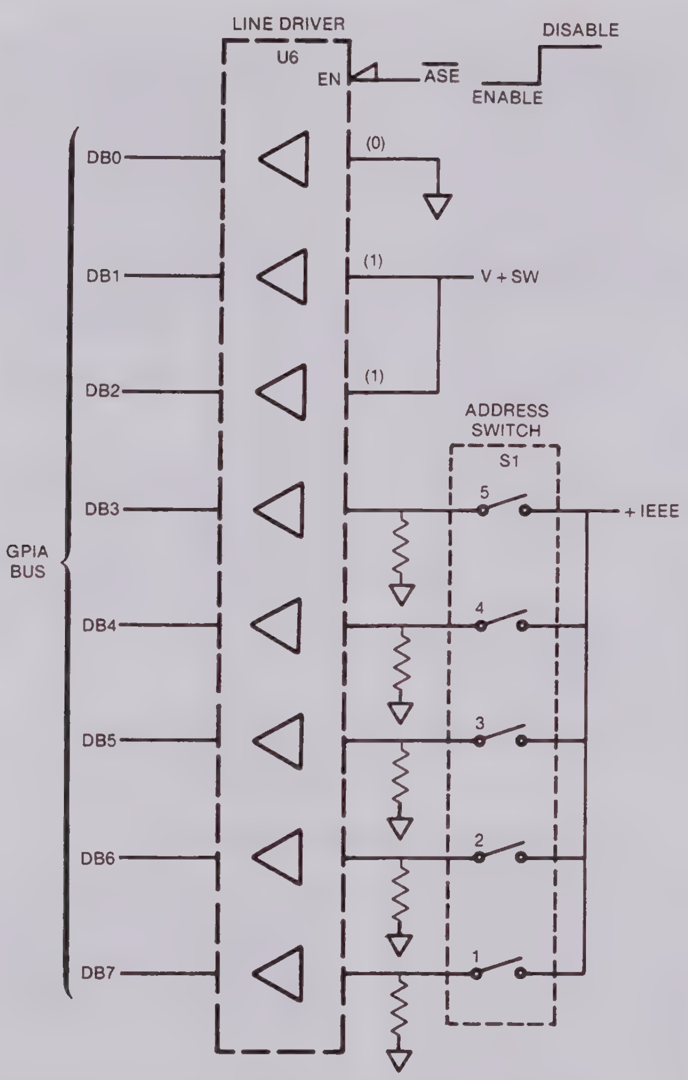


Figure 5-66. GPIB Address/Identification

cuit consists of the tristate bidirectional transceiver U5 and its control circuit U1D, U4B, U4C, and U4D.

The GPIA Transceiver (U5-19 EN) receives its enable command (RS488 — unlabled on the schematic) from the Power Initializer (see paragraph 5.9.2.6). The transceiver is normally enabled (low). Yet, the transceiver can be disabled (high) when the multimeter is powered from internal batteries or for a short time on an external source when the multimeter powers on or powers down. The direction of data flow through the GPIA Transceiver (U5-1 — EN) is selected by the transceiver's control circuit. When the direction line is low, data flows from the GPIA to the multimeter Address/Data bus (AD0 – AD7). When the direction line is high, the data flows from the multimeter Address/Data bus (AD0 – AD7) to the GPIA.

The control circuit U1D, U4B, U4C, and U4D controls the data flow direction through the transceiver. This circuit is a two input RS NOR flip flop. The Address Strobe (AS) line from the multimeter drives the reset (R) input to the flip flop. The flip flop's other input is derived from the Enable clock (E), Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$), and Board Enable ($\overline{\text{BD}_{(N)}}$) lines which originate from the multimeter. Data flows (direction line — low) from the GPIA bus

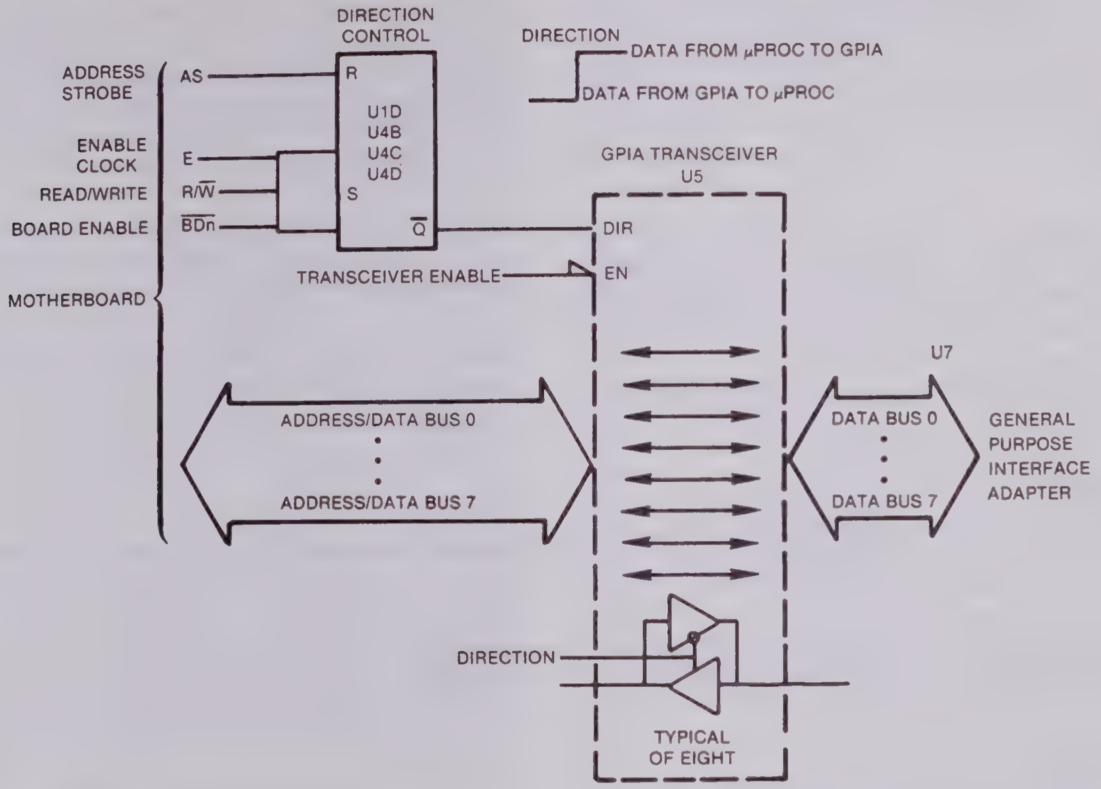

DIRECTION CONTROL
DIRECTION
DATA FROM μPROC TO GPIA
DATA FROM GPIA TO μPROC
ADDRESS STROBE
AS
R
U1D
U4B
U4C
U4D
ENABLE CLOCK
E
READ/WRITE
R/$\overline{W}$
S
BOARD ENABLE
$\overline{BDn}$
$\overline{Q}$
GPIA TRANSCEIVER
U5
DIR
TRANSCEIVER ENABLE
EN
MOTHERBOARD
U7
ADDRESS/DATA BUS 0
ADDRESS/DATA BUS 7
DATA BUS 0
DATA BUS 7
GENERAL PURPOSE INTERFACE ADAPTER
DIRECTION
TYPICAL OF EIGHT

Figure 5-67. GPIA Transceiver

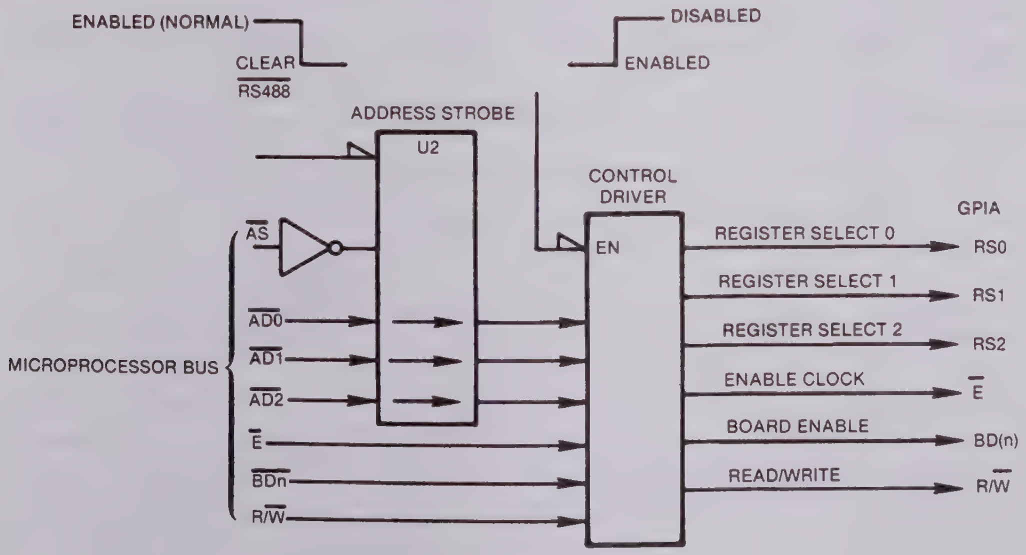

ENABLED (NORMAL)
CLEAR
$\overline{RS488}$
DISABLED
ENABLED
ADDRESS STROBE
U2
CONTROL DRIVER
EN
GPIA
$\overline{AS}$
$\overline{AD0}$
$\overline{AD1}$
$\overline{AD2}$
$\overline{E}$
$\overline{BDn}$
R/$\overline{W}$
MICROPROCESSOR BUS
REGISTER SELECT 0
RS0
REGISTER SELECT 1
RS1
REGISTER SELECT 2
RS2
ENABLE CLOCK
$\overline{E}$
BOARD ENABLE
BD(n)
READ/WRITE
R/$\overline{W}$

Figure 5-68. Buffer

multiplexer is set up for single ended input connections, the switch matrix enables a single column at a time.

When measuring thermocouples, the channel list must contain a cold junction measurement of a multiplexer channel; this measurement should the first entry in a channel list. The multimeter reads the cold-junction temperature once each scan of the channel list.

5.10.2.1 Multiplexer Switching

The Multiplexer switches do the actual routing for the multiplexer. The switches are made up of 20 Field Effect Transistor (FET) switches optically coupled to the Switch Matrix. This multiplexer has a maximum input level of 300 Vdc or peak ac between any two input terminals. In addition, the multiplexer inputs are protected from up to 6kV peak (<10μs duration) transients.

Figure 5-71 illustrates the switches. The switches in this illustration are shown as traditional switches, rather than as FET switches. The "input switches" U8, U9, U10, U11, U12, U13, U14, and U14 connect the input terminals to the "bank switches". For single ended inputs, each switch is closed as needed by the switch matrix; for example, switch U8B closes selecting the input for Channel 1, single ended. For differential inputs, pairs of switches are closed as needed; for example, U8B and U8D closes selecting the positive and negative inputs for Channel 1. The "bank switches" select which group of four input switches are connected to the output terminal. For single ended inputs, only one switch (U16B, U16D, U17B, or U17D) of the four switches is closed. For differential inputs, pairs of switches (U16B and D or U17B and D) are closed. The single ended/differential "switch" (J2) determines how the inputs "tie" to the output terminal. Figure 5-72 illustrates an example of a single ended switching which connects Channel 3's input terminals to the output terminals. Figure 5-73 illustrates an example of differential switching which connects the positive and negative input terminal of Channel 3 to the output terminals.

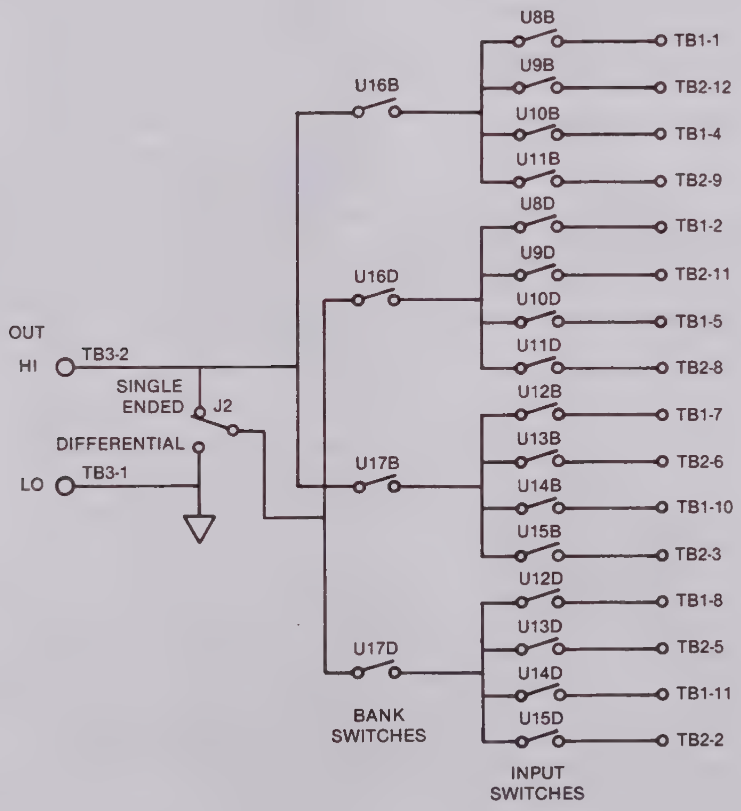

U8B
TB1-1
U9B
TB2-12
U16B
U10B
TB1-4
U11B
TB2-9
U8D
TB1-2
U9D
TB2-11
U16D
U10D
TB1-5
OUT
HI
TB3-2
U11D
TB2-8
SINGLE
ENDED
J2
U12B
TB1-7
DIFFERENTIAL
U13B
TB2-6
LO
TB3-1
U17B
U14B
TB1-10
U15B
TB2-3
U12D
TB1-8
U13D
TB2-5
U17D
U14D
TB1-11
BANK
SWITCHES
U15D
TB2-2
INPUT
SWITCHES

Figure 5-71. Multiplexer Switching

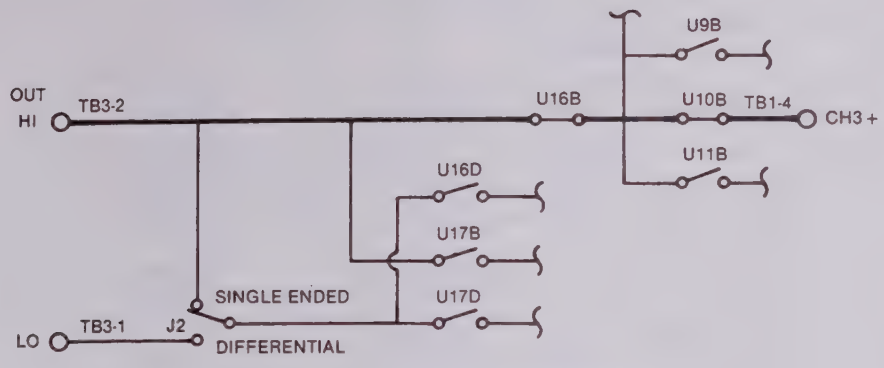

U9B
OUT
HI
TB3-2
U16B
U10B
TB1-4
CH3 +
U11B
U16D
U17B
SINGLE ENDED
U17D
LO
TB3-1
J2
DIFFERENTIAL

Figure 5-72. Single Ended Switching

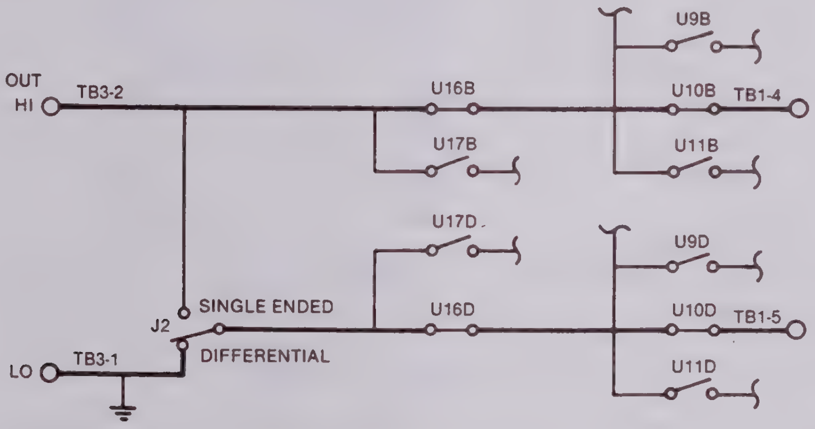

U9B
OUT
HI
TB3-2
U16B
U10B
TB1-4
U17B
U11B
U17D
U9D
SINGLE ENDED
J2
U16D
U10D
TB1-5
TB3-1
LO
DIFFERENTIAL
U11D

Figure 5-73. Differential Switching

Table 5-20 Switch lists the terminal strips, inputs switches, bank switches for each input channel input for both single ended and differential settings. The primary difference between single ended and differential input connections is the bank switching; single ended switching closes only one bank switch at a time, while differential switching closes two bank switches at a time.

5.10.2.2 Switch Matrix

The Switch Matrix "opens and closes" the multiplexer switches by turning off or on light emitting diodes which are optically coupled to the multiplexer's FET switches. The matrix consists of a 4 × 4 light emitting diode array, as shown in figure 5-74.

The four rows (Y1, Y2, Y3, Y4) control the cathodes of the matrix diodes. A low on any row enables a switch diode providing the anode is high. Regardless of the mode (single ended or differential) only one row will be active at a time.

The columns (X1, X2, X3, X4) control the anodes of the matrix diodes. A high on any of these rows enables a diode providing a diode's cathode is low. The column enabled depends on the mode. For single ended mode, a single column is enabled. For differential mode, pairs of columns are enabled (X1 and X3, or X2 and X4). Also, in series with each column is the "bank" diodes which enables the group of input switches to be routed to the multiplexer's output.

Table 5-21 lists the switches and their respective channels by row and column.

Table 5-20 Switch. Multiplexer Switching

Terminal Number	CH Number		Input Switch (Closed)	Bank Switch (Closed)
	Single Ended	Differential		
TB1-1	CH1 +	CH1 +	U8B	U16B
TB1-2	CH9 +	CH1 –	U8D	U16D
TB1-3	Ground			
TB2-12	CH2 +	CH2 +	U9B	U16B
TB2-11	CH10 +	CH2 –	U9D	U16D
TB2-10	Ground			
TB1-4	CH3 +	CH3 +	U10B	U16B
TB1-5	CH11 +	CH3 –	U10D	U16D
TB1-6	Ground			
TB2-9	CH4 +	CH4 +	U11B	U16B
TB2-8	CH12 +	CH4 –	U11D	U16D
TB2-7	Ground			
TB1-7	CH5 +	CH5 +	U12B	U17B
TB1-8	CH13 +	CH5 –	U12D	U17D
TB1-9	Ground			
TB2-6	CH6 +	CH6 +	U13B	U17B
TB2-5	CH14 +	CH6 –	U13D	U17D
TB2-4	Ground			
TB1-10	CH7 +	CH7 +	U14B	U17B
TB1-11	CH15 +	CH7 –	U14D	U17D
TB1-12	Ground			
TB2-3	CH8 +	CH8 +	U15B	U17B
TB2-2	CH16 +	CH8 –	U15D	U17D
TB2-1	Ground			

Table 5-21. Switch Matrix

	X1		X2		X3		X4	
	SE	Dif	SE	Dif	SE	Dif	SE	Dif
Y1	U8A Ch1	U8A Ch1	U12C Ch5	U12C Ch5	U8C Ch9	U8C Ch1 –	U12C Ch13	U12C Ch5 –
Y2	U9A Ch2	U9A Ch2	U13A Ch6	U13A Ch6	U9C Ch10	U9C Ch2 –	U13C Ch14	U13C Ch6 –
Y3	U10A Ch3	U10A Ch3	U14A Ch7	U14A Ch7	U10C Ch11	U10C Ch3 –	U14C Ch15	U14C U7 –
Y4	U11A Ch4	U11A Ch4	U15A Ch8	U15A Ch8	U11A Ch12	U11A Ch4 –	U15C Ch16	U15C Ch8 –

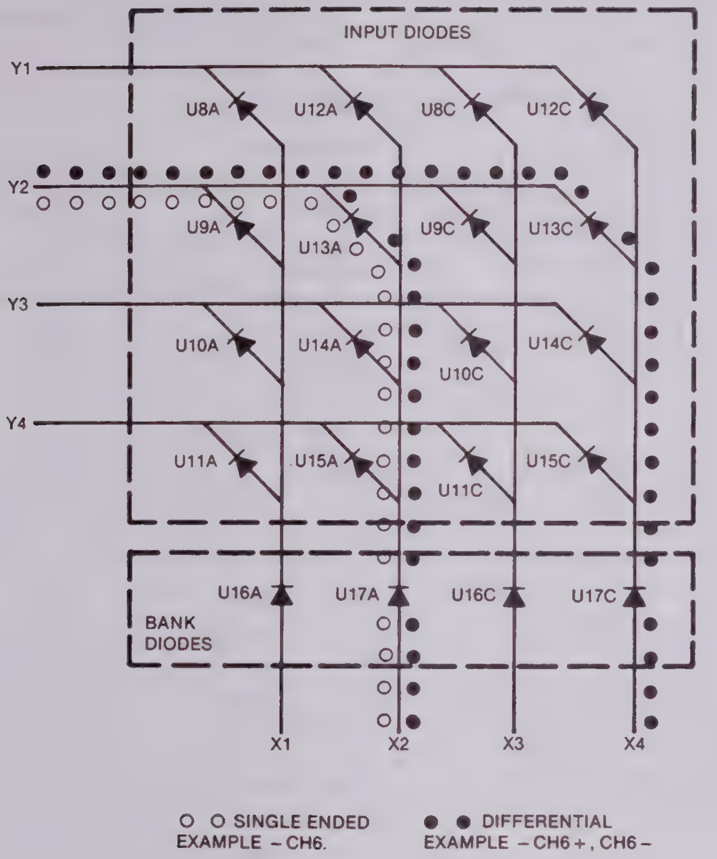

INPUT DIODES
Y1
Y2
Y3
Y4
U8A
U12A
U8C
U12C
U9A
U13A
U9C
U13C
U10A
U14A
U10C
U14C
U11A
U15A
U11C
U15C
U16A
U17A
U16C
U17C
BANK DIODES
X1
X2
X3
X4
○ ○ SINGLE ENDED
EXAMPLE – CH6.
● ● DIFFERENTIAL
EXAMPLE – CH6 +, CH6 –

Figure 5-74. Switch Matrix

5.10.2.3 Switch Control

Switch Control (see figure 5-75) receives a six-bit byte from the Measurement Module "Mux" control bus, decodes the byte, and switches the rows and columns of the Switch Matrix. The six-bits perform various functions which are illustrated as follows:

F E D C B A
[Channel Enable] [Row Select]
[Column Select]

The A and B lines select the row of the switch matrix, the C and D lines select the column of the Switch Matrix, and the lines D, E, and F select the multiplexer's channel number.

The Row Decoder U3B decodes the two lower order bits (A and B) from the "Mux" control bus. Table 5-22 illustrates the input versus output combinations of the Row Decoder.

Table 5-22. Row Decoder Logic

EN (G)	B	A	Output	Row
Low	Low	Low	Yo	$\overline{Y1}$
Low	Low	High	Y1	$\overline{Y2}$
Low	High	Low	Y2	$\overline{Y3}$
Low	High	High	Y3	$\overline{Y4}$
High	X	X	X	High All rows disabled

The decoder is enabled when the EN (G) line goes low. This line is controlled by Channel Enable and Cold Junction Temperature. To enable the decoder, the multimeter must be scanning a multiplexer channel number in the group setup by the Channel Enable switch S1.

Column Decoder U3A decodes the two middle bits (C and D) from the "Mux" control bus. Table 5-23 illustrates the input versus output combinations of the

Column Decoder. Column Decoder sets up the Switch Matrix for single ended for differential mode. The "switch" U6 routes both input and outputs to and from the Column Decoder U3A. Each output from the decoder is inverted by the hex inverters U4B, U4F, U4A, U4E.

Table 5-23. Column Decoder

Single Ended				Differential			
Input		Output	Column	Input		Output	Column
D	C	Y		Ground	C	Y	
Low	Low	$\overline{Y0}$	$\overline{X1}$	Ground	Low	$\overline{Y0}$	$\overline{X1}$ & $\overline{X3}$
Low	High	$\overline{Y1}$	$\overline{X2}$	Ground	High	$\overline{Y1}$	$\overline{X2}$ & $\overline{X4}$
High	Low	$\overline{Y2}$	$\overline{X3}$	Ground	—	—	— —
High	High	$\overline{Y3}$	$\overline{X4}$	Ground	—	—	— —

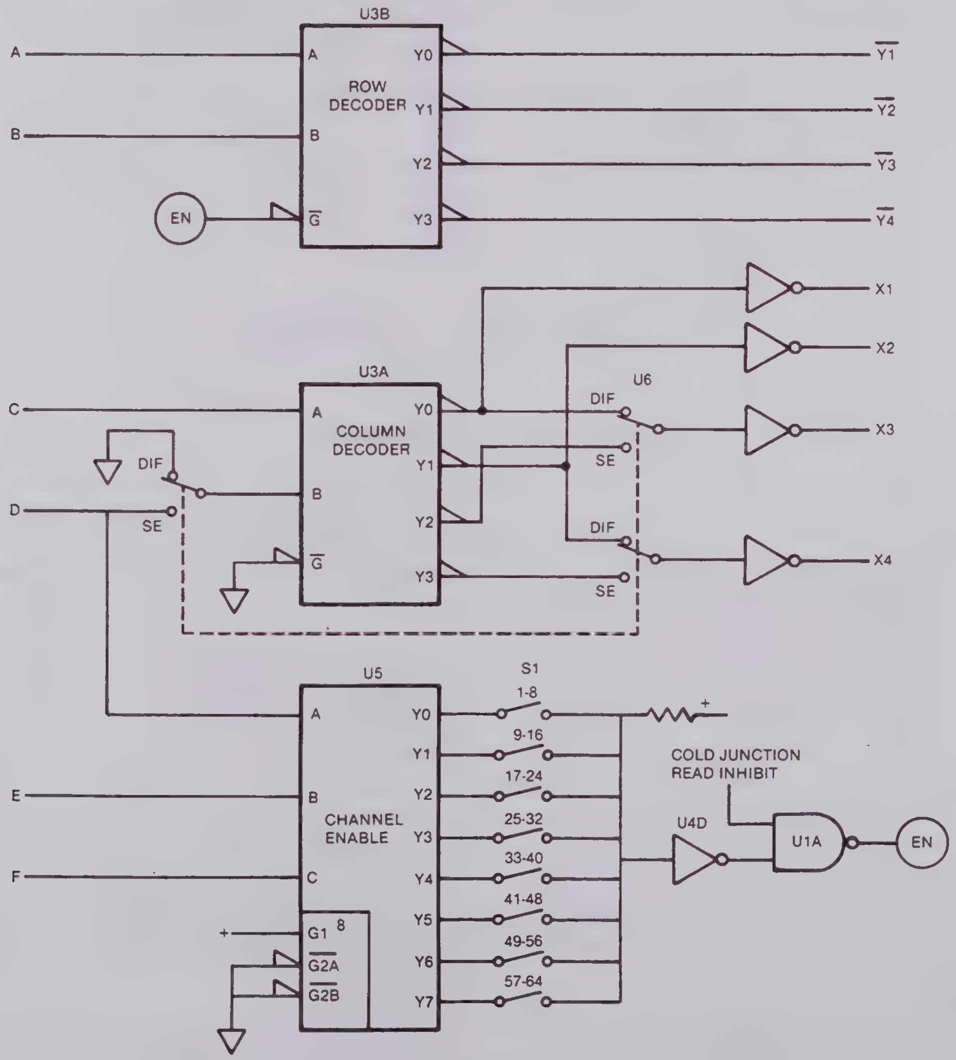

U3B
A
B
EN
A
ROW DECODER
B
$\overline{G}$
Y0
Y1
Y2
Y3
$\overline{Y1}$
$\overline{Y2}$
$\overline{Y3}$
$\overline{Y4}$
X1
X2
U3A
C
D
DIF
SE
A
COLUMN DECODER
B
$\overline{G}$
Y0
Y1
Y2
Y3
U6
DIF
SE
DIF
SE
X3
X4
U5
A
B
C
E
F
CHANNEL ENABLE
G1
8
$\overline{G2A}$
$\overline{G2B}$
+
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
S1
1-8
9-16
17-24
25-32
33-40
41-48
49-56
57-64
+
COLD JUNCTION READ INHIBIT
U4D
U1A
EN

Figure 5-75. Switch Control

Channel Enable activates the Row Decoder when the multimeter is addressing the selected multiplexer channel group. Channel Enable consists of the three to eight line decoder U5, the multiplexer channel group switch S1, and the gate logic U4D and U1A.

Table 5-24. Channel Enable

Input			Output	Multiplexer Channel Group
F	E	D		
Low	Low	Low	$\overline{Y0}$	1 through 8
Low	Low	High	$\overline{Y1}$	9 through 16
Low	High	Low	$\overline{Y2}$	17 through 24
Low	High	High	$\overline{Y3}$	25 through 32
High	Low	Low	$\overline{Y4}$	33 through 40
High	Low	High	$\overline{Y5}$	41 through 48
High	High	Low	$\overline{Y6}$	49 through 56
High	High	High	$\overline{Y7}$	57 through 64

The decoder U5 decodes the three higher order bits (D, E, F) (see table 5-24). Each output from the decoder connects to the channel group switch S1. To enable the multiplexer, at least one channel switch must be closed. For single-ended operation, two switches are usually closed, and for differential operation, only one switch is closed. When the decoder "finds" a closed switch, the $\overline{EN}$ line to the Row Decoder goes low providing the Cold Junction Read line is not inhibiting the $\overline{EN}$ line.

5.10.2.4 Cold Junction Temperature

The Cold-Junction Temperature circuit allows the multimeter to "read" the multiplexer's cold junction temperature by pulling the CJTEMP line high (once each scan of a channel list). The multimeter can only read the cold junction temperature if the CJ TEMP EN switch S1-1 on the multiplexer is closed and the multimeter calls a channel in the enabled switch group with the cold junction temperature function. Figure 5-76 provides a simplified diagram of the cold junction temperature.

The Multiplexer sends the cold-junction temperature when the output from U1B goes low which inhibits the Row Decoder U13B and forces the output from U1D high. With U1D high, the LED U18A conducts optically closing the FET U18B which routes the output from from the Centigrade Temperature Sensor U7 to the Multiplexer's output terminal. The sensor produces an output voltage (+10.0mV/°C) proportional to the temperature of the Multiplexer's isothermal block. All multiplexer switches are forced open while the multimeter reads the cold junction temperature. Table 5-25 gives the operating conditions for the Cold Junction circuit.

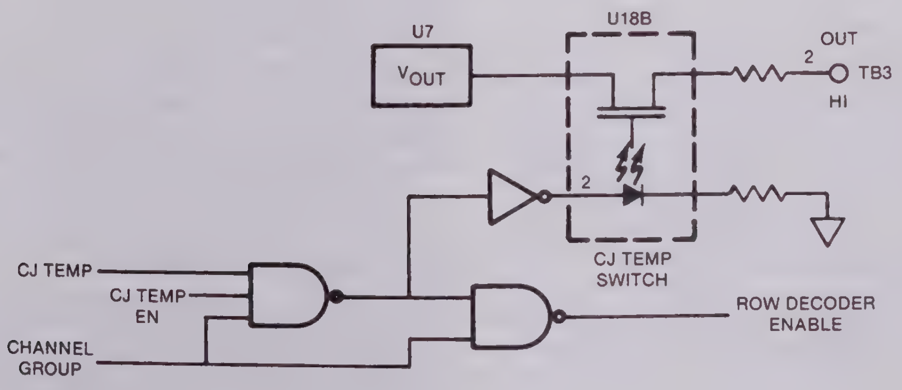


Figure 5-76. Cold Junction Temperature

Table 5-25. Cold Junction Temperature

U1C-9 CJ TEMP	U1C-10 CJTEMP EN	U1B-5 Channel Group	U18A-2 CJTEMP Switch	U3B-15 Row Decoder Enable
Low (0)	Open (0)	Low (0)	Off (0)	Disabled (1)
Low (0)	Open (0)	High (1)	Off (0)	Enabled (0)
Low (0)	Closed (1)	Low (0)	Off (0)	Disabled (0)
Low (0)	Closed (1)	High (1)	Off (0)	Enabled (1)
High (1)	Open (0)	Low (0)	Off (0)	Disabled (0)
High (1)	Open (0)	High (1)	Off (0)	Enabled (1)
High (1)	Closed (1)	Low (0)	Off (0)	Disabled (0)
High (1)	Closed (1)	High (1)	On (1)	Disabled (0)

5.10.3 Option 53-1 Multiplexer

The Option 53-1 multiplexer, which plugs into the Model 53 Expansion Chassis, routes up to 32 channels (differential), 64 channels (single ended), or 16 channels (four terminal) to Model 51 and 52 measurement module. The multiplexer also has built in temperature compensation which is needed when using thermocouples with the multiplexer. In addition, the multiplexer contains a 1mA current source and buffer for the output.

The Option 53-1 multiplexer functions much the same as the Option 50-20 multiplexer (paragraph 5.10.2) except for the following. Refer to schematic 0103-00-2877 located in the rear of this manual.

5.10.3.1 Multiplexer Switching

The multiplexer switching consists of eight, eight-channel analog multiplexers (U11, U13, U14, U15, U18, U19, U22, and U23). The outputs from theses multiplexers are routed through analog switches (U10A, U10BC, U10C, U17C, U17A, U17B, U21A, U21B) to switch S1, which selects the outputs (OUT 1-4) for the buffered output U1. Also, the outputs (OUT 1-4). The output can be taken directly from the terminal block or fed through the amplifier U1 for buffering.

This multiplexer has a limited input level of ±3.2 Vdc or ±4.8 Vpeak ac. In addition, the multiplexer inputs are protected from up to 6kV peak (<10μs duration) transients.

The analog multiplexers are controlled by the inverted A, B, and C (U6 A-F and U7 A-D) bits from the multiplexer control byte. Also, each analog multiplexer must be enabled ("G" goes low) by the bank control block.

5.10.3.2 Bank Control

Bank control selects which of the eight analog multiplexers are used to route the input signal to the measurement module. The bank control consists the bank selector U8A and its channel enable switches S2 1-4. It produces the bank select lines B1, B2, B3, B4. Furthermore, the bank select lines are decoded by demultiplexers U12 A-B and U20 A-B for each group of switch multiplexers.

5.10.3.3 Cold-Junction Temperature

The cold-junction temperature circuit allows the multimeter to "read" the multiplexer's cold junction temperature. This circuit is identical to the Option 50-20's circuit (paragraph 5.10.2.4) except the Option 53-1 uses analog switches U3A-B.

5.10.3.4 Current Source

The current source U2 provides 1mA of output current for use in resistance measurements and transducer excitation. Remember, when using this current source, the math channel or scaling must be used to calculate the resistance.

5.10.4 Option 53-2 Multiplexer

The Option 53-2 multiplexer, which plugs into the Model 53 Expansion Chassis, routes up to 16 channels (differential), 32 channels (single ended), or 8 channels (four terminal) to Model 51 and 52 measurement module. The multiplexer also has built in temperature compensation which is needed when using thermocouples with the multiplexer. In addition, the multiplexer supplies a 1mA current.

The Option 53-2 multiplexer functions the same as the Option 50-20 multiplexer (paragraph 5.10.2); refer to schematic 0103-00-2886 located in the rear of this manual. The only difference is the number of multiplexer channels.

5.10.4.1 Multiplexer Switching

The Multiplexer switches does the actual routing for the multiplexer. The switches are made up of 36 Field Effect Transistor FET switches optically coupled to the Switch Matrix. This multiplexer has a maximum input level of 300 Vdc or peak ac between any two input terminals. In addition, the multiplexer inputs are protected from up to 6kV peak (<10μs duration) transients.

The "input switches" U1 through U16 connect the input terminals to the "bank switches". For single ended inputs, each switch is closed as needed by the switch matrix; for example, switch U1B closes selecting the input for Channel 1, single ended. For differential inputs, pairs of switches are closed as needed; for example, U1B and U1D closes selecting the positive and negative inputs for Channel 1. The "bank switches" select which group of four input switches are connected to the output terminal. For single ended inputs, only one switch (U17B, U17D, U18B, or U18D) of the four switches is closed. For differential inputs, pairs of switches (U17B and D or U18B and D) are closed. The single ended/differential "switch" (S1-9) determines how the inputs "tie" to the output terminal.

The difference between single ended and differential input connects is the bank switching; single ended switching closes only one bank switch at a time, differential switching closes two bank switches at a time, and four terminal switching closes all four bank switches at once.

5.10.4.2 Switch Matrix

The Switch Matrix "opens and closes" the multiplexer switches by turning off or on light emitting diodes which are optically coupled to the multiplexer's FET switches. The matrix consists of a 8 × 4 light emitting diode array.

The eight rows (Y0 through Y7) control the cathodes of the matrix diodes. A low on any row enables a switch diode providing the anode is high. Regardless of the mode (single ended, differential, or four terminal) only one row will be active at a time.

The columns control the anodes of the matrix diodes. A high on any of these rows enables a diode providing a diode's cathode is low. The column enabled depends on the mode. For single ended mode, a single column is enabled. For differential mode, pairs of columns are enabled. For four terminal mode, all four columns are enabled at once. Also, in series with each column is the "bank" diodes which enables the group of input switches to be routed to the multiplexer's output.

5.10.4.3 Switch Control

Switch Control receives a six-bit byte from the Measurement Module "Mux" control bus, decodes the byte, and switches the rows and columns of the Switch Matrix. The A, B, and C lines select the row of the switch matrix, the C, D, and E lines select the column of the Switch Matrix, and the lines D, E, and F select the multiplexer's channel number.

The Row Decoder U23 decodes the three lower order bits ($\overline{A}$, $\overline{B}$, and $\overline{C}$) from the "Mux" control bus. The decoder is enabled when the G2A line goes low. This line is controlled by Channel Enable switching S1 and U22. To enable the decoder, the multimeter must be scanning a multiplexer channel number in the group setup by the Channel Enable switch S1.

Column Decoder U24, U25, and U26 decodes the three middle bits (D, E, and F) from the "Mux" control bus. Column Decoder sets up the Switch Matrix for single ended or differential mode.

The decoder U22 decodes the three higher order bits (D, E, F). Each output from the decoder connects to the channel group switch S1. To enable the multiplexer, at least one channel switch must be closed. When the decoder "finds" a closed switch, the G2A line to the Row Decoder goes low.

5.10.4.4 Cold Junction Temperature

The Cold-Junction Temperature circuit allows the multimeter to "read" the multiplexer's cold junction temperature by enabling CJTEMP FET U19D (once each scan of a channel list).

The Centigrade Temperature Sensor U27 produces an output voltage (+10.0mV/°C) proportional to the temperature of the Multiplexer's isothermal block. All multiplexer switches are forced open while the multimeter reads the cold junction temperature.

5.10.4.5 Current Source

The current source U2 provides 1mA of output current for use in resistance measurements and transducer excitation. Remember, when using this current source, a math channel or scaling must be used to calculate the resistance.

5.11 RECHARGEABLE BATTERY ASSEMBLY

The Rechargeable Battery Assembly, Option 50-11, provides a rechargeable battery and battery charging circuit. This assembly (1000-00-0467) consists of the 12V lead-acid battery, the Battery Charger, and the Power Detector; see figure 5-77.

The 12V battery allows the Model 51 and 52 (multimeter) to be used independent of external power sources. The GPIB board cannot be used while running on internal batteries. The Battery Charger recharges the battery whenever the multimeter is connected to an external source. The Power Detector monitors the external power and switches in the battery (no external power source) or out the battery (external power source).

5.11.1 Battery

The Battery, a 2.9 ampere-hour sealed lead-acid battery, can operate the multimeter up to 70 hours. The length of operation depends on the unit configuration. From a deep discharge, the battery can be recharged to a full charge in 12 hours. From a half discharge, the Battery can be recharged to a full charge in 4 hours.

5.11.2 Battery Charger

The Battery Charger (see figure 5-78), a single integrated circuit U1 configured as a dual-level float charger, monitors the battery condition and controls the battery charge and hold cycles. The integrated circuit varies the battery charging current by controlling the pass transistor Q1; typically the charging current can vary between 25 mA and 600 mA. The Battery Charger's input is the external power source.

The easiest way to understand the operation of the Battery Charger is through its charging cycle; see figure 5-79. Connecting the unit to an external power source begins the trickle charging of the battery (approximately 25 mA). When the battery reaches approximately 10V, the Battery Charger turns on the pass transistor Q1 and turns off the trickle bias (U1 pin 11). Now the Battery Charger begins recharging the battery at the maximum rate (approximately 600 mA) until the battery voltage reaches the transition voltage (approximately 14V). At the transition voltage, the Battery Charger changes to the over-charge state (approximately 15V) and the charging current begins to decrease. At approximately 60 mA, the current sense output (U1 pin 1) goes high forcing OCTERM high. This changes the Battery Charger to a float state that holds the battery voltage at approximately 14V over a 0 to 600 mA charging rate. Once the multimeter loads and begins to discharge the battery, the Battery Charger begins its recharge cycle when the battery voltage drops to approximately 12.6V.

Two additional portions of the Battery Charger prevent it from draining the battery when external power is disconnected. The diode CR1 in series with the pass transistor Q1 is reverse biased which effectively opens the path through the pass transistor Q1. Also, the bottom of the resistor string (R6) connects to the Battery Charger's power indicator line (U1-7) which will go high when the unit is running on internal batteries effectively opening the resistor string.

5.11.3 Power Detector

The Power Detector (see figure 5-80) serves three functions. First, it switches to the internal battery when there is no external power. Second, it tells the motherboard the unit is operating off internal or external power. Finally, it is used by the microprocessor in determining the type, if any of battery option installed.

The Power Detector consists of two comparators U2A and U2B. Each inverting input of the comparators U2 pins 2 and 6 are referenced to a +2.5V reference voltage originating from the zener diode VR1. The noninverting inputs of the comparators U2 pins 3 and 5 monitors through a 3:1 resistance divider R8 and R9 the external power input J1 pin 3. When external power exceeds +7.5V, the comparator output U2 pin 1 goes high turning off the field effect transistor (FET) Q2 which disconnects the battery from the multimeter. If the external voltage drops below 7.5V or no external voltage, the comparator output U2 pin 1 goes low turning on the FET Q2 which connects the battery to the unit.

At the same time the other comparator U2 pin 7 signals the motherboard the type of power source used. If there is an external source, this output U2 pin 7 $\overline{\text{INTPWR}}$ is high telling the microprocessor the unit is running off external power source. If no external power source is connected or the external source is less than +7.5V, the line $\overline{\text{INTPWR}}$ is low telling the microprocessor the unit is running off internal batteries.

Both possible power sources (external and battery) power the Power Detector. If powered by the external power source the voltage, this circuit receives its power via diode CR2; diode CR3 is reverse biased. If powered by the internal batteries, this circuit receives its power via diode CR3.

The microprocessor also uses the Power Detector's $\overline{\text{INTPWR}}$ line to identify the type of power source: refer to paragraphs 5.2.3.3 and 5.2.3.4.

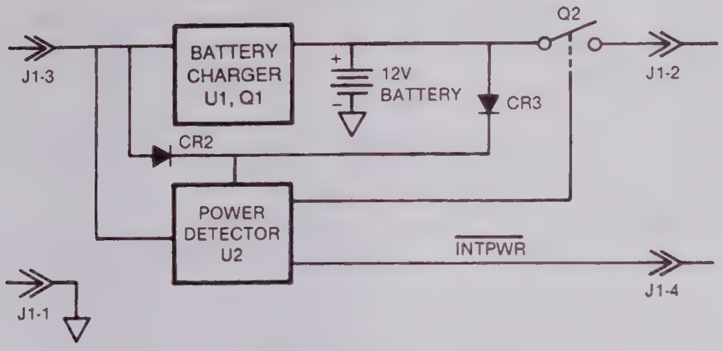

Q2
J1-3
BATTERY CHARGER U1, Q1
+
12V BATTERY
-
CR3
J1-2
CR2
POWER DETECTOR U2
INTPWR
J1-4
J1-1

Figure 5-77. Battery Charger

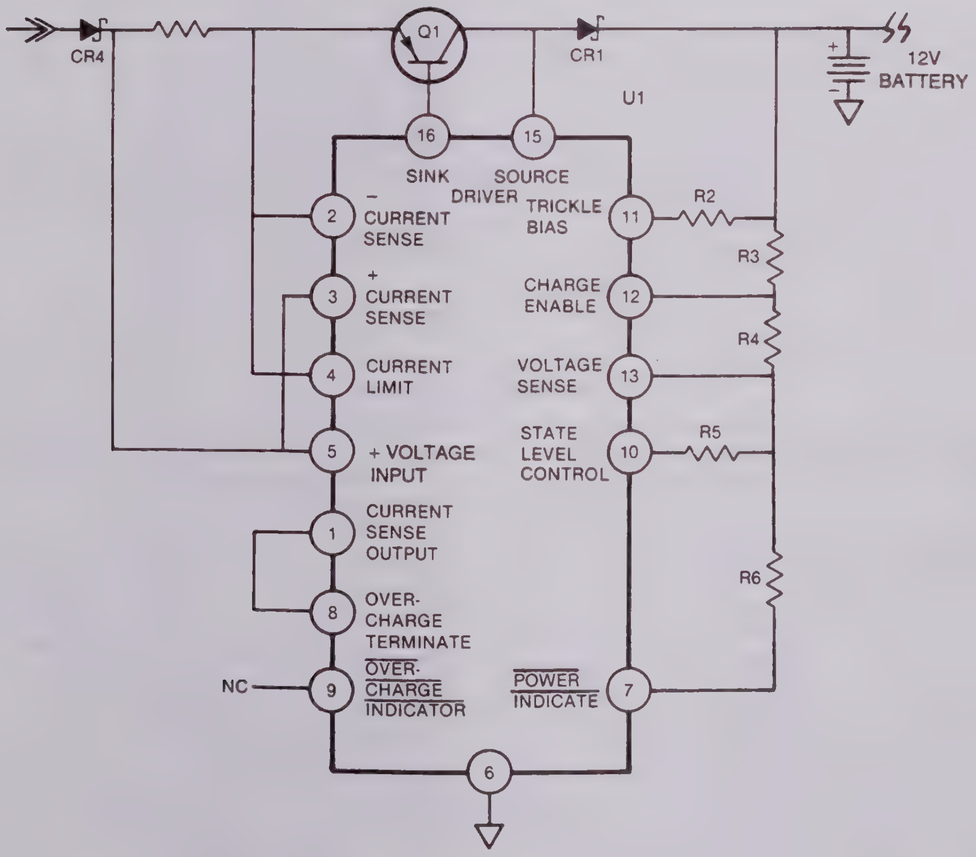

CR4
Q1
CR1
+
12V BATTERY
-
U1
16
15
SINK
SOURCE
DRIVER
2
−
CURRENT SENSE
TRICKLE BIAS
11
R2
R3
3
+
CURRENT SENSE
CHARGE ENABLE
12
R4
4
CURRENT LIMIT
VOLTAGE SENSE
13
5
+ VOLTAGE INPUT
STATE LEVEL CONTROL
10
R5
1
CURRENT SENSE OUTPUT
8
OVER-CHARGE TERMINATE
R6
NC
9
OVER-CHARGE INDICATOR
POWER INDICATE
7
6

Figure 5-78. Battery Charger

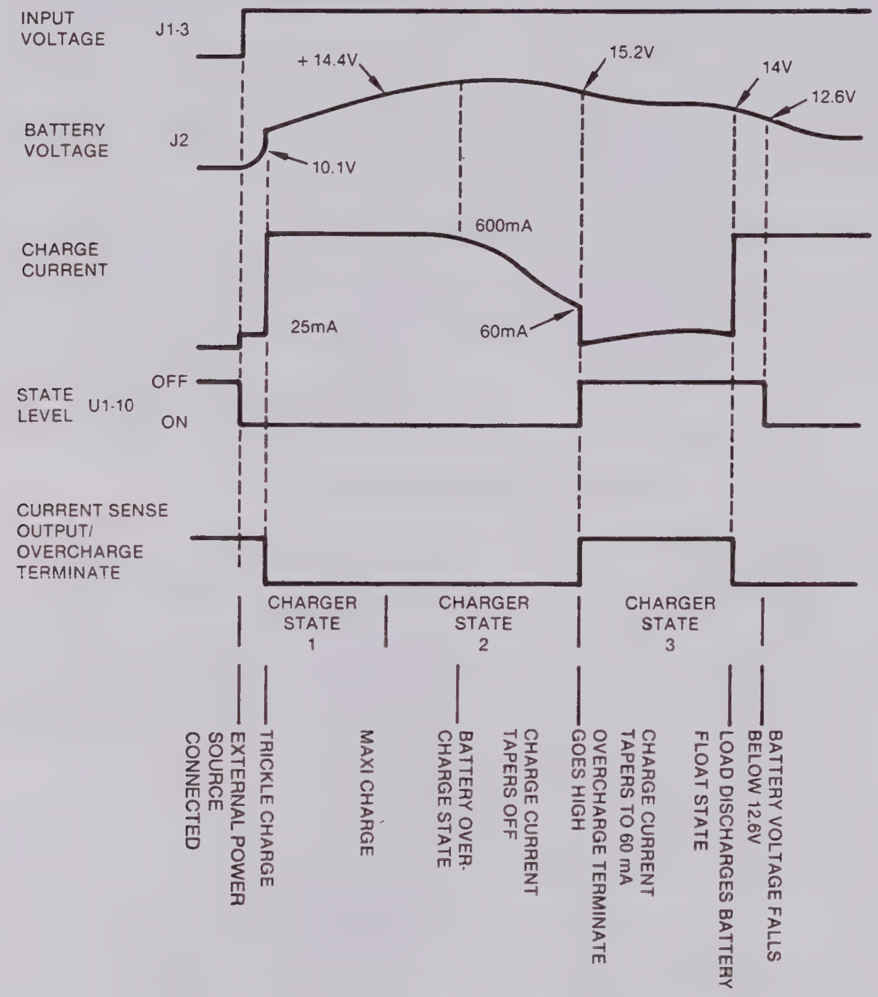

INPUT VOLTAGE
J1-3
BATTERY VOLTAGE
J2
+ 14.4V
15.2V
14V
12.6V
10.1V
CHARGE CURRENT
600mA
25mA
60mA
STATE LEVEL
U1-10
OFF
ON
CURRENT SENSE OUTPUT/ OVERCHARGE TERMINATE
CHARGER STATE 1
CHARGER STATE 2
CHARGER STATE 3
EXTERNAL POWER SOURCE CONNECTED
TRICKLE CHARGE
MAXI CHARGE
BATTERY OVER-CHARGE STATE
CHARGE CURRENT TAPERS OFF
OVERCHARGE TERMINATE GOES HIGH
CHARGE CURRENT TAPERS TO 60 mA
LOAD DISCHARGES BATTERY FLOAT STATE
BATTERY VOLTAGE FALLS BELOW 12.6V

Figure 5-79. Battery Charger Timing

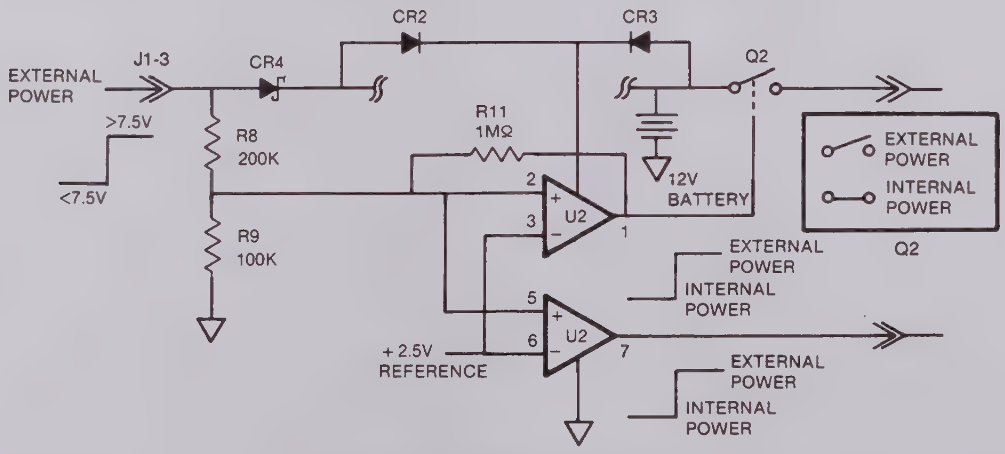

EXTERNAL POWER
J1-3
>7.5V
<7.5V
CR4
CR2
CR3
Q2
R8 200K
R9 100K
R11 1MΩ
2
3
U2
1
+
−
12V BATTERY
EXTERNAL POWER
INTERNAL POWER
Q2
EXTERNAL POWER
INTERNAL POWER
5
6
U2
7
+ 2.5V REFERENCE
EXTERNAL POWER
INTERNAL POWER

Figure 5-80. Power Detector

SECTION 6
TROUBLESHOOTING

6.1 INTRODUCTION

This section presents information which when used with the verification procedures (Section 3), circuit description (Section 5), calibration procedure (Section 4), and schematic and assembly drawings (Section 7) returns the Models 51 and 52 and their options to normal operation.

Table 6-1 lists test equipment that may be required for troubleshooting this instrument. Isolating some problems may require user competence with a signature analyzer or logic analyzer.

Appendix B contains a listing of recommended spare parts for users who want to troubleshoot their own units.

6.2 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the personnel or test equipment to troubleshoot the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the problem symptoms should be attached to minimize turnaround time.

Table 6-1. Suggested Test Equipment

Equipment Type	Suggested	Comments
triac or 0 to +15V, variable 2A power supply	LuTechnology 4206A or equivalent	Used for troubleshooting turn off or low battery point for battery operation
Calibrator	Datron 4700 or equivalent	For measurement module quantitative problems
Oscilloscope 2 channel, with delayed time base	Tektronix 2645 or equivalent	For general use
Or		
Storage Oscilloscope 2 channel, with delayed time base	Tektronix 7613 Vertical: 7A26 Horizontal: 7B53A	Extremely useful for verifying one-time digital signals
Sharp-tipped oscilloscope probe		For small outline devices
DVM	Wavetek 52 or equivalent	For general use
Counter	Wavetek 52 or equivalent	For general use
Signature Analyzer	Hewlett Packard 5004A or equivalent	For verifying signals between motherboard and measurement module
Logic Probe	Radio Shack 22-303 or equivalent	For measurement module—used in verifying the measurement control bits
Logic Analyzer	Arium ML4100	For isolating problems between motherboard and GPIB, Digital I/O, or RAM option board.
8, 14, and 40 pin IC test clips	Pomona Electronics or A P Products	For general use

Before returning the instrument, call Wavetek's Customer Service department and obtain a Return Authorization Number; this number is used to identify your instrument while it is in for repair.

The instrument should be packed according to paragraph 2.2, *Models 51 and 52 Operator's Manual*, and shipped to:

Customer Service
Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123

6.3 BEFORE YOU START TROUBLESHOOTING

Before beginning the troubleshooting process, verify that the instrument setup is correct. Instrument operation is covered by sections 3, 4, and 5, of the *Models 51 and 52 Operator's Manual.*

Also, visually inspect the instrument for physical damage and ensure the fuses are intact (paragraph 2.2). Finally, verify that the wall transformer, other external source, or internal batteries are good.

6.4 TROUBLESHOOTING THE MODELS 51 AND 52

6.4.1 Troubleshooting Overview

Section 6 troubleshooting material is organized into four "bridges" that are crossed in sequence:

- Accurately identify the symptom or problem (paragraph 6.4.2).
- Locate the problem board (paragraph 6.4.3).
- Isolate the problem on a board to a functional block or circuit stage (paragraph 6.4.4).
- Locate and replace the defective component.

Section 6 does not always give explicit troubleshooting techniques for isolating a problem all of the way to the bad component. However, in almost all cases, a careful reading of the Circuit Description for the bad circuit will allow you to deduce how troubleshooting to the bad part should proceed.

6.4.2 Narrowing Down The Fault Possibilities

Regardless of when a fault is suspected, whether during the instrument's routine operation, Performance Verification (Section 3), or Calibration Procedure (Section 4), always check for related symptoms before plunging into troubleshooting. For example, if one measurement module function is bad, check to see if the same function on other measurement modules is also bad. It is undesirable to waste time troubleshooting a measurement module when the problem is really the software for that function on the motherboard. So, the first step in isolating the problem to a board is to use the front panel controls exhaustively.

6.4.3 Isolating A Problem To A Board

6.4.3.1 Overview

The motherboard is also implicated on any problem that may at first appear to be certainly only a plug-in board or module. Not only is there some motherboard circuitry that interfaces uniquely to the suspect plug-in board, but the software for the plug-in board's functions resides on the motherboard (in ROM and RAM). Swap one of the suspect boards with a similar board, if available, and see if the problem goes with the board.

Paragraphs 6.4.3.2 through 6.4.3.9 are organized by pairs of suspect boards, and describe methods for isolating the problem to the board level.

Table 6-2. Circuit Board Supporting Paragraphs

Board	Performance Verification	Circuit Description	Troubleshooting	Drawing or Schematic
Motherboard	—	5.2	6.4.4.2	0103-00-1808
Measurement Module	3.5.1– 3.5.13	5.3.5.4	6.4.4.3	0103-00-1811
Keypad		5.5	6.4.4.4	0103-00-2414
Display		5.6	6.4.4.5	1206-00-2619
Digital I/O	3.8	5.7	6.4.4.6	0103-00-1814
Expansion RAM Board				
-12	3.9	5.8	6.4.4.7	0103-00-1817
-12A	3.9	5.8	6.4.4.7	0103-00-2947
GPIB Board	3.7	5.9	6.4.4.8	0103-00-2451
Multiplexer	3.11	5.10	6.4.4.9	0103-00-2656 0103-00-2886 0103-00-2877
Primary Battery	3.10	5.2.3.3	2.3.1	1000-00-0466
Rechargeable Battery	3.10	5.2.3.3 5.11	6.4.4.10	0103-00-2724

Table 6-2 references verification procedures which may be used to verify most functions on the boards, circuit descriptions of the boards, troubleshooting sections for isolating problems within boards, and drawings relating to each board.

6.4.3.2 Motherboard Vs. Measurement Module

6.4.3.2.1 Operating Vs. Board Swapping

Paragraph 6.4.3.2 covers only how to isolate the problem to which board. This will be sufficient for those wishing to return any bad measurement module to the factory for repair, while keeping the rest of the system. Paragraph 6.4.4.2 covers troubleshooting a problem on the motherboard. Paragraph 6.4.4.3 covers troubleshooting a problem on the measurement module.

Operating for problem isolation. If a second measurement module is installed, trying to operate it (from the front panel) produces some evidence as to whether the motherboard is at fault or not. However, operation by itself does not isolate a problem conclusively to the motherboard or a measurement module. This is because not all of the circuitry for one channel's measurement function is located on a measurement module.

Module-swapping (covered under paragraph 6.4.3.2.3) is conclusive and easy: If the problem follows the module, the problem is on the module; if not, the motherboard is bad.

6.4.3.2.2 One-measurement-module Approaches

If only one measurement module is available, the troubleshooter is limited to three approaches for conclusively finding out which board (motherboard vs. measurement module) is causing a module to not be recognized. The first uses a storage scope to see if the serial setups from the motherboard are correct during the power up routine (reference paragraph 5.4.4). A regular oscilloscope will not work for this since the scope trace will occur only once each time the power up routine is run, and the CRT persistence is not enough for the eye to see well. The second approach uses a signature analyzer to verify the serial data (paragraph 6.4.3.2.4). The third approach is to capture the serial data with one channel of a logic analyzer.

If the serial setup data is OK, also check the return signal from the measurement module. Figure 6-1 shows the pinout of the measurement module ribbon connector on the motherboard (J12, J13, J14, or J15).

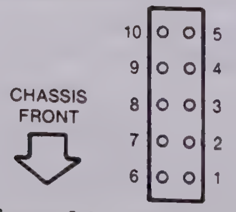


Figure 6-1. J12-J15 Pinout

Try connecting the module to another motherboard connector. This may isolate the problem as being in the motherboard circuitry just for the one channel. Remember to plug the LED (which substitutes for a measurement module optoisolator LED) into the alternate channel connector. (The channels are in pairs: J12 with J13, and J14 with J15). If the substitute-LED doesn't flash during the power up routine, the latch pulse loop is not being completed. In this case, ohm out the LED on each channel — the discrete LED, and the LED inside the measurement module optoisolator, U23 to find out which LED is at fault, or where the break is.

If the measurement module is working on some functions, this is strong evidence that the motherboard hardware and the measurement module measurement control hardware for that channel is working on all functions. The serial data for the bad measurement function(s) is *probably* good. In this case, you may choose to bypass verifying the serial data between the boards, and go right to examining parallel control bits on the measurement module (reference paragraph 5.4.5). If the parallel control bits on the suspect function are OK and the return signal is bad (paragraph 5.4.3), this is conclusive proof that the problem is on the measurement module. If the parallel bits are bad, obviously you don't know yet if the problem is on the motherboard, or in the measurement module digital (schematic sheet 2), without checking the serial data from the motherboard.

When using an oscilloscope to check for activity on the three line serial bus, also check that the $\overline{\text{PSEN}}$ line is low when the measurement module is used. Also check for a bad ribbon cable connection.

6.4.3.2.3 Two-module Approaches (Preferred)

Although the approaches of paragraph 6.4.3.2.2 may be used, having a second measurement module allows for the simple alternative of swapping measurement modules' connections at the motherboard connectors (J12, etc.). To swap boards, refer to paragraphs 2.4 and 2.6. When swapping boards, disconnect power before moving the board. Remember that it takes two measurement modules (channels 1 and 2, or, 3 and 4) to complete the path for the latch pulse on the motherboard. If the problem is on the suspect measurement module, the problem symptom will move with the measurement module, regardless of which motherboard connector (J12-J15) it is plugged into.

If neither of the two measurement modules is recognized, (check it on the CONFIGURATION menu, a main menu), assume the problem is on the motherboard, with the possible exception of the LATCH pulse current loop through the two measurement modules' U23 optoisolator LEDs.

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Expansion RAM Board				
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-12A	3.9	5.8	6.4.4.7	0103-00-2947
GPIB Board	3.7	5.9	6.4.4.8	0103-00-2451
Multiplexer	3.11	5.10	6.4.4.9	0103-00-2656 0103-00-2886 0103-00-2877
Primary Battery	3.10	5.2.3.3	2.3.1	1000-00-0466
Rechargeable Battery	3.10	5.2.3.3 5.11	6.4.4.10	0103-00-2724

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Module-swapping (covered under paragraph 6.4.3.2.3) is conclusive and easy: If the problem follows the module, the problem is on the module; if not, the motherboard is bad.

6.4.3.2.2 One-measurement-module Approaches

If only one measurement module is available, the troubleshooter is limited to three approaches for conclusively finding out which board (motherboard vs. measurement module) is causing a module to not be recognized. The first uses a storage scope to see if the serial setups from the motherboard are correct during the power up routine (reference paragraph 5.4.4). A regular oscilloscope will not work for this since the scope trace will occur only once each time the power up routine is run, and the CRT persistence is not enough for the eye to see well. The second approach uses a signature analyzer to verify the serial data (paragraph 6.4.3.2.4). The third approach is to capture the serial data with one channel of a logic analyzer.

If the serial setup data is OK, also check the return signal from the measurement module. Figure 6-1 shows the pinout of the measurement module ribbon connector on the motherboard (J12, J13, J14, or J15).

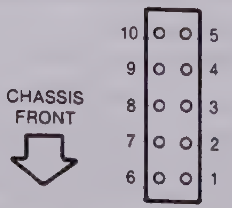

Figure 6-1. J12-J15 Pinout

Try connecting the module to another motherboard connector. This may isolate the problem as being in the motherboard circuitry just for the one channel. Remember to plug the LED (which substitutes for a measurement module optoisolator LED) into the alternate channel connector. (The channels are in pairs: J12 with J13, and J14 with J15). If the substitute-LED doesn't flash during the power up routine, the latch pulse loop is not being completed. In this case, ohm out the LED on each channel — the discrete LED, and the LED inside the measurement module optoisolator, U23 to find out which LED is at fault, or where the break is.

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When using an oscilloscope to check for activity on the three line serial bus, also check that the $\overline{\text{PSEN}}$ line is low when the measurement module is used. Also check for a bad ribbon cable connection.

6.4.3.2.3 Two-module Approaches (Preferred)

Although the approaches of paragraph 6.4.3.2.2 may be used, having a second measurement module allows for the simple alternative of swapping measurement modules' connections at the motherboard connectors (J12, etc.). To swap boards, refer to paragraphs 2.4 and 2.6. When swapping boards, disconnect power before moving the board. Remember that it takes two measurement modules (channels 1 and 2, or, 3 and 4) to complete the path for the latch pulse on the motherboard. If the problem is on the suspect measurement module, the problem symptom will move with the measurement module, regardless of which motherboard connector (J12-J15) it is plugged into.

If neither of the two measurement modules is recognized, (check it on the CONFIGURATION menu, a main menu), assume the problem is on the motherboard, with the possible exception of the LATCH pulse current loop through the two measurement modules' U23 optoisolator LEDs.

6.4.3.2.4 Signature Analysis Of Motherboard Signals

If only one measurement module is available, and it is not recognized, problem isolation requires that you look at the serial signals between the motherboard and the measurement module. You can look at the complex serial setup coming from the motherboard, visually, with an oscilloscope, and attempt to make a value judgement of the long data stream. Or, you can let a signature analyzer make the judgement as to the integrity of the serial data for you.

The power up routine is done when the MPU comes out of reset. For this test, the power is left on.

The following signature analysis setup verifies the DATA and CLOCK signals from the U27 gate array for each of the four measurement module channels, while type checking is occurring during the power up routine. If these signals are good, a scope should also be used to verify good logic levels at the measurement module ribbon cable connector(s).

Equipment required: HP 5004A Signature Analyzer, or equivalent. Momentary pushbutton switch (normally open). Two feet of small gage, insulated, stranded wire; soldering iron. (A jumper clip wire may be used instead of connecting the switch, but it is not recommended.)

Setup:

Analyzer	Signal Name	IC-pin#
START (↓)	$\overline{\mathrm{PSEN1}}$	U27-16
STOP (↑)	$\overline{\mathrm{PSEN4}}$	U27-19
CLOCK (↓)	E	U27-13
GND	VSS	U27-21

To force power-up routine runs with the power on: The pushbutton switch must be connected between V+ and the node at U13A-2 (schematic location 2C4). The end of one foot of wire is soldered to the cathode of CR20 (V+), the other end to the switch.

One end of the other foot of wire is soldered to the end of R66 which connects to C29. The other end is soldered to the pushbutton switch. Tape the switch so its terminals can't accidentally contact any circuitry.

Verify with an oscilloscope during the power up routine that TOUT is correct. TOUT should have one latch pulse after each DATA/CLOCK cluster, occurring just before the next cluster.

After moving the probe to each new location, press the pushbutton momentarily to put the unit into reset. When the unit comes out of reset, the power up routine generates a unique signature for that probe location. An incorrect signature indicates that the problem is on the motherboard.

Signal Name	Location	Signature
$\overline{\mathrm{PSENx}}$	U27-(16-19)	0000
DATA1	U27-29	6605
DATA2	U27-28	6U43
DATA3	U27-27	9P97
DATA4	U27-26	H8U9
CLK1	U27-25	2C16
CLK2	U27-24	046P
CLK3	U27-23	U77C
CLK4	U27-22	A4P7

6.4.3.3 Motherboard Vs. Keypad

The reference theory of operation paragraph is 5.5.

A logic analyzer may be used, but the majority of keypad related problems are either in the keypad assembly, or the connection to the motherboard.

Check J3, and the signals around U10B and U11.

See also paragraph 6.4.4.4.

6.4.3.4 Motherboard Vs. Display

If another display assembly is available, possibly in another unit, plug it into the suspect chassis using an extender cable.

A logic analyzer is appropriate for determining if the motherboard is sending correct data. The reference theory of operation paragraph is 5.6.

See also paragraph 6.4.4.5.

6.4.3.5 Motherboard Vs. Digital I/O Board

WARNING

Always disconnect external power and any internal battery pack (50-10 or 50-11), and wait one minute, before removing/replacing an option board.

If a logic analyzer is available, refer to appendix C.

If you have a mix of option boards (RAM, IEEE-488, Digital I/O), if one option board fails and the rest of the option boards work, generally the motherboard is good. (Hardware, not software, usually fails.)

If the Model 51 or 52 has only one Digital I/O board, install the board in another slot (paragraph 2.4) and check it out. If the Digital I/O board works in the new slot, the problem is with the motherboard. If it does not work, it is inconclusive where the problem is. See paragraphs 2.4 and 2.6.

If the problem is thought to be on the Digital I/O board, see paragraph 6.4.4.6 for troubleshooting.

If the problem is thougnt to be on the motherboard, see paragraph 6.4.4.2.

6.4.3.6 Motherboard Vs. RAM Board

WARNING

Always disconnect external power and any internal battery pack (50-10 or 50-11), and wait one minute, before removing/replacing an option board.

If a logic analyzer is available, refer to appendix C.

When a RAM expansion board seems bad, try operating any other RAM boards installed in the unit. If another RAM board works, this is an indication that the problem is likely on the suspect RAM board. To be sure, open the unit's cover and swap the two RAM boards (paragraph 2.4). If the problem is on the suspect board, the operating symptom will move with the option board.

Having a second RAM board is the best way of checking that the internal software which handles expansion RAM communications, and all required motherboard hardware is OK. Almost the only things on the motherboard, that are peculiar to the suspect RAM's former socket are the board enable signal, and some small space in motherboard RAM and ROM.

If the only other option board is a non-RAM board, try operating it anyway. This is a rough test of the motherboard IC and software which generates the socket enable signals — if both option boards seem bad, assume the problem is on the motherboard. If the second option board operates OK in its present position, open the unit's cover and swap it with the suspect RAM board. This will provide a conclusive test of the board enable signal and the socket signal buffering circuitry (on the motherboard), but not the bank switching line or software.

If you think the problem is on the expansion RAM board, see paragraph 6.4.4.7 for troubleshooting.

If you think the problem is on the motherboard, see paragraph 6.4.4.2 for troubleshooting.

6.4.3.7 Motherboard Vs. GPIB Board

WARNING

Always disconnect external power and any internal battery pack (50-10 or 50-11), and wait one minute, before removing/replacing an option board.

If a logic analyzer is available, refer to appendix C.

Verify the GPIB address is correct, the Model 51 or 52 is powered by an external source, and the rear panel IEEE On switch is on. See paragraph 2.3.9 and 2.3.5 of the *Models 51 and 52 Operator's Manual.*

If the unit does not respond to GPIB commands, try to set up the unit using the front panel controls. If the unit does not respond to either front panel and GPIB commands, you can assume the problem is on the motherboard (paragraph 6.4.4.2) or the keypad (paragraph 6.4.3.3). If the unit responds to front panel control and not GPIB commands, assume the problem is on the GPIB board.

When there is a mix of option boards (RAM, IEEE-488, Digital I/O), if the only one of one type of board fails and the rest of the option boards work in that slot, you can generally assume the option board has failed, and not the motherboard.

Table 6-3 identifies common GPIB problems and recommended solutions.

6.4.3.8 Measurement Module Vs. Multiplexer

First verify the multiplexer is set up correctly (paragraph 2.3.7 of the *Models 51 or 52 Operator's Manual*). If it is set up correctly, there are two ways to check it out. Plug the suspected multiplexer into another measurement module and check its operation. If the multiplexer works, assume the measurement module is bad and if the multiplexer does not work, assume the multiplexer is bad (paragraph 6.4.4.9). Also, another multiplexer can be connected to the measurement module and checked which confirms whether the problem is a multiplexer or measurement module problem.

6.4.3.9 Motherboard Vs. Batteries

When the Model 51 or 52 contains either Option 50-10 alkaline or Option 50-11 rechargeable batteries and the Model 52 does not power on, connect the unit to an external source and verify it works. If the Model 51 or 52 does power on, assume the batteries are bad. To replace the alkaline batteries, refer to paragraph 2.3.1. To repair the rechargeable battery assembly, refer to paragraph 6.4.4.10.

6.4.4. Isolating A Bad Circuit Within A Board

6.4.4.1 Overview

Each subparagraph of 6.4.4 contains a listing of the circuit description, calibration procedure, and drawing related to that specific board.

These subparagraphs list the pertinent schematics, assembly drawings, and circuit descriptions. In addition, the subparagraphs list a series of likely items to check to isolate problems on the board.

The circuit boards' subparagraph numbers are in the following order:

Motherboard
Measurement Module
Keypad Display
Digital I/O
RAM Board
GPIB Board Multiplexer
Rechargeable Battery Assembly

Before connecting test instruments, visually inspect the wiring and circuit boards for damage.

WARNING

> **With the covers removed and a high voltage applied at a measurement module input connector, dangerous voltage points may be exposed in the measurement module. Contact with any of these points may cause serious injury or death.**

NOTE

> *There are no high or dangerous voltages present in the Models 51 and 52, unless such a voltage is applied to the front or rear panel input connectors.*

A pin on an S.O.(Swiss—"small" outline) IC may sometimes need to be lifted in order to isolate that pin from the signal in the board for troubleshooting purposes. Use solderwick (a kind of braid) to wick the solder from the pin-to-pad bond. Nudge the pin at the pad slightly with a metal pick to free the pin from the pad. Then the IC pin can be lifted slightly.

Caution

> Bending IC leads too high increases the risk that they will break off.

6.4.4.2 Motherboard Troubleshooting

Schematic: 0103-00-1808
Assembly Drawing: 1100-00-1808
Circuit Description: Paragraph 5.2

Model 52 Power Supplies and On/Off Control

Before working on the power supplies, read "What can be taken off the MPU bus."

What Runs What.

This tells you where to look and what you can disconnect if a particular supply is loaded down. See also appendix G.

B+:	U16 (V+), U12 (V++), 50-11 battery recharger board. Also goes through Digital I/O boards to the rear panel.
V++:	V+++, U15, U14, U13, expansion RAM boards.
V+++:	U3, U4, U7, U10.
V+:	U1, U2, U5, U6 (via Q3), U9, U11, IEEE-488 board (via S1-8),U18, U19, U20, U25, U26, U27, U28, U29, U30, U31, Digital I/O board.
V+6, $\overline{\text{PSENx}}$:	Measurement modules. (PSEN is not a power line.)

Troubleshooting the Linear and Switching Regulators.

Their input is B+. It must be greater than 10.0 volts for V+ power to stay on. This number used to be +5, but some rechargeable batteries failed when allowed to discharge so low, so all newer units have a 4:1 R48/R49 ratio.

Linear Supply (V++)

See paragraphs 5.2.3.1 through 5.2.3.8.

Switching Supply (V+6, V+)

1. Check F1, on the motherboard/rear panel if no B+ (cathode of CR16).
2. Ohm output to ground with power off: Should be more than: 10Ω.
3. Connect TP2 high, and try to turn unit on.
4. While battery pack and external power are disconnected, unplug all plug-in boards. Unplug measurement modules at J11-J15. Try to power up.
5. While B+'s are disconnected, disconnect the display ribbon cable from the motherboard. Try to power up.
6. While B+'s are disconnected, replace display ribbon cable. Check Q2: jumper G to S, ohm S to D — should be greater than 20KΩ. Remove jumper. Check U16 open-collector output: pin 3 to pin 4 should be greater than 50 KΩ.
7. Unsolder CR20's cathode, raise from board. Jumper about a 100Ω resistor from CR20's cathode to ground. Reconnect the B+ source. Verify you have V++ to pin 14 of U15. Try to power up. It may be necessary to jumper TP2 to V++ to keep U15 in the set (V+ on) state. See if U16 is oscillating (signal at U16-3). If it is, and B+ is not getting applied to the coil input during the pulses, Q2 is bad.

What Can Be Taken Off The MPU Bus

If jumpering TP2 to +5 (cathode of CR20) keeps the unit on), a MPU bus crash is causing random $\overline{\text{PWROFFs}}$ (U24-7) to turn off the V+. See figure 5-1, and the motherboard schematic. The following IC's must be functional for the unit to complete the power up routine: U1, U2, U3, U5, U4, and U7. In the address decoder, U19F, U18A, U23, U19D, U18B, and U10A must also be working. Other components on the MPU bus that aren't used during the power up routine and whose failure can interfere with the power up routine may be manually inhibited, or removed. This is largely the bus troubleshooting approach which follows. Devices on the bus that may be removed without interferring with the power up routine are plug-in boards, IC's U25, U26, U27, U11, U24, and the display module. U10B (1B3) may not be physically removed (U10A is needed at 2B2). However, the A0, A1, and A2 pins can be lifted off the board.

Troubleshooting Guide

Problem	Step	Process	Comment
Model 51 or 52 does not power up.	1.	Try the other two methods of obtaining a turn on (paragraph 5.2.4).	
	2.	Tying TP2 high (see motherboard schematic, 2C5) bypasses the software turn-off control. If this keeps the unit on, the power supplies are OK.	
	3.	Check these supplies: B+: Greater than 10.0 volts V+++: BT1 positive lead measures +3V V++: U12-2 measures +5V V+: Cathode of CR20 measures +5.3V	
Model 51 or 52 does not complete power-up routine correctly (garbage on display).	1.	Remove external source and internal batteries. Unplug all plug-in boards (measurement modules may be left plugged in). Unplug U27. Connect external power, try a turn-on.	Following is a step by step sequence for replacing parts. If the unit turns on ok, troubleshoot option boards, or replace U27, if indicated.
	2.	Remove external power. Replace U1 CPU and U5 ROM. Connect external power, try a turn-on.	
	3.	Remove external power. Unplug the display at J4. Reconnect external power, try a turn-on.	
	4.	Scope the $\overline{\text{KEYBD}}$ signal at U10B (1B3) to verify correct completion of the turn-on sequence. $\overline{\text{KEYBD}}$ should be narrow, regular, low-active pulses, at every $8.\dot{3}$ milliseconds.	Replace display, if indicated.
	5.	Check U1 MPU Mode set combination (pins 8-12) during the reset period. Check bus overhead signals: E, AS, and R/$\overline{\text{W}}$. Also, check address latch U2 operation.	
	6.	Check that standard RAMs (U4 and U7), clock chip U3, and ROM U5 get appropriate decoder signals. Also, check U10A at 2B2.)	For decoders: A logic pulser can provide missing decoder signal inputs. Use logic probe with stretcher on decoder output.
	7.	Check CPU U1 bus lines for shorts or stuck bits. Shorts: Ohm between all data and address lines with the power off.	
	8.	Disconnect external power. Unsolder bus-ICs form the bus in groups of 8, physically lifting them from the board only slightly. After each group of 8, reconnect power, and scope the line(s) in question. Don't expect to obtain a good power up sequence. Reconnect any pins lfted on this step, before moving to next step.	

Troubleshooting Guide (Continued)

Problem	Step	Process	Comment
	9.	IC-isolation: Remove external power. U25 (3D7) may be good, but the DIR line may be bad (high). Since the program is not executing properly, there is no way to tell if the DIR flip-flop U22C-8 switching signals are correct. To keep U25 pointing away from the CPU bus, make sure U25 pin 1 is forced high (unsolder U25-1 from its pad, lift slightly, and pull to a logic high with a 10K resistor).	
	10.	Connect external power, try a turn-on. If this "fixes" things, the problem may be U25, or, something causing a bad address decoder DIR output. Once the power up routine is working the address decoder (if good) should not make DIR ever go low (U25 pointing in), since no plug-in boards were recognized during the power up routine.	
	11.	Keep U11 from driving the CPU bus. Remove external power. Temporarily remove CR22 (use solder wick); pull up to a logic high U11-19 and U11-1 with a 10k pull up resistor at the CR22-anode pad. This ensures that U11, good or bad, does not drive the CPU bus. Reconnect external power, try a turn-on.	
	12.	Check all address decoder outputs. Sync the scope on each output, one by one; while seeing if the address lines are the correct combination for that output. (Ignore lower-order address lines that don't affect the addressing within a block.) Start with U18A (2B8) and work to the right. If U18A, U23, or U10A never have any output, replace the IC.	Or, use a logic analyzer on the chip inputs and output.
	13.	Disconnect external power. Replace clock chip U3. Connect external power, try a turn-on.	
	14.	Disconnect external power. Replace RAMs U4 and U7 as a *pair*. Connect external power, try a turn-on.	
	15.	Disconnect external power. Remove U25 (3D8), U26 (3D7), U11 and U10 (1B3). Reconnect external power, try a turn-on.	
	16.	Disconnect external power. Address decoder: Replace U18, U23. Reconnect external power, try a turn-on.	
Model 51 or 52 completes power up but does not recognize option boards. (Leave measurement modules plugged in.)		U24, and signals to U25, U26. U18A-7.	

Troubleshooting Guide (Continued)

Problem	Step	Process	Comment
Model 51 or 52 completes power up but recognizes only certain option boards.		Swap option boards, if available, to isolate problem to motherboard or plug-in board. If on motherboard, check signals from U24, U25, U26. If problem is on plug-in board, see the appropriate trouble-shooting guide.	
After unit powers up, it goes off again.	1.	A Program may be running, and be in power-save monitor mode. Stop the Program (use the Menu key until getting "Stop Program?"; then select "OK").	
	2.	Assuming a Program is not running, check U24 pin 7. U15B-4 should not be receiving any pulses. Replace ROM, U5. Replace RAM U4, U7.	
Power Off does not work; but unit recognizes any option plug-in board.		Check U15A, B, U20A, U14C, U13A, U14A, and associated passive components. Check $\overline{\text{PWROFF}}$ line.	
Power key turns unit off, but a program in power down mode does not.		Recall that remainder of scan interval must be less than 10 seconds for the software to turn the unit off. Check also that MONITOR MODE menu is set to PWR DOWN.	
Alarm tone is nonexistent or frequencies are wrong.		Check component values connected to OSC1 and OSC2 pins of U3 clock chip.	

6.4.4.3 Measurement Module Troubleshooting

Schematic:	0103-00-1811
Assembly Drawing:	1100-00-1811 (Option 50-1) 1100-00-2615 (Option 50-2)

Circuit Description: Paragraphs 5.3, 5.4

Before searching for bad circuits in the measurement module, you may check out the function in table 6-3. This table lists each function along with reference material in this manual relative to the function. The function may only need calibration; use the referenced calibration steps. Also, the function can be further evaluated using the verification procedure which could reveal that the function might work on other ranges. If you want to learn more about how the circuits for a function work, read the referenced circuit description paragraphs.

If you are troubleshooting during a power up routine, use paragraphs 5.4.2 and 5.4.4 as references.

If at least one of the measurement modules is recognized, that motherboard connector position can be used for stimulating other measurement modules. In that case, you may bypass troubleshooting the bad module during the power up routine.

Set up the unit for a measurement function according to table 5-12, and check the control bits.

To isolate a problem on the measurement module:

1. Check the digital control bits. If the digital control bits are incorrect, troubleshoot the measurement module's digital circuits.
2. If the digital control bits are correct, check the analog section of the measurement module. Identify all functions that work and do not work. Use table

6-4 to identify the circuits associated with the working and nonworking functions. Compare the list of working function's circuits against the list of nonworking function's circuits. The working circuits common to both working and nonworking functions can be assumed to be working. Those circuits unique to the nonworking function can be assumed to be bad. For example, if the VAC function does not work, find a working function such as VDC and compare the common circuits and the different circuits listed for each. In this example, the problem is probably in the AC CONVERTER, the TRUE RMS CONVERTER, or the signal routing components.

Note

> *The motherboard will not stimulate a measurement module if it is not "recognized" during the power-on routine. To allow a nonworking measurement module to be stimulated by the motherboard, do the following: Unplug the ribbon cable connector of the bad measurement module from its socket on the motherboard. Plug the ribbon cable connector of a good measurement module into the connector position. Turn on the unit. That channel should now be recognized (check the CONFIGURATION menu). Without turning off the power, unplug the ribbon plug of the good measurement module from the motherboard, and plug in the ribbon plug of the bad measurement module. The bad module will now be stimulated by control signals when measurements are done.*

Table 6-3. Measurement Module Function References

Measurement Module	Performance Verification	Calibration Procedure Table 4-2 Steps	Circuit Description
DC Voltage	3.5.1	8 to 30	5.3 5.4.5.3
dBdc CJ Temp	3.5.2	31 to 34	5.4.5.5
Temp			5.4.5.6
Ohms, Continuity Diode Chk			5.4.5.7

Table 6-3. Measurement Module Function References (Continued)

Measurement Module	Performance Verification	Calibration Procedure Table 4-2 Steps	Circuit Description
0Ω	3.5.4		
>1KΩ	3.5.5		
≤100Ω	3.5.6		
MΩ		61 to 63	
AC Volts	3.5.3	36 to 43	5.4.5.8
AC+DC Volts			5.4.5.9
dB			5.4.5.10
DC (mA) Current	3.5.7	64 to 69	5.4.5.11
DC (A) Current	3.5.8	70 to 74	5.4.5.11
AC (mA) Current	3.5.9	75 to 76	5.4.5.12
AC (A) Current	3.5.10	77 to 80	5.4.5.12
AC+DC Current			5.4.5.13
DC Watts			5.4.5.14
AC V-A			5.4.5.15
AC+DC V-A			5.4.5.16
Events			5.4.5.17.2
Frequency	3.5.11	81	5.4.5.17.3
Input Sens.	3.5.12		
Period			5.4.5.17.4
Time Int			5.4.5.17.5
Time Int 1-Sht			5.4.5.17.6
Pulse Width			5.4.5.17.7
Pulse Width 1-Sht			5.4.5.17.8
Logic			5.4.5.18
Input Sens TTL	3.5.13		
Input Sens CMOS	3.5.14		

Table 6-4. Function Vs. Circuit Blocks Matrix

5.4 Paragraph		J1	J2	U1	J3	J4	J101	J201	CURRENT SOURCE	RN2 INPUT DIVIDER	U7B MUX	A/D GAIN	+12VSW	-12	U15D	U17B	U15A	U16	U6A Selector sw.	A/D CONVERTER	SCHMITT TRIGGER	PRESCALER	U31
5.4.5.3	Vdc	X	X				X	X		*	*	X							X	X			
5.4.5.4	dBdc	X	X				X	X		*	*	X							X	X			
5.4.5.5	CJTEMP			X							X	X							X	X			
5.4.5.6	TEMP	X	X	X			X	X				X							X	X			
5.4.5.7	OHMS, CONT, —▶|—CHK	X	X						X	*		X							X	X			
5.4.5.8	Vac	X	X				X	X		*			X	X	*		X	X	X	X			
5.4.5.9	Vac+dc	X	X				X	X		*			X	X	*		X	X	X	X			
5.4.5.10	dB	X	X				X	X		*			X	X	*		X	X	X	X			
5.4.5.11	Adc		*		X	*					X	X							X	X			
5.4.5.12	Aac		*		X	*					X		X	X		X	X	X	X	X			
5.4.5.13	Aac+dc		*		X	*					X		X	X		X	X	X	X	X			
5.4.5.14	Wdc		See Vdc and Adc.																				
5.4.5.15	VAac		See Vac and Aac.																				
5.4.5.16	VAac+dc		See Vac and Aac.																				
5.4.5.17.2	EVENTS	X	X				X	X					X	X	*		X				X		X
5.4.5.17.3	FREQ	X	X				X	X					X	X	*		X				X	*	X
5.4.5.17.4	PERIOD	X	X				X	X					X	X	*		X				X	*	X
5.4.5.17.5	T-INT, T-INT..1 SHOT	X	X				X	X					X	X	*		X				X		X
5.4.5.17.6	P-WTH, P-WTH..1SHOT	X	X				X	X					X	X	*		X				X		X
5.4.5.18	LOGIC	X	X				X	X					X	X	*		X				X		X

*Circuit is used only on some ranges (for example, High MΩ).

Troubleshooting Guide

Problem	Step	Process	Comment
Model 51 or 52 completes power up routine, but does not recognize any measurement modules.		On motherboard, check the $\overline{\text{A/D}}$ decoded output line at U27-20. Check U27, U30, U31, U28, U29. If an odd number of measurement modules is installed, check that the TIL-220 channel card substitute LED is installed. See paragraph 2.6.	
Model 51 or 52 completes power up routine, but does not recognize *one* measurement module (according to CONFIGURATION menu).	1.	Swap measurement module (ribbon cable connector on motherboard) with another recognized module to see if problem is on motherboard, or on measurement module. U27, PSEN line. Check optoisolators on measurement module (paragraph 5.3).	
	2.	Listen for a relay click when turning on the Model 51 or 52. Also, in DMM mode, Vdc, there should be a relay click when changing between the 3V and 30V ranges. If not, then either the digital section on the measurement module (schematic sheet 2), or power on the measurement module (schematic sheet 5) is at fault.	
Measurement module fails some measurement functions, but not others.		Compare the measurement module block diagram, figure 5.11, to which measurement functions do work. See table 6-4, the matrix. Determine whether AC vs DC functions work. If the AC section is bad, test the module by making an AC Voltage measurement and frequency measurement to further divide the circuitry. Then isolate to which ranges work. Check the control line states from the shift register outputs.	
No DC (volts, amperes, ohms) functions work.		Start by checking A/D CONVERTER. Check A/D-A and A/D-B lines. Sync the scope on the rising edge on A/D-A. See control lines sections, paragraphs 5.3.1.2 and 5.3.2.2	
Measurement module makes FREQ measurements until the input is disconnected; the display shows NOTRIG... then when the signal source is reconnected to the unit, there is no reading.		Replace U22 optoisolator on measurement module.	

Troubleshooting Guide (Continued)

Problem	Step	Process	Comment
Model 51 or 52 recognizes non-existent measurement modules.	1.	Check signals to and from U27 gate array on motherboard.	Change U27.
	2.	Pull up the input to the gate array input board 74HC14 by installing a pull up resistor: put a mating connector on the phantom channel's ribbon cable connector on the motherboard. Then solder a 10K pullup resistor from pin 8 (INXA) to pin 1, V+.	
When measuring Vac, with auto-range, if input voltage is close to 3.0 volts, the measurement module switches back and forth continuously between ranges (3V and 30V). May be helped by using a 0.1 second measurement delay in the DMM or channel list setup.	1.	Check U15D and U15C outputs for excessive noise or dc offset. DC offset RTO should be less than about 20mV.	
	2.	Remove and measure C39 and C37 near U16 (RMS converter). Both should be 1uF, +2% to −10%.	
Measurement module fails high-MOhms cal or performance test.		Clean the ohms and input sections of board with alcohol. Use rubber glove when handling board. *Note* *Freon-based cleaners may leave too much residue for this application.*	
Measurement module temperature function is bad.		Remove the thermocouple, and any multiplexers from the input of the measurement module. Short the input of the measurement module. If the correct ambient temperature is displayed, the problem is the thermocouple or multiplexer.	
	1.	See if VDC works (30mV and 300 mV ranges).	
	2.	See if CJTEMP function works.	
	3.	If both work, the problem is in software (ROM or RAM).	

Troubleshooting Guide (Continued)

Problem	Step	Process	Comment
Measurement module has high noise level on AC measurements.	1.	Put 10 uF tantalum (not aluminum) capacitors from the power pins of the affected OP AMP to ground, close to the OP AMP.	No margin between feedback loop division ratios, and the OP AMP specification of a minimum of two.
	2.	Reduce R24 slightly.	
	3.	Reduce R30 slightly.	
Measurement module has poor high frequency response.	1.	Adjust R25, C29 (near U15B).	
	2.	Replace U15.	Change U15.
Measurement module has poor common mode rejection.		Verify that the center shield is a cut-away version.	

6.4.4.4 Keypad Troubleshooting

Schematic: 0103-00-2414.
Assembly Drawing: 1100-00-2414.
Circuit Description: Paragraph 5.5.

Troubleshooting Guide

Problem	Step	Process	Comment
Unit beeps once at turn on, display works, keypad is inoperative.	1.	Check U10B.	Change U10B, R41-47.
	2.	Check one of the R40-47 resistors.	
One key on keypad doesn't work, or responds erratically.		Probably a dirty or oxidized metallic pad under the button. Remove keypad assembly, and clean the keypad using an ordinary clean pencil eraser.	
No response from keypad, no beep at turn on.		Check U10B-1 for keyboard enable.	Change U10B, CR22, U11.
More than one key on keypad not working—other keys working.		Check CR6, CR9, or CR10.	Change CR6, CR9, CR10.
One row or column on keypad doesn't work.		Check the appropriate pin/jack connection on J3.	

6.4.4.5 Display Troubleshooting Guide

Assembly Drawing: 1100-00-2619.
Circuit Description: Paragraph 5.6.

Troubleshooting Guide

Problem	Step	Process	Comment
If display is unplugged (ribbon connector at J4), the Model 51 or 52 powers up OK.		Replace display module.	
Display looks bad, Model 51 or 52 responds to keypad presses with one beep for each press.	1.	Unplug J4 display connector on motherboard with the power on.	"Relics" may show on the screen after the clock chip, U3, or one of the motherboard RAM chips, U4 or U7, is replaced.
	2.	Replug the display connector. Do a power on clear. Press the Menu key.	
At least ¼ of local display works.		Check Disp line(s) for the quarter(s) of the display in question.	
Display works, Viewing Angle does not.	1.	Unplug P4 (display connector), and while cycling through viewing angles using the 5LCD key, measure resistances from pin 12B to 12A on motherboard. If the problem is on the motherboard, turn off the power and measure resistances across R32 - R38.	
	2.	Check that U9 is getting 8 binary patterns on its S0-S2 inputs.	

6.4.4.6 Digital I/O Board Troubleshooting

To troubleshoot the digital I/O board,

1. Check the digital control lines to the digital I/O board. Verify the overhead signals work correctly (E Clock, Read/Write, Address Strobe, and Board Enable)
2. Check the individual functional blocks:
   Digital output problems paragraph 5.7.3
   Analog output problems paragraph 5.7.4
   Digital input problems paragraph 5.7.5

The following list identifies some common digital I/O board problems and suggested solutions.

Schematic: 0103-00-2856.
Assembly Drawing: 1100-00-2856.
Circuit Description: Paragraph 5.7.
Verification Procedure: Paragraph 3.8

Troubleshooting Guide

Problem	Step	Process	Comment
No or incorrect digital output.		Compare address/data bus lines, data latch outputs, and output FETs. Sync off rising edge of clock U3-11.	Change U3, Q1, Q2, Q3, Q4, Q5, Q6, Q7, or Q8.
No or incorrect digital input.		Compare input line and address/data bus line. Sync off the enable line U4-15 and U5-15 (active low). Verify A*/B U4-1 and U5-1 is low.	Change U4, U5, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R18, R19, R20, R21, R22, R23, or R24.

Troubleshooting Guide (Continued)

Problem	Step	Process	Comment
No or incorrect analog output.		Compare analog output and address/data bus lines (table 5-18). Sync off the chip select line (active low) U6-10.	Change U6.
Model 51 or 52 does not recognize Digital I/O board.	1. 2.	See paragraphs 5.7.2, 5.7.6. Check the address/data bus lines for 0000 0001. Sync off the enable line (active low) U4-15 and U5-15.	U4, U5.

6.4.4.7 Expansion RAM Board Troubleshooting

Schematic: 0103-00-2451.
Assembly Drawing: 1100-00-2451.
Circuit Description: Paragraph 5.9
Verification Procedure: Paragraph 3.7

Schematic: 0103-00-1817.
Assembly Drawing: 1100-00-1817.
Circuit Description: Paragraph 5.8
Verification Procedure: Paragraph 3.8

To troubleshoot the RAM boards,

1. Check the digital controls lines to the digital I/O board. Verify the overhead signals work correctly (E Clock, Read/Write, Address Strobe, and Board Enable).
2. Check the digital lines on the RAM board; refer to paragraph 5.8.

6.4.4.8 GPIB Board Troubleshooting

To troubleshoot the GPIB board,

1. Check the digital controls lines to the GPIB board. Verify the overhead signals work correctly (E Clock, Read/Write, Address Strobe, and Board Enable). Check that Q1 is turning on.
2. Check the digital lines between the digital control lines and the GPIA:
    GPIA, paragraph 5.9.2.1
    GPIA transceiver, paragraph 5.9.2.4
    the buffer, paragraph 5.9.2.5
3. Check the digital lines between the GPIA and GPIB controller:
    GPIA, paragraph 5.9.2.1
    GPIB transceivers,5.9.2.2

The following list identifies some common GPIB board problems and recommmended solutions.

Troubleshooting Guide

Problem	Step	Process	Comment
GPIB board is not recognized.	1.	Review paragraph 5.9.2.6.	
	2.	Check the rear panel DIP switch IEEE On; see paragraph 3.4 item 6 of the *Models 51 and 52 Operator's Manual.*	The GPIB board only operates from external power.
	3.	Check V+SW (+5V), INTPWR* (High), and IEEEV+ (+5V).	Change U5, Q1.
	4.	Compare address/data lines on both sides of buffers U2 and U5; sync off address strobe (AS).	Change U2, U5.
	5.	Review paragraphs 5.9.2.3 and 5.9.2.4.	
	6.	At power up check the board ID code (paragraph 5.9.2.3) when enabled (active low) U6-1&9.	Change U6.
	7.	At power up the bus transceiver is enable (active low) U5-19 and direction control U5-1 set (low).	Change U5.

Troubleshooting Guide (Continued)

Problem	Step	Process	Comment
Model 51 or 52 does not handshake with the GPIB controller.		Review paragraphs 5.9.2.1 and 5.9.2.2.	Change U7, U8, U9.
Model 51 or 52 handshakes with controller but does not respond to commands.	1.	Review paragraph 5.9.2.1.	
	2.	Verify U3-1 and 15 enabled (active low).	Change U3.
	3.	Check data flow through buffer U3.	Change U3.
	4.	Verify data strobed into U2 on rising edge of clock U2-9.	Change U2.
	5.	Verify data flow through GPIA transceiver U5. The DIR line U5-1 controls the direction.	Change U5.

6.4.4.9 Multiplexer Troubleshooting

Schematic: 0103-00-2856, 0103-00-2886, and 0103-00-2877.
Assembly Drawing: 1100-00-2856, 1100-00-2886, and 1100-00-2877.
Circuit Description: 5.10.
Verification Procedure: Paragraph 3.11

To troubleshoot a multiplexer,

1. Make sure the correct input terminals are used; refer to paragraph 2.3.7 of the *Models 51 and 52 Operator's Manual.*
2. Check the multiplexer to Model 51 or 52 interconnections; refer to paragraph 2.3.7 of the *Models 51 and 52 Operator's Manual.*
3. Verify the multiplexer's switches are set correctly; refer to paragraph 2.3.7 of the *Models 51 and 52 Operator's Manual.*
4. Check multiplexer's control input; refer to paragraph 5.10.2.3.
5. Check the multiplexer's matrix switch logic levels. If the correct switch diode is not on, check the switch control; paragraph 5.10.2.3. If the switch diode is on and the input does not connect to the Model 51 or 52, check the optically coupled FET switch.

The following list identifies some common multiplexer problems and recommmended solutions.

Troubleshooting Guides

Problem	Step	Process	Comment
Inaccurate cold junction temperature from multiplexer.	1.	Verify switch SW1-1 is closed.	
	2.	Review paragraph 5.10.2.4.	
	3.	Check U1C, U4C, U1B, U1D, U18A, U7.	
No input to Model 51 or 52.	1.	Check multiplexer setup; see paragraph 2.3.7 of the *Models 51 and 52 OPerator's Manual.*	
	2.	Check J2 and multiplexer channel switch S1.	Change U8a, B, C, D; U9A, B, C, D; U10A, B, C, D; U11A, B, C, D; U12A, B, C, D; U13A, B, C, D; U14A, B, C, D; U15A, B, C, D; U16A, B, C, D; U17A, B, C, D.
	3.	Check switch matrix diode; review paragraph 5.10.22.	
	4.	Review switch control; see paragraph 5.10.2.3.	Change U3B, U3A, U5.
Thermocouple temperature drifts.	1.	Disconnect thermocouple.	
	2.	Connect a copper wire across the MUX input terminals.	Cold junction (ambient) temperature should be displayed if unit is good. If so, replace thermocouple.

6.4.4.10 Rechargeable Battery Assembly Troubleshooting

Schematic: 0103-00-2724.
Assembly Drawing: 1100-00-2724.
Circuit Description: 5.11.

The following list identifies some common multiplexer problems and recommmended solutions.

Troubleshooting Guide

Problem	Step	Process	Comment
On battery power, no battery voltage at J6-2.	1.	Check the fuse; review paragraph 2.3.2, Battery Charger Fuse in the *Models 51 and 52 Operator's Manual*.	Change Fuse F1.
On external power, the battery does not switch off.	1.	Review paragraph 5.11.3.	Change U2, Q2.
Battery does not charge correctly	1.	Review paragraph 5.11.2.	Change U1, Q1, 12V battery.

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit and, if applicable, the function performed.

7.3 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavekek instrument as quickly as developement and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted inside the shipping carton with this manual.

	DRAWING	**DRAWING NUMBER**
Model 52	Outline Drawing	0002-00-0440
	Instrument Schematic	0004-00-0440
	Model 52 Assembly Drawing	1000-00-0490
	Model 52 Parts List	1000-00-0490
	Chassis	
	Assembly	1101-00-2617
	Parts List	1101-00-2617
	Mother Board	
	Schematic	0103-00-1808
	Assembly Drawing	1100-00-1808
	Parts List	1100-00-1808
	Rear Panel	
	Assembly Drawing	1206-00-2618
	Parts List	1206-00-2618
	Keyboard	
	Schematic	0103-00-2414
	Assembly Drawing	1208-00-2414
	Parts List	1208-00-2414
	Bottom Cover	
	Assembly Drawing	1206-00-2620
	Parts List	1206-00-2620
	Top Cover	
	Assembly Drawing	1206-00-2621
	Parts List	1206-00-2621

	DRAWING	DRAWING NUMBER
Model 51	Model 51 Option Drawing	0002-00-0492
	Model 51 Assembly Drawing	1000-00-0492
	Model 51 Parts List	1000-00-0492
	Chassis	
	Assembly	1101-00-2853
	Parts List	1101-00-2852
	Mother Board	
	Parts List	1100-00-2822
Model 50-1	Measurement Module	
	Parts List	1000-00-0464
	Assembly Drawing	1000-00-0464
	Table 7-1. Measurement Module Signal Sources and Destinations	
	Table 7-2. Measurement Module Power Line Destinations	
	PC Board	
	Assembly Drawing	1100-00-1811
	Parts List	1100-00-1811
	W-10 Cable	
	Assembly Drawing	1207-00-2806
	Parts List	1207-00-2806
Model 50-2	Measurement Module	
	Assembly Drawing	1000-00-0465
	Parts List	1000-00-0465
	PC Board	
	Assembly Drawing	1100-00-2615
	Parts List	1100-00-2615
Option 50-10	Primary Cell Battery	
	Assembly Drawing	1000-00-0466
	Parts List	1000-00-0466
	Assembly Drawing	1207-00-2869
	Parts List	1207-00-2869
Option 50-11	Rechargeable Battery	
	Assembly Drawing	1000-00-0467
	Parts List	1000-00-0467
	Recharger Board	
	Schematic	0103-00-2724
	Assembly Drawing	1100-00-2724
	Parts List	1100-00-2724

	DRAWING	DRAWING NUMBER
Option 50-12-64	64K Expansion RAM	
	Assembly Drawing	1000-00-0468
	Parts List	1000-00-0468
	RAM Board	
	Assembly	1100-00-1817
	Parts List	1100-00-1817
Option 50-12-128	128K Expansion RAM	
	Assembly Drawing	1000-00-0469
	Parts List	1000-00-0469
Option 50-12-192	192K Expansion RAM	
	Assembly Drawing	1000-00-0470
	Parts List	1000-00-0470
Option 50-12-256	256K Expansion RAM	
	Assembly Drawing	1000-00-0471
	Parts List	1000-00-0471
Option 50-14	Digital I/O Board	
	Assembly Drawing	1000-00-0472
	Parts List	1000-00-0472
	PC Board	
	Schematic	0103-00-1814
	Assembly Drawing	1100-00-1814
	Parts List	1100-00-1814
Option 50-20	High Voltage Multiplexer	
	Outline Drawing	0002-00-0473
	Assembly Drawing	1000-00-0473
	Parts List	1000-00-0473
	PC Board	
	Schematic	0103-00-2656
	Assembly Drawing	1100-00-2656
	Parts List	1100-00-2656
Option 50-13	IEEE-488 Board	
	Assembly Drawing	1000-00-0476
	Parts List	1000-00-0476
	PC Board	
	Schematic	0103-00-2451
	Assembly Drawing	1100-00-2451
	Parts List	1100-00-2451
Accessory 50-32	Digital I/O Module	
	Outline Drawing	0002-00-0486
	Assembly Drawing	1000-00-0486
	Parts List	1000-00-0486
	PC Board	
	Schematic	0103-00-2856
	Parts List	1100-00-2856

	DRAWING	DRAWING NUMBER
Option 53-2	16/32 Multiplexer	
	Reference Schematic	0004-00-0498
	Assembly Drawing	1000-00-0498
	Parts List	1000-00-0498
	PC Board	
	Schematic	0103-00-2886
	Assembly Drawing	1100-00-2886
	Parts List	1100-00-2886
	Parts List	1208-00-2953
Option 53-1	32/64 Multiplexer	
	Reference Schematic	0004-00-0499
	Assembly Drawing	1000-00-0499
	Parts List	1000-00-0499
	PC Board	
	Schematic	0103-00-2877
	Assembly Drawing	1100-00-2877
	Parts List	1100-00-2877
	Parts List	1208-00-2954

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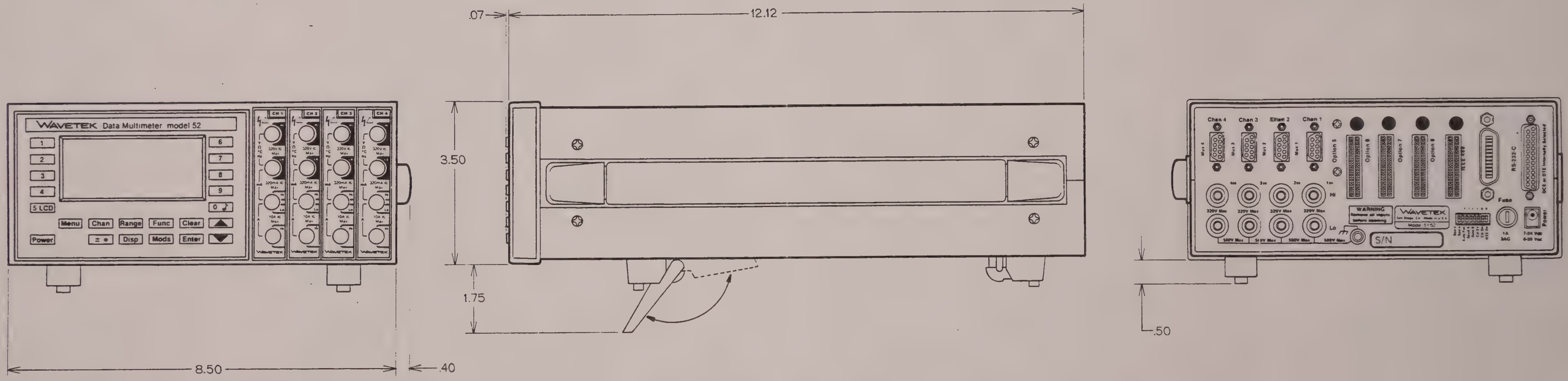

WAVETEK Data Multimeter model 52
1
2
3
4
5 LCD
6
7
8
9
0
Menu
Chan
Range
Func
Clear
Power
±
Disp
Mods
Enter
CH 1
CH 2
CH 3
CH 4
.07
12.12
3.50
1.75
8.50
.40
.50
Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS-232-C
WARNING
S/N
Fuse
Power

1. UNIT WEIGHT: 3.85 KG. (8.5 LBS.) NET,
(WITH BATTERY OPTION ADD 1.25 KG. (2.75 LBS.);
SHIPPING (WITHOUT BATTERY): 5.0 KG. (11.00 LBS.).

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 4/1/86	WAVETEK SAN DIEGO • CALIFORNIA		
MATERIAL	PROJ ENGR N. E. Miller	4/10/86	TITLE OUTLINE DRAWING, MODEL 52		
	RELEASE APPROV C. Seagrave 4-17-86				
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.050				
	DO NOT SCALE DWG		MODEL NO 52	DWG NO. 0002-00-0440	REV A
	SCALE NONE		CODE IDENT 23338	SHEET 1 OF 1	

0002-00-0440 A

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

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A	FOR RELEASE	A.T.		N.M.
B	#7600	A.T.		A.R.T.
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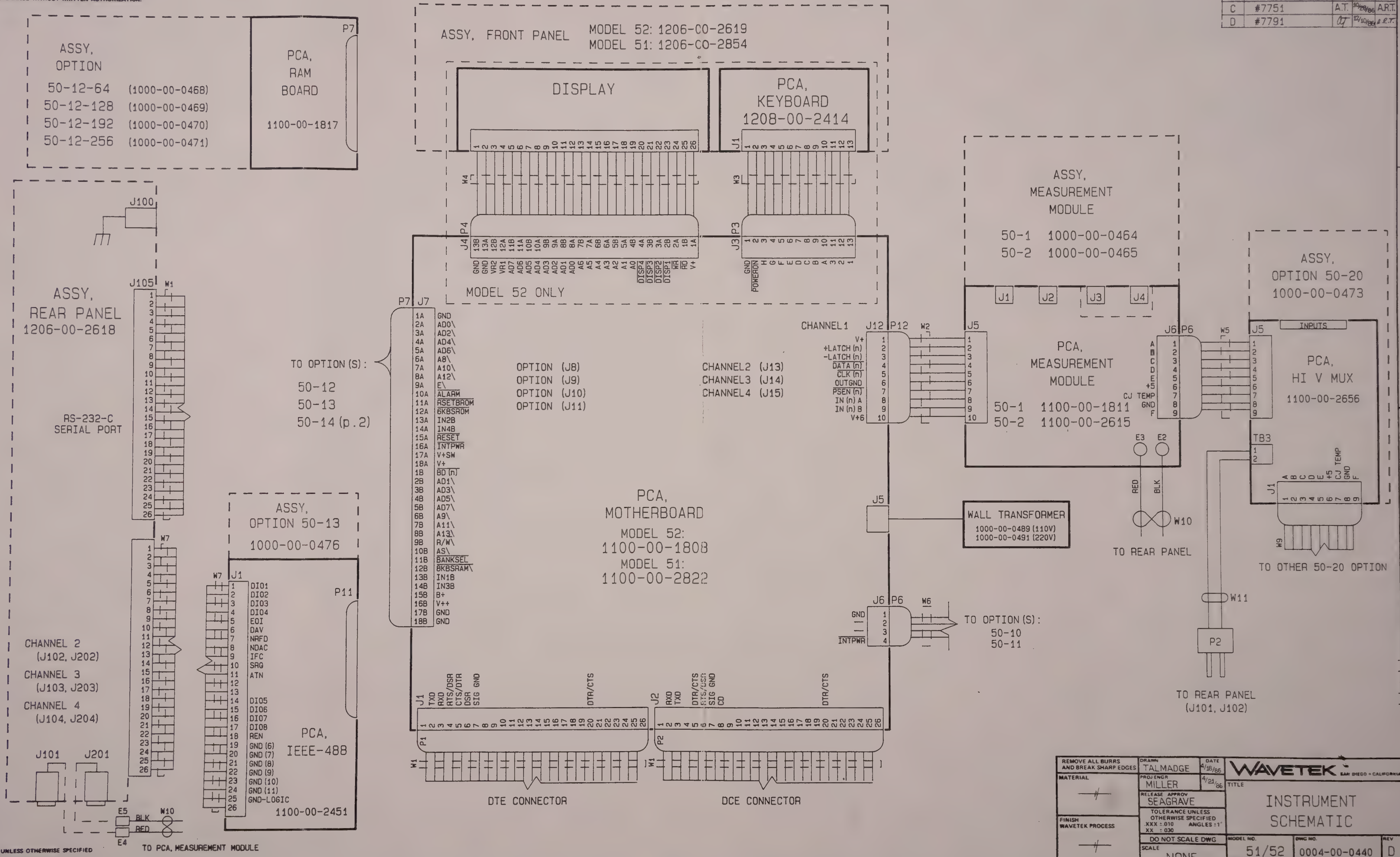
D	#7791	AT	12/10/86	A.R.T.

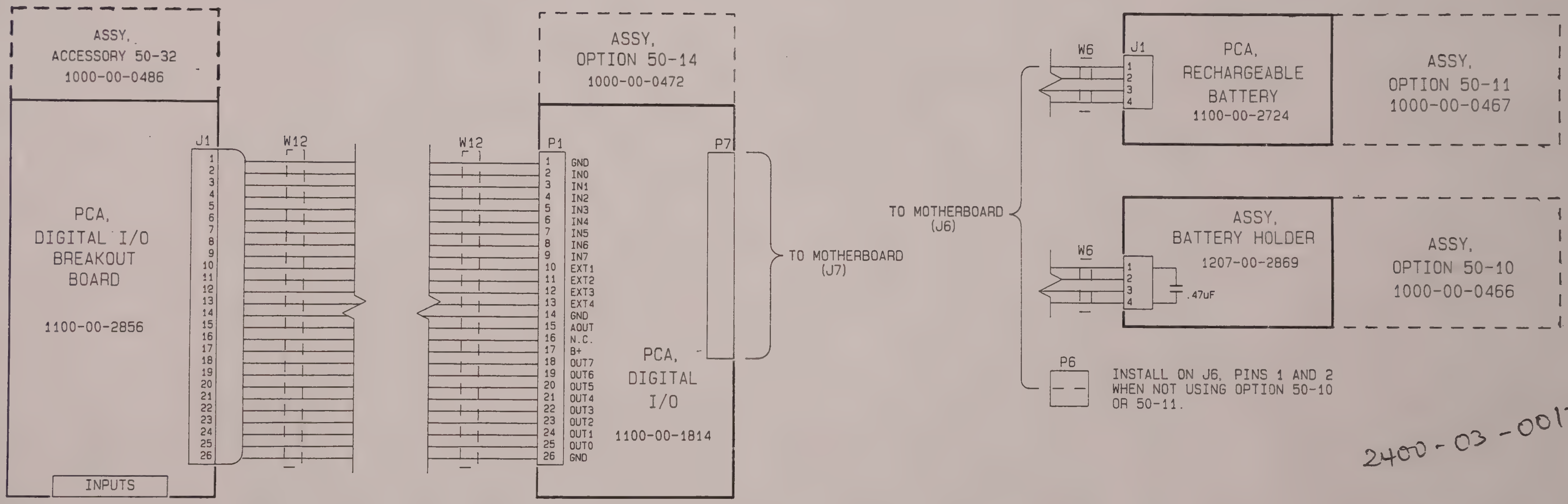

ASSY, OPTION
50-12-64 (1000-00-0468)
50-12-128 (1000-00-0469)
50-12-192 (1000-00-0470)
50-12-256 (1000-00-0471)
P7
PCA, RAM BOARD
1100-00-1817
ASSY, FRONT PANEL
MODEL 52: 1206-C0-2619
MODEL 51: 1206-C0-2854
DISPLAY
PCA, KEYBOARD
1208-00-2414
W4
J1
W3
J4 P4
13B 13A 12B 12A 11B 11A 10B 10A 9B 9A 8B 8A 7B 7A 6B 6A 5B 5A 4B 4A 3B 3A 2B 2A 1B 1A
GND GND VR2 VR1 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 A6 A5 A4 A3 A2 A1 A0 DISP4 DISP3 DISP2 DISP1 WR RD V+
J3 P3
1 2 3 4 5 6 7 8 9 10 11 12 13
GND POWERON H G F E D C B A 3 2 1
MODEL 52 ONLY
ASSY, MEASUREMENT MODULE
50-1 1000-00-0464
50-2 1000-00-0465
J1 J2 J3 J4
ASSY, OPTION 50-20
1000-00-0473
J100
J105
W1
ASSY, REAR PANEL
1206-00-2618
RS-232-C SERIAL PORT
W7
CHANNEL 2 (J102, J202)
CHANNEL 3 (J103, J203)
CHANNEL 4 (J104, J204)
J101 J201
E5 BLK RED W10 E4
TO PCA, MEASUREMENT MODULE
TO OPTION (S):
50-12
50-13
50-14 (p.2)
P7 J7
1A GND
2A AD0\
3A AD2\
4A AD4\
5A AD6\
6A A8\
7A A10\
8A A12\
9A E\
10A ALARM
11A RSETBROM
12A 6KBSROM
13A IN2B
14A IN4B
15A RESET
16A INTPWR
17A V+SW
18A V+
1B BD (n)
2B AD1\
3B AD3\
4B AD5\
5B AD7\
6B A9\
7B A11\
8B A13\
9B R/W\
10B AS\
11B BANKSEL
12B 8KBSRAM\
13B IN1B
14B IN3B
15B B+
16B V++
17B GND
18B GND
OPTION (J8)
OPTION (J9)
OPTION (J10)
OPTION (J11)
CHANNEL2 (J13)
CHANNEL3 (J14)
CHANNEL4 (J15)
CHANNEL 1
J12 P12
W2
1 V+
2 +LATCH (n)
3 -LATCH (n)
4 DATA (n)
5 CLK (n)
6 OUTGND
7 PSEN (n)
8 IN (n) A
9 IN (n) B
10 V+6
J5
PCA, MEASUREMENT MODULE
50-1 1100-00-1811
50-2 1100-00-2615
J6 P6
W5
A B C D E +5 CJ TEMP GND F
E3 E2
RED BLK
W10
TO REAR PANEL
J5
INPUTS
PCA, HI V MUX
1100-00-2656
TB3
1 2
J1
A B C D E +5 CJ TEMP GND F
W9
TO OTHER 50-20 OPTION
W11
P2
TO REAR PANEL (J101, J102)
ASSY, OPTION 50-13
1000-00-0476
W7 J1
1 DIO1
2 DIO2
3 DIO3
4 DIO4
5 EOI
6 DAV
7 NRFD
8 NDAC
9 IFC
10 SRG
11 ATN
14 DIO5
15 DIO6
16 DIO7
17 DIO8
18 REN
19 GND (6)
20 GND (7)
21 GND (8)
22 GND (9)
23 GND (10)
24 GND (11)
25 GND-LOGIC
P11
PCA, IEEE-488
1100-00-2451
PCA, MOTHERBOARD
MODEL 52: 1100-00-1808
MODEL 51: 1100-00-2822
J5
WALL TRANSFORMER
1000-00-0489 (110V)
1000-00-0491 (220V)
J6 P6
W6
GND
INTPWR
TO OPTION (S):
50-10
50-11
J1 TXD RXD RTS/DSR CTS/DTR DSR SIG GND DTR/CTS
P1
W1
DTE CONNECTOR
J2 RXD TXD DTR/CTS RTS/DSR SIG GND CD DTR/CTS
P2
W1
DCE CONNECTOR

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN TALMADGE	DATE 4/18/86	**WAVETEK** SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR MILLER	4/21/86	TITLE INSTRUMENT SCHEMATIC
	RELEASE APPROV SEAGRAVE		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52
	SCALE NONE		DWG NO. 0004-00-0440
			REV D
			CODE IDENT 23338
			SHEET 1 OF 2

0004-00-0440 D

REV	ECN	BY	DATE	APP


ASSY,
ACCESSORY 50-32
1000-00-0486
PCA,
DIGITAL I/O
BREAKOUT
BOARD
1100-00-2856
INPUTS
J1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
W12
W12
ASSY,
OPTION 50-14
1000-00-0472
P1
1 GND
2 IN0
3 IN1
4 IN2
5 IN3
6 IN4
7 IN5
8 IN6
9 IN7
10 EXT1
11 EXT2
12 EXT3
13 EXT4
14 GND
15 AOUT
16 N.C.
17 B+
18 OUT7
19 OUT6
20 OUT5
21 OUT4
22 OUT3
23 OUT2
24 OUT1
25 OUT0
26 GND
P7
PCA,
DIGITAL
I/O
1100-00-1814
TO MOTHERBOARD
(J7)
TO MOTHERBOARD
(J6)
W6
J1
1
2
3
4
PCA,
RECHARGEABLE
BATTERY
1100-00-2724
ASSY,
OPTION 50-11
1000-00-0467
W6
1
2
3
4
.47uF
ASSY,
BATTERY HOLDER
1207-00-2869
ASSY,
OPTION 50-10
1000-00-0466
P6

INSTALL ON J6, PINS 1 AND 2
WHEN NOT USING OPTION 50-10
OR 50-11.

2400-03-0017

224.

0004-00-0440 D

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN A.TALMADGE
DATE 4/10/86
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
XX ±.030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
INSTRUMENT
SCHEMATIC
MODEL NO. 51/52
DWG NO. 0004-00-0440
REV D
CODE IDENT 23338
SHEET 2 OF 2

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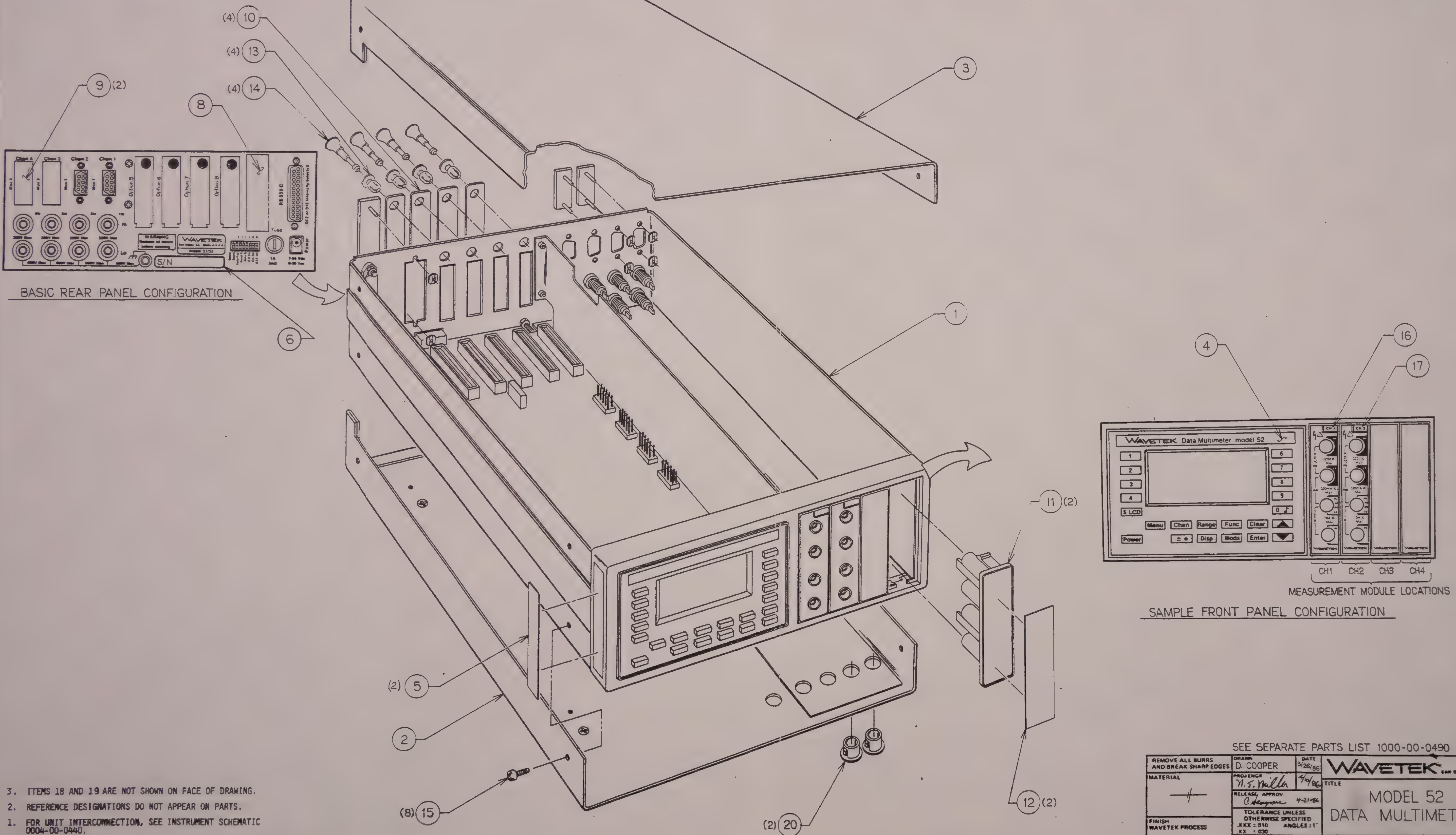

(4) 10
(4) 13
(4) 14
9 (2)
8
3
Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS 232 C
WARNING
WAVETEK
Model 31/52
Fuse
Power
S/N
BASIC REAR PANEL CONFIGURATION
6
1
4
16
17
WAVETEK Data Multimeter model 52
1
2
3
4
5 LCD
6
7
8
9
0
Menu
Chan
Range
Func
Clear
Power
±
Disp
Mode
Enter
CH1
CH2
CH3
CH4
MEASUREMENT MODULE LOCATIONS
SAMPLE FRONT PANEL CONFIGURATION
11 (2)
(2) 5
2
(8) 15
(2) 20
12 (2)

3. ITEMS 18 AND 19 ARE NOT SHOWN ON FACE OF DRAWING.
2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0490

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN D. COOPER DATE 3/26/86
PROJ ENGR N. S. Miller 4/10/86
RELEASE, APPROV 4-21-86

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
MODEL 52
DATA MULTIMETER

MODEL NO 52
DWG NO. 1000-00-0490
REV A
CODE IDENT 23338
SHEET 1 OF 1

1000-00-0490 A

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	OUTLINE DRAWING-52	0002-00-0440	WVTK	0002-00-0440	1
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
1	ASSY, CHASSIS	1101-00-2617	WVTK	1101-00-2617	1
2	ASSY, BOTTOM COVER	1206-00-2620	WVTK	1206-00-2620	1
3	ASSY, TOP COVER	1206-00-2621	WVTK	1206-00-2621	1
NONE	MODEL 52 INSTRUCTION MANUAL	1300-00-0440	WVTK	1300-00-0440	1. 3
6	SERIAL TAG MODEL 602	602-6950	WVTK	1400-01-6950	1
11	FRONT PANEL, BLANK	52-0860	WVTK	1400-02-0860	2
16	LABEL CHANNEL 1	52-1110	WVTK	1400-02-1110	1
17	LABEL, CHANNEL 2	52-1120	WVTK	1400-02-1120	1
18	LABEL CHANNEL, 3	52-1130	WVTK	1400-02-1130	1
19	LABEL CHANNEL, 4	52-1140	WVTK	1400-02-1140	1
12	DECAL, BLANK CHANNEL	52-1150	WVTK	1400-02-1150	2
4	LOGO, FRONT PANEL, MODEL 52	52-1160	WVTK	1400-02-1160	1
5	DECAL, SIDE TRIM	52-1200	WVTK	1400-02-1200	2

WAVETEK
PARTS LIST
TITLE
MODEL 52 DATA MULTIMETER
ASSEMBLY NO.
1000-00-0490
REV
A
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
10	COVER, DIGITAL I/O	1400-02-1593	WVTK	1400-02-1593	4
15	MACHINE SCREW, PANHEAD, PHLPS, W/NYLOCK PATCH	6-32X3/16 PAN LOK BLK	CMRCL	2800-23-6103	8
20	PLUG BUTTON, NYLON, 17/32 HEAD, BLACK	2633	HEYCO	2800-35-0007	2
13	NYLATCH GROMMET, 1/4 HOLE ONE OF TWO PARTS	HN4043-1	HART	2800-60-0004	4
14	NYLATCH PLUNGER, 1/4 HOLE, ONE OF TWO PARTS	HN4P43-4-1	HART	2800-60-0005	4
NONE	TEST LEAD SET, 48 INCH	3000-00-0156	WVTK	3000-00-0156	1
NONE	INSERT	101-18	WVTK	3300-00-0015	1
NONE	CARTON	101-18A	WVTK	3300-01-0012	1
8	COVER, CONNECTOR CUT-OUT	12-24R BLACK	PEPER	3300-03-0002	1
9	COVER, CONNECTOR CUT-OUT	10-9 BLACK	PEPER	3300-03-0003	2

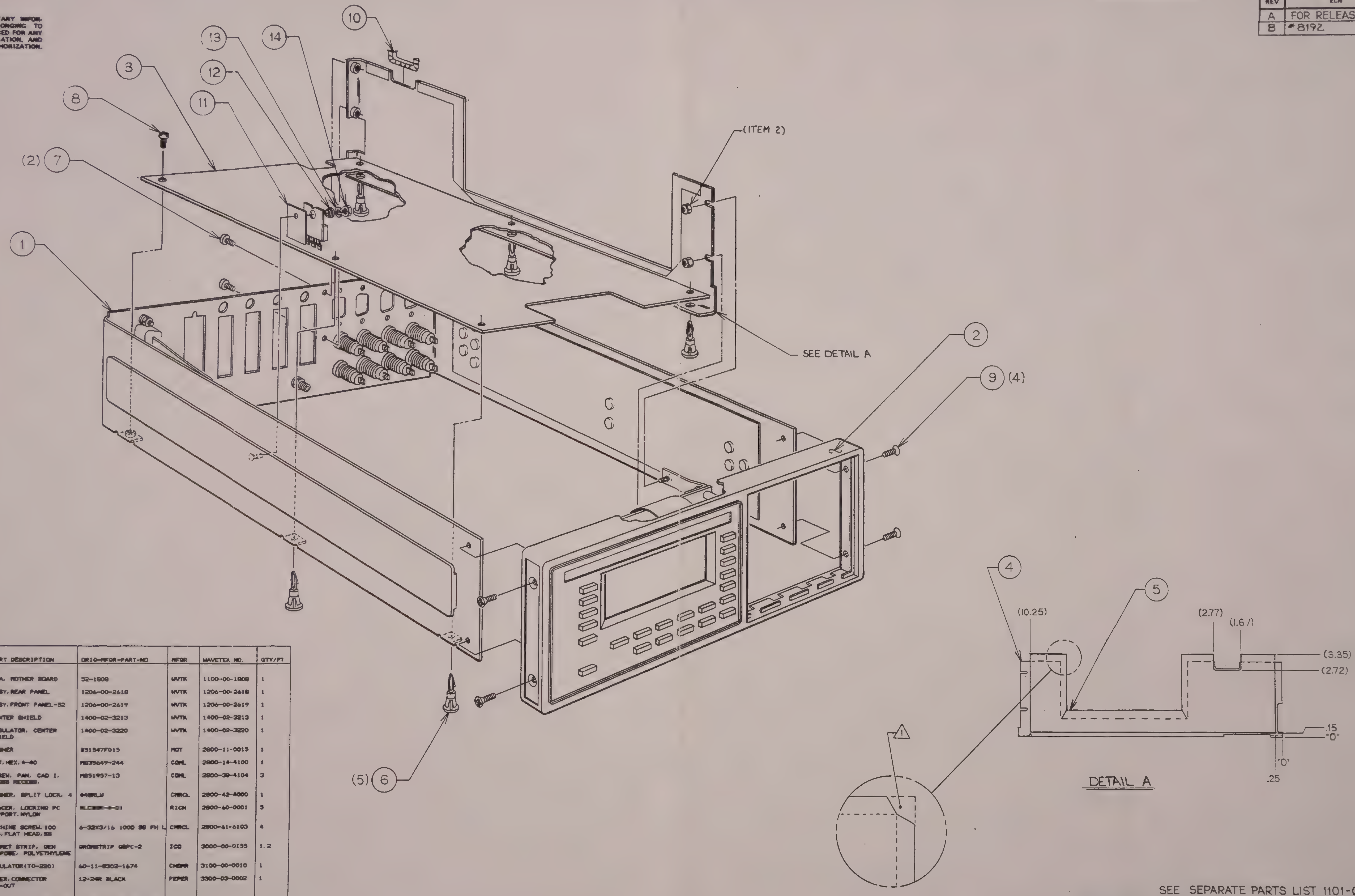
WAVETEK
PARTS LIST
TITLE
MODEL 52 DATA MULTIMETER
ASSEMBLY NO.
1000-00-0490
REV
A
PAGE 2

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
DATA MULTIMETER
SIZE D
FSCM NO. 23338
DWG. NO. 1000-00-0490
REV A
SCALE
MODEL 52
SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE	AT	3/25/86	DM
B	#8192	J.E. 4-22-87	4-30-87	RRT



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
3	PCA, MOTHER BOARD	52-1808	WVTK	1100-00-1808	1
1	ASSY, REAR PANEL	1206-00-2618	WVTK	1206-00-2618	1
2	ASSY, FRONT PANEL-52	1206-00-2619	WVTK	1206-00-2619	1
4	CENTER SHIELD	1400-02-3213	WVTK	1400-02-3213	1
5	INSULATOR, CENTER SHIELD	1400-02-3220	WVTK	1400-02-3220	1
12	WASHER	931547F015	MOT	2800-11-0015	1
14	NUT, HEX, 4-40	MS35649-244	COML	2800-14-4100	1
8 7	SCREW, PAN, CAD I, CROSS RECESS,	MS51957-13	COML	2800-39-4104	3
13	WASHER, SPLIT LOCK, 4	04SRLW	CMRCL	2800-42-4000	1
6	SPACER, LOCKING PC SUPPORT, NYLON	[redacted]	RICH	2800-60-0001	5
9	MACHINE SCREW, 100 DEG, FLAT HEAD, SS	6-32X3/16 100D SS FH L	CMRCL	2800-61-6103	4
10	GROMET STRIP, GEN PURPOSE, POLYETHYLENE	GROMSTRIP GSPC-2	ICO	3000-00-0135	1.2
11	INSULATOR (TO-220)	60-11-8302-1674	CHOMR	3100-00-0010	1
NONE	COVER, CONNECTOR CUT-OUT	12-24R BLACK	PEPER	3300-03-0002	1

WAVETEK PARTS LIST
TITLE ASSY, CHASSIS
ASSEMBLY NO. 1101-00-2617
REV B
PAGE 1

⚠1 SMOOTH INSULATOR (ITEM 5) OVER EDGES OF CENTER SHIELD (ITEM 4) AND FOLD IT DOWN ONTO REAR SIDE. FOLD CORNER OVER FIRST THEN FOLD ADJACENT SIDES OVER ON TOP OF CORNER, HOLDING IT DOWN.

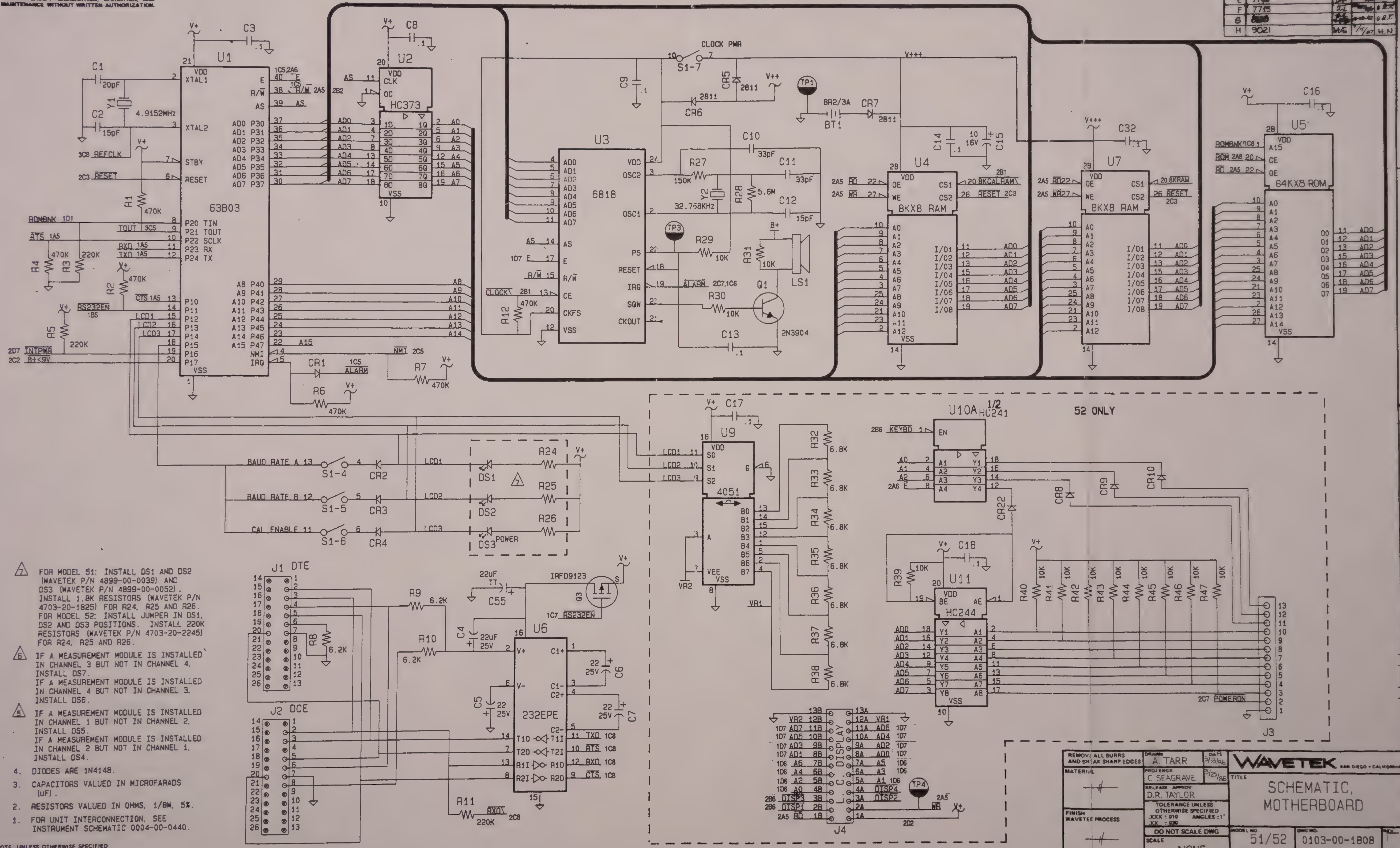
NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1101-00-2617

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL —
FINISH WAVETEK PROCESS —
DRAWN D. COOPER DATE 3/12/86
PROJ ENGR N. S. Muller 3/26/86
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE ASSEMBLY, CHASSIS
MODEL NO 51/52
DWG NO 1101-00-2617
REV B
CODE IDENT 23338
SHEET 1 OF 1

1101-00-2617 B

REV	[illegible]	BY	DATE	APP
C	[illegible]			
D	7332	A.T.	[illegible]	A.R.T.
E	7790	[illegible]	3/25/86	A.R.T.
F	7715	[illegible]	[illegible]	A.R.T.
G	[illegible]	[illegible]	[illegible]	A.R.T.
H	9021	M.G.	7/5/87	H.N.
J	#9108	A.T.	3/28/87	A.R.T.
K	#9204	A.T.	10/21/87	A.R.T.


U1
63B03
U2
HC373
U3
6818
U4
8KX8 RAM
U7
8KX8 RAM
U5
64KX8 ROM
U6
232EPE
U9
4051
U10A 1/2 HC241
U11
HC244
52 ONLY
Y1 4.9152MHz
Y2 32.768KHz
CLOCK PWR
S1-7
BT1 BR2/3A
TP1
TP2
TP3
TP4
Q1 2N3904
Q3 IRFD9123
LS1
BAUD RATE A
BAUD RATE B
CAL ENABLE
S1-4
S1-5
S1-6
DS1
DS2
DS3
POWER
J1 DTE
J2 DCE
J3
J4
L.C. DISPLAY
VDD
VSS
V+
V++
V+++
B+
XTAL1
XTAL2
STBY
RESET
REFCLK
ROMBNK
RTS
CTS
RXD
TXD
RS232EN
INTPWR
B+<9V
LCD1
LCD2
LCD3
NMI
IRQ
ALARM
AS
R/W
E
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
A8
A9
A10
A11
A12
A13
A14
A15
CLOCK
RD
WR
8KCALRAM
8KRAM
ROM
KEYBD
POWERON
DISP1
DISP2
DISP3
DISP4
VR1
VR2
C1 20pF
C2 15pF
C10 33pF
C11 33pF
C12 15pF
C13 .1
C4 22uF 25V
C5 22 25V
C6 22 25V
C7 22 25V
C55 22uF
C15 10 16V
R1 470K
R2 470K
R3 220K
R4 470K
R5 220K
R6 470K
R7 470K
R8 6.2K
R9 6.2K
R10 6.2K
R11 220K
R12 470K
R27 150K
R28 5.6M
R29 10K
R30 10K
R31 10K
R32 6.8K
R33 6.8K
R34 6.8K
R35 6.8K
R36 6.8K
R37 6.8K
R38 6.8K
R39 10K
R40 10K
R41 10K
R42 10K
R43 10K
R44 10K
R45 10K
R46 10K
R47 10K
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR22

- ⚠7 FOR MODEL 51: INSTALL DS1 AND DS2 (WAVETEK P/N 4899-00-0039) AND DS3 (WAVETEK P/N 4899-00-0052). INSTALL 1.8K RESISTORS (WAVETEK P/N 4703-20-1825) FOR R24, R25 AND R26. FOR MODEL 52: INSTALL JUMPER IN DS1, DS2 AND DS3 POSITIONS. INSTALL 220K RESISTORS (WAVETEK P/N 4703-20-2245) FOR R24, R25 AND R26.
- ⚠6 IF A MEASUREMENT MODULE IS INSTALLED IN CHANNEL 3 BUT NOT IN CHANNEL 4, INSTALL DS7.
  IF A MEASUREMENT MODULE IS INSTALLED IN CHANNEL 4 BUT NOT IN CHANNEL 3, INSTALL DS6.
- ⚠5 IF A MEASUREMENT MODULE IS INSTALLED IN CHANNEL 1 BUT NOT IN CHANNEL 2, INSTALL DS5.
  IF A MEASUREMENT MODULE IS INSTALLED IN CHANNEL 2 BUT NOT IN CHANNEL 1, INSTALL DS4.

4. DIODES ARE 1N4148.
3. CAPACITORS VALUED IN MICROFARADS (uF).
2. RESISTORS VALUED IN OHMS, 1/8W, 5%.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN	A. TARR	3/18/86
PROJ ENGR	C SEAGRAVE	3/25/86
RELEASE APPROV	D.R. TAYLOR	

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC, MOTHERBOARD

MODEL NO. 51/52

DWG NO. 0103-00-1808

REV

CODE IDENT 23338

SHEET 1 OF 3

0103-00-1808

BISHOP GRAPHICS/ACCUPRESS REORDER NO A2708

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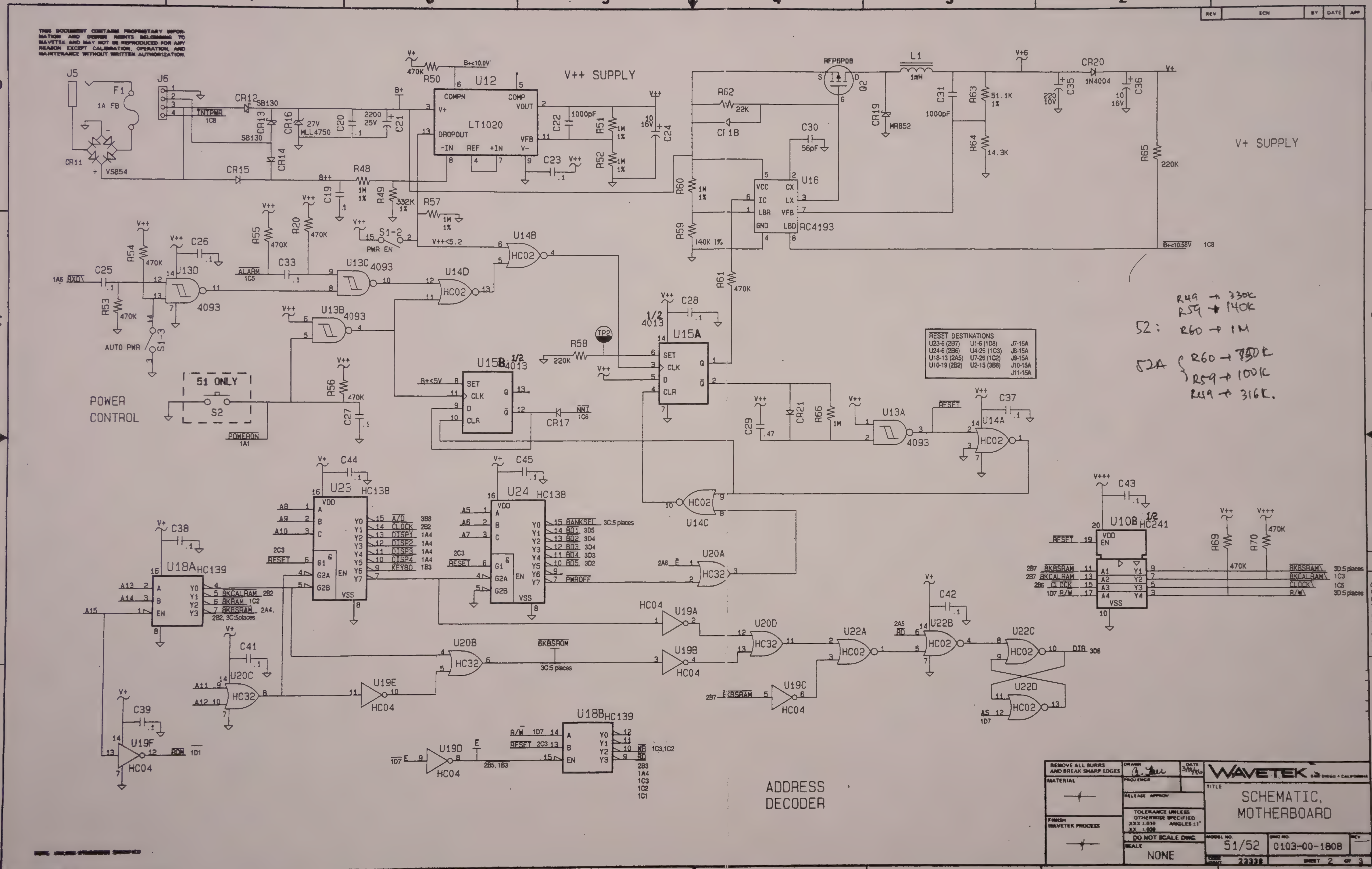

V++ SUPPLY
V+ SUPPLY
POWER CONTROL
ADDRESS DECODER
J5
J6
F1
1A FB
CR11
VSB54
CR12
SB130
CR13
CR14
CR15
CR16
27V
MLL4750
C20
C21
2200
25V
U12
LT1020
COMPN
COMP
VOUT
DROPOUT
VFB
-IN
REF
+IN
V-
B+<10.0V
R50
470K
C22
1000pF
R51
R52
1M 1%
C23
C24
10 16V
R48
R49
332K 1%
R57
C19
INTPWR
Q2
RFP6P08
L1
1mH
CR19
MR852
C31
1000pF
R63
51.1K 1%
R64
14.3K
C35
220 10V
CR20
1N4004
C36
10 16V
V+6
R65
220K
R62
22K
CR18
C30
56pF
U16
RC4193
VCC
CX
IC
LX
LBR
VFB
GND
LBD
R60
1M 1%
R59
140K 1%
R61
470K
B+<10.58V
S1-2
PWR EN
V++<5.2
U14B
HC02
U14D
U13C
4093
U13D
U13B
C25
RXD\
C26
C33
ALARM
R53
R54
R55
R20
470K
S1-3
AUTO PWR
51 ONLY
S2
R56
C27
POWERON
U15A
U15B
1/2 4013
SET
CLK
D
CLR
Q
R58
220K
TP2
C28
B+<5V
CR17
NMI
CR21
C29
.47
R66
1M
U13A
RESET
U14A
C37
U14C
U20A
HC32
U23
HC138
C44
VDD
VSS
G1
G2A
G2B
A8
A9
A10
A/D
CLOCK
DISP1
DISP2
DISP3
DISP4
KEYBD
U24
C45
A5
A6
A7
BANKSEL
BD1
BD2
BD3
BD4
BD5
PWROFF
U18A
HC139
C38
A13
A14
A15
BKCALRAM
BKRAM
BKBSRAM
U20B
U20C
C41
A11
A12
U19E
HC04
BKBSROM
U19A
U19B
U20D
U22A
U22B
C42
U22C
U22D
DIR
AS
U19C
BSRAM
U19F
C39
ROM
U19D
U18B
R/W
WR
RD
U10B
HC241
C43
V+++
R69
R70
470K

RESET DESTINATIONS		
U23-6 (2B7)	U1-6 (1D8)	J7-15A
U24-6 (2B6)	U4-26 (1C3)	J8-15A
U18-13 (2A5)	U7-26 (1C2)	J9-15A
U10-19 (2B2)	U2-15 (3B8)	J10-15A
		J11-15A

R49 → 330K
R59 → 140K
52: R60 → 1M

52A { R60 → 850K
R59 → 100K
R49 → 316K.

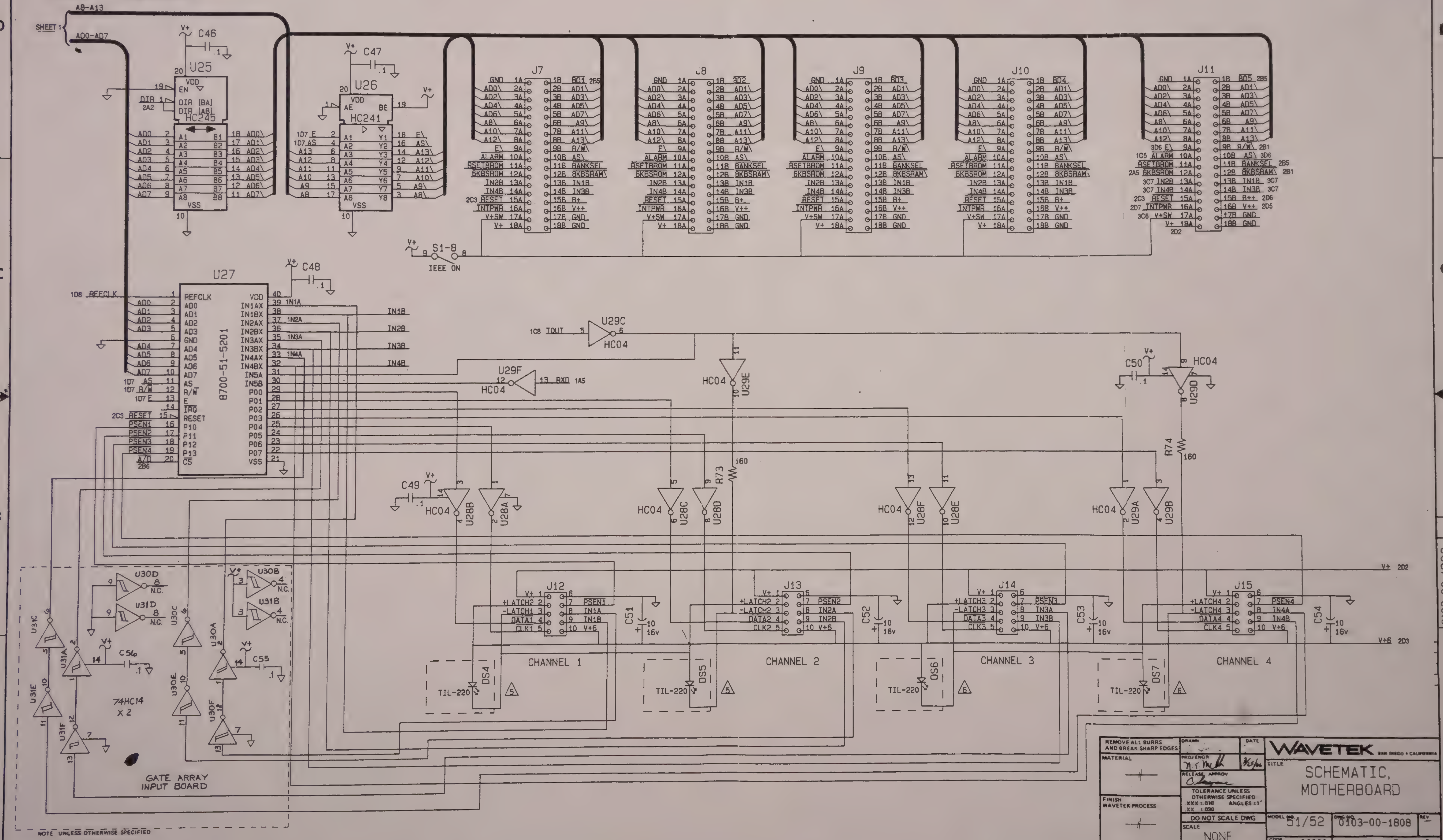
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN A. Lee
DATE 3/13/96
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC, MOTHERBOARD

MODEL NO. 51/52
DWG NO. 0103-00-1808
REV
CODE IDENT 23338
SHEET 2 OF 3

0103-00-1808


8 7 6 5 4 3 2 1
D C B A
SHEET 1
A8-A13
AD0-AD7
U25
HC245
C46
U26
HC241
C47
J7
J8
J9
J10
J11
GND
AD0\ AD1\ AD2\ AD3\ AD4\ AD5\ AD6\ AD7\
A8\ A9\ A10\ A11\ A12\ A13\
E\
AS\
R/W\
ALARM
RSETBROM
BANKSEL
6KBSROM
8KBSRAM
IN1B IN2B IN3B IN4B
RESET
INTPWR
B+
V++
V+SW
V+
S1-8
IEEE ON
U27
8700-51-5201
C48
REFCLK
IRQ
PSEN1 PSEN2 PSEN3 PSEN4
A/D
CS
IN1A IN2A IN3A IN4A
U29C
TOUT
HC04
U29F
RXD
U29E
U29D
C50
R74
160
R73
160
C49
U28B
U28A
U28C
U28D
U28F
U28E
U29A
U29B
J12
J13
J14
J15
+LATCH1 -LATCH1 DATA1 CLK1
+LATCH2 -LATCH2 DATA2 CLK2
+LATCH3 -LATCH3 DATA3 CLK3
+LATCH4 -LATCH4 DATA4 CLK4
V+6
C51 C52 C53 C54
10 16v
CHANNEL 1
CHANNEL 2
CHANNEL 3
CHANNEL 4
DS4 DS5 DS6 DS7
TIL-220
U30D U31D U30B U31B
N.C.
U31C U31A U31E U31F
U30C U30A U30E U30F
C56 C55
74HC14
X 2
GATE ARRAY
INPUT BOARD
NOTE: UNLESS OTHERWISE SPECIFIED
0103-00-1808

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN

DATE

PROJ ENGR N. T. Mc

3/25/86

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
MOTHERBOARD

MODEL NO. 51/52

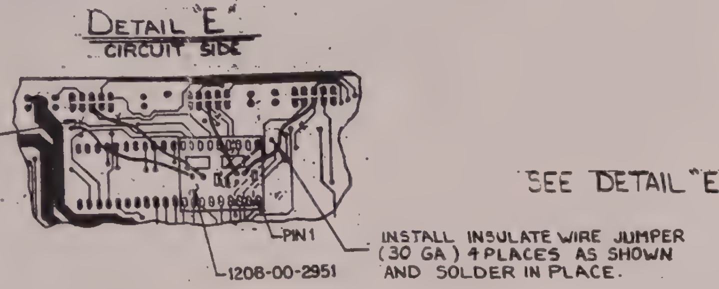
DWG NO. 0103-00-1808

REV —

CODE IDENT 23338

SHEET 3 OF 3

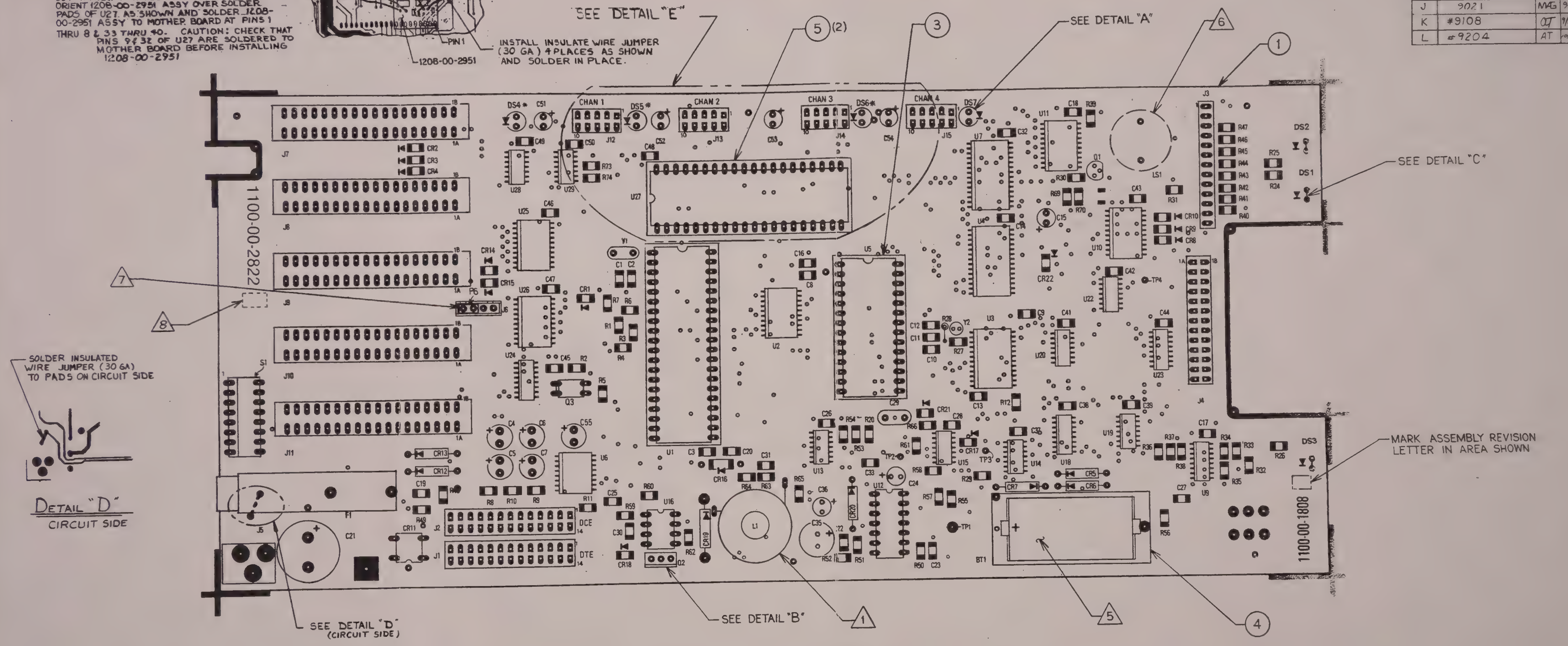
[illegible]	[illegible]	BY	DATE	APP
C	FOR RELEASE	AT	3/13/86	NM
D	# 7332, 7379	OT	4/22/86	A C T
E	#7700	OT	9/24/86	A R.T.
F	#7751	OT	10/28/86	A R.T.
G	# 7989	N.C.	2/6/87	A R T
H	# 8130	N.C. 4-9-87	4-10-87	A.R.T.
J	9021	MAG	9-15-87	H N
K	#9108	OT	9/29/87	A R T.
L	#9204	AT	10/22/87	A R T


PIN 1
1208-00-2951

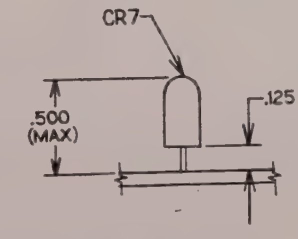
DETAIL "E"
CIRCUIT SIDE

CUT TRACES 4 PLACES "X" ON CIRCUIT SIDE. ORIENT 1208-00-2951 ASSY OVER SOLDER PADS OF U27 AS SHOWN AND SOLDER 1208-00-2951 ASSY TO MOTHER BOARD AT PINS 1 THRU 8 & 33 THRU 40. CAUTION: CHECK THAT PINS 9 & 32 OF U27 ARE SOLDERED TO MOTHER BOARD BEFORE INSTALLING 1208-00-2951

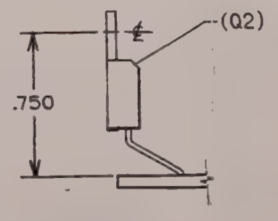
INSTALL INSULATE WIRE JUMPER (30 GA) 4 PLACES AS SHOWN AND SOLDER IN PLACE.


SEE DETAIL "E"
5 (2)
3
SEE DETAIL "A"
6
1
SEE DETAIL "C"
7
8
1100-00-2822
1100-00-1808
CHAN 1
CHAN 2
CHAN 3
CHAN 4
J7
J8
J9
J10
J11
J12
J13
J14
J15
J1
J2
J3
J4
J5
J6
P6
S1
U1
U2
U3
U27
LS1
L1
BT1
F1
DS1
DS2
DS3
DCE
DTE
SEE DETAIL "B"
1
5
4
SEE DETAIL "D" (CIRCUIT SIDE)
MARK ASSEMBLY REVISION LETTER IN AREA SHOWN
SOLDER INSULATED WIRE JUMPER (30 GA) TO PADS ON CIRCUIT SIDE

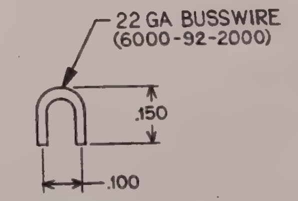
DETAIL "D"
CIRCUIT SIDE


CR7
.500 (MAX)
.125

DETAIL "A"



DETAIL "B"


22 GA BUSSWIRE (6000-92-2000)
.150
.100

DETAIL "C"
(3 PLACES)

8. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.

7. INSTALL P6 ON J6 PINS 1 & 2. REMOVE WHEN USING BATTERY OPTION 50-10 OR 50-11.

6. INSTALL LS1 ON CIRCUIT SIDE OF BOARD.

5. INSTALL BATTERY (BT1) USING A THIN PIECE OF MYLAR (OR EQUIV.) TO INSULATE "+" END OF BATTERY FROM IT'S CONTACT ONLY AFTER ALL SOLDER OPERATIONS ARE COMPLETED.

4. * = TRIM. INSTALLATION TO BE DETERMINED AT UNIT TEST.

3. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

2. SEE C103-00-1808 FOR SCHEMATIC.

1. APPLY RTV (WAVETEK #1600-03-0004) PERMANENTLY BONDING L1 TO SURFACE OF CIRCUIT BOARD.

NOTES:

SEE SEPARATE PARTS LIST 1100-00-1808

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL —
FINISH WAVETEK PROCESS —
DRAWN A.TALMADGE DATE 1/21/86
PROJ ENGR N.E.MILLER 3/25/86
RELEASE APPROV C. SEAGRAVE
TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ±.010 ANGLES ±1
.XX ±.030
DO NOT SCALE DWG
SCALE 2/1

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PCA,
MOTHER BOARD

MODEL NO 52
DWG NO. 1100-00-1808
REV L
CODE IDENT 23338
SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC PCA, MOTHER BOARD	0103-1808	WVTK	0103-00-1808	1
NONE	ASSY, GATE ARRAY PIGGYBACK	1208-00-2951	WVTK	1208-00-2951	1
C29	CAP, CER, MON, .47UF, 20%, 50V, 25U	CRC230Z5U474M050	CORNG	1500-04-7406	1
C15 C24 C36 C51 C52 C53 C54	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	7
C35	CAP, ELECT, 220MF/10V	ECEA1AU221	PANAS	1500-32-2001	1
C4 C5 C55 C6 C7	CAP, ELECT, 22MF/25V	SRA25VB22MC	UNCON	1500-32-2002	5
C21	CAP, ELECT, 2200MF, 25V RADIAL LEAD	ECEA1EV222S	PANAS	1500-32-2202	1
C22 C31	SMD, CAP, CER, 2%, 50V, 1000PF	C1206C102J2GAC	KEMET	1500-81-0201	2
C13 C14 C16 C17 C18 C19 C20 C23 C25 C26 C27 C28 C3 C32 C33 C37 C38 C39 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C8 C9	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	30
C12 C2	SMD, CAP, CER, 2%, 50V, 15PF	C1206C150J2GAC	KEMET	1500-81-5001	2
C1	SMD, CAP, CER, 2%, 50V, 20PF	C1206C200G5GAC	KEMET	1500-82-0001	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD
ASSEMBLY NO. 1100-00-1808
REV L
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C10 C11	SMD, CAP, CER, 2%, 50V, 33PF	C1206C330J2GAC	KEMET	1500-83-3001	2
C30	SMD, CAP, CER, 2%, 50V, 56PF	C1206C560J2GAC	KEMET	1500-85-6001	1
L1	CHOKE, TORROIDAL, 1MH	4294	CASYS	1800-00-0025	1
J6	CONNECTOR, HEADER (4 PIN)	102202-1	AMP	2100-02-0131	1
J1 J2 J4	CONN, HEADER 26 PIN/2 ROW	929836-01-13	A/P	2100-02-0156	3
J10 J11 J7 J8 J9	CONNECTOR, EDGE 36 PIN	ETC18DRXN	SULL	2100-02-0191	5
J5	CONNECTOR POWER JACK	16PJ032	MOUSR	2100-02-0192	1
J12 J13 J14 J15	CONNECTOR, HEADER, DOUBLE 5 PIN ROWS, 0.1X0.1	929836-01-05	APTRN	2100-02-0212	4
P6	JUMPER, FEMALE, 2 POSITION, 0.1 SPACE	929950-00	APTRN	2100-02-0213	1
J3	CONNECTOR, HEADER, 13 PIN, 0.1 SPACE	929834-01-13	APTRN	2100-02-0218	1
5	SKT, IC, 40PIN	DILB40P-108T	BURND	2100-03-0030	2
3	SOCKET, IC, 28 PIN	DILB28P-108T	BURND	2100-03-0081	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD
ASSEMBLY NO. 1100-00-1808
REV L
PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
TP1 TP2 TP3 TP4	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	4
Y2	CRYSTAL 32.768KHZ	KF38G	KYCRA	2300-99-0020	1
Y1	CRYSTAL 4.915MHZ	C1700	MIDRO	2300-99-0021	1
F1	FUSE, 1A, 250V	312001	LITFU	2400-05-0007	1
2	FUSE HOLDER, PCB MOUNT	345101	LITFU	2400-05-0043	1
4	BATTERY HOLDER	BH 2/3A	MPD	3000-00-0137	1
LS1	PIEZO	PKM24-4A0	MURAT	3000-00-0141	1
BT1	BATTERY, 3V LITHIUM	BR-2/3A	PANAS	4000-02-0008	1
R29 R30 R31 R39 R40 R41 R42 R43 R44 R45 R46 R47	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 10K OHM	MCR18EZH103JW5%	ROHM	4703-20-1035	12
R27	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 150K OHM	MCR18EZH154JW5%	ROHM	4703-20-1545	1
R73 R74	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 160 OHM	MCR18EZH161JW5%	ROHM	4703-20-1615	2
R62	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 22K OHM	MCR18EZH223JW5%	ROHM	4703-20-2235	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD
ASSEMBLY NO. 1100-00-1808
REV L
PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R11 R24 R25 R26 R3 R5 R58 R65	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 220K OHM	9C12063A2203JLR	MEPCO	4703-20-2245	8
R1 R12 R2 R20 R4 R50 R53 R54 R55 R56 R6 R61 R69 R7 R70	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 470K OHM	MCR18EZH474JW5%	ROHM	4703-20-4745	15
R10 R8 R9	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 6.2K OHM	MCR18EZH622JW5%	ROHM	4703-20-6225	3
R32 R33 R34 R35 R36 R37 R38	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 6.8K OHM	MCR18EZH682JW5%	ROHM	4703-20-6825	7
R48 R51 R52 R57 R60 R66	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 1M OHM	MCR18FXTA1004F	ROHM	4703-21-0041	6
R59	RES, SMD 1/8 LONG, 100PPM, 1%, 140K OHM	CRCW1206-1403FB	DALE	4703-21-4031	1
R64	SMD, RESISTOR, 1/8 LONG, 100PPM, 1% 14.3K OHM	9C12063A1432FKR	MEPCO	4703-21-4321	1
R49	RES, SMD, 1/8 LONG, 100PPM, 1%, 332K OHM	CRCW1206-3323FB	DALE	4703-23-3231	1
R63	SMD, RESISTOR, 1/8	9C12063A5112FKR	MEPCO	4703-25-1121	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD
ASSEMBLY NO. 1100-00-1808
REV L
PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	LONG, 100PPM, 1%, 51.1K OHM				
R28	RES, CC, 1/8W 5% 5.6M	BB5655	AB	4704-05-5604	1
CR16	ZENER DIODE, LEAD LESS, 27V, 10%, 1W	MLL4750	MOT	4801-02-0002	1
CR20	RECTIFIER, GEN PURP, 400V, 1A	IN4004	MOT	4806-01-4004	1
CR11	DIODE, RECTIFIER, DUAL IN-LINE	VSB54	VARO	4806-02-0054	1
CR12 CR13	DIODE, STTKY	SB130	GI	4806-02-0130	2
CR19	DIODE, 3A, 200V, FR	MR852	MOT	4806-02-0852	1
CR1 CR10 CR14 CR15 CR17 CR18 CR2 CR21 CR22 CR3 CR4 CR8 CR9	SMD, DIODE, LEADLESS EQUIVALENT IN4148, 500MW	RLS4148	ROHM	4807-01-4148	13
CR5 CR6 CR7	DIODE	5082-2811	HP	4809-02-2811	3
DS7	LED	TIL-220	TI	4899-00-0006	1
Q1	TRANS	2N3904	FAIR	4901-03-9040	1
Q2	TRANSISTOR, POWER FET, P-CHAN ENHANCMNT MODE	RFP6P08	RCA	4902-00-6081	1
Q3	TRANSISTOR	IRFD9123	IR	4902-09-1230	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD
ASSEMBLY NO. 1100-00-1808
REV L
PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
S1	SWITCH, DIP PIANO LEVER	76PSB08	GRAHL	5199-00-0005	1
U12	IC, REG, COMP	LT1020	LINTE	7000-10-2000	1
U16	IC, REGULATOR SWITCHING, VARIABLE	RC4193NB	RAYTH	7000-41-9300	1
U4 U7	SMD, 8X8192 RAM, CMOS	SRM2064M15	S-MOS	8000-20-6400	2
U15	FLIP-FLOP, DUAL D, CMOS, SMD	HEF4013BTD	SIG	8000-40-1341	1
U9	MUX/DEMUX 8-CHANNEL ANALOG CMOS SMD	HEF4051BTD	SIG	8000-40-5141	1
U13	GATE, NAND, S/TRIG, QUAD 2-INP, CMOS, SMD	HEF4093BTD	SIG	8000-40-9341	1
U1	IC	HD63B03RP	HTACH	8000-63-0301	1
U14 U22	GATE, NOR QUAD 2 INPUT POS HCMOS SMD	74HC02D	SIG	8000-74-0241	2
U19 U28 U29	HEX INVERTER	74HC04D	SIG	8000-74-0442	3
U20	SMD, QUAD 2-INPUT OR GATE, HCMOS	74HC32D	SIG	8000-74-3241	1
U23 U24	SMD, 1 OF 8 DECODER/DEMUX, HCMOS	74HC138D	SIG	8007-41-3841	2

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD
ASSEMBLY NO. 1100-00-1808
REV L
PAGE 6

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

DRAWN | DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PARTS LIST
MOTHER BOARD

SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-1808
REV L
SCALE
MODEL 52
SHEET 1 OF 2

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U18	SMD, IC, DUAL 2-TO-4 DECODER DEMUX	74HC139D	SIG	8007-41-3941	1
U10 U26	SMD, OCTAL BUFFER/LN DRIVER, TRISTATE, HCMOS	74HC241D	SIG	8007-42-4140	2
U11	BUF/LN DRIVER, OCTAL, TRISTATE, HCMOS, SMD	N74HC244D	SIG	8007-42-4441	1
U25	SMD, OCTAL BUSS TRANCEIVER, TRISTATE HCMOS	74HC245D	SIG	8007-42-4541	1
U2	SMD, OCTAL, D-TRANSPARENT LATCH, TRISTATE, HCMOS	74HC373D	SIG	8007-43-7341	1
U3	IC, SO	HD146818FP	HTACH	8014-68-1800	1
U6	SMD, RECEIVER/TRANSMITTER, RS-232 +5V, 16 PIN	MAX232EWE	MAXIM	8100-00-0012	1
U5	EPROM-PROGRAMMED USES 1 EA. 8002-75-1201	8600-00-0441	WVTK	8600-00-0441	1
U27	LSI, CUSTOM GATE ARRAY, CMOS, 4 CHAN UNIV	8700-51-5201	WVTK	8700-51-5201	1

WAVETEK
PARTS LIST

TITLE
PCA, MOTHER BOARD

ASSEMBLY NO.
1100-00-1808

REV
L

PAGE 7

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN | DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

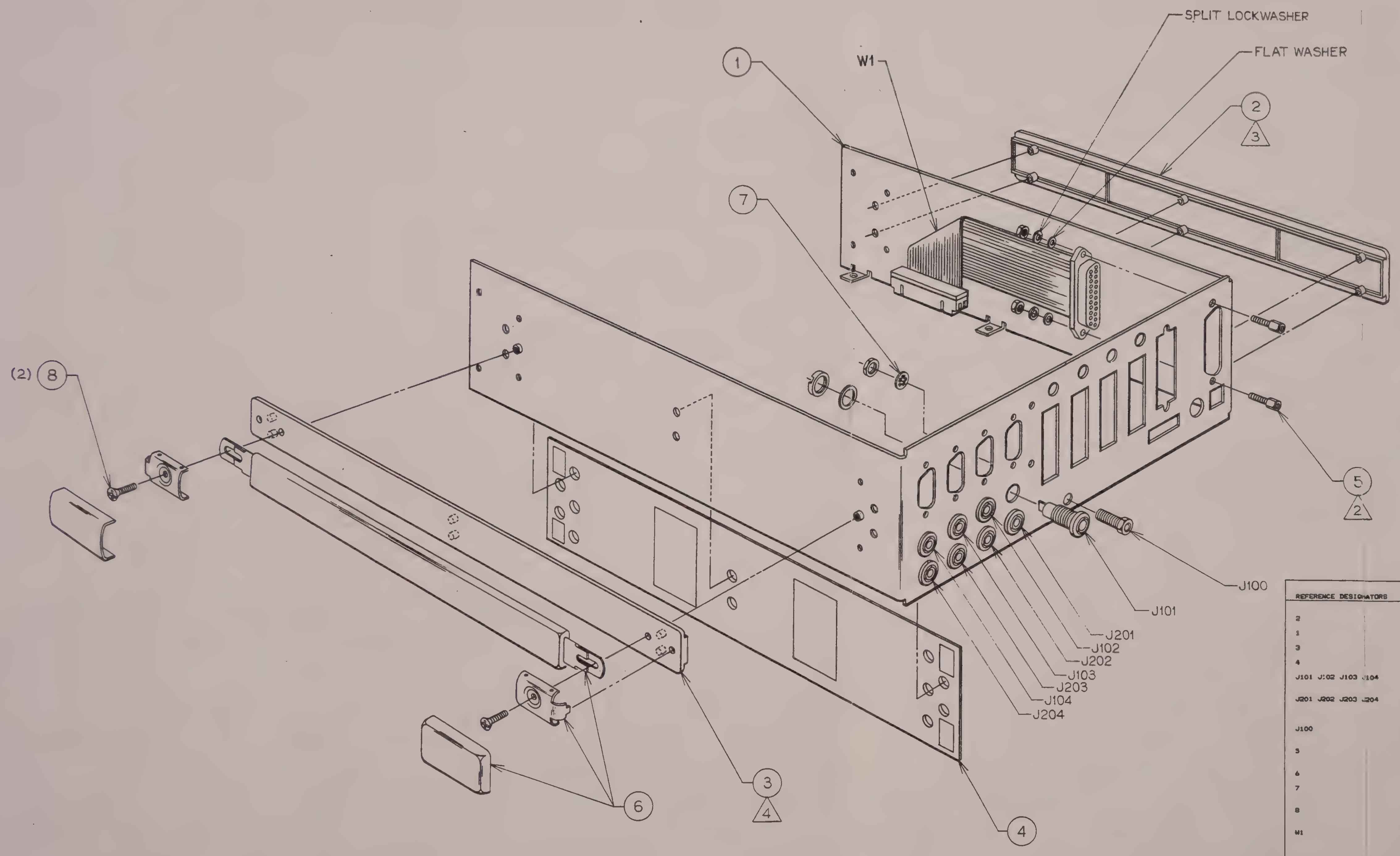
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PARTS LIST
MOTHER BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1100-00-1808	L

SCALE | MODEL 52 | SHEET 2 OF 2

REV	ECN	BY	DATE	APP
A	FOR RELEASE	JT	3/11/86	Jm



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
2	SIDE TRIM	1400-02-1180	WVTK	1400-02-1180	1
1	PANEL, REAR	1400-02-1273	WVTK	1400-02-1273	1
3	SIDE TRIM	31-32-1330	WVTK	1400-02-1330	1
4	INSULATOR, REAR PANEL	1400-02-1620	WVTK	1400-02-1620	1
J101 J102 J103 J104	SOCKET SAFETY LAB. RED FLAT CONNECTION	23.3000-1	INLOK	2100-03-0082	4
J201 J202 J203 J204	SOCKET, SAFETY LAB. BLACK FLAT CONNECTION	23.3000-4	INLOK	2100-03-0083	4
J100	JACK, BANANA, 1/4 DIA MOUNT HOLE	109	SMITH	2100-03-0085	1
5	JACK SOCKET 2 PCS PER BAG	207719-1	AMP	2100-07-0021	1
6	HANDLE, RETRACTABLE	2800-07-0035	WAVTK	2800-07-0035	1
7	LOCKWASHER, 1/4, INT TOOTH, SS	MS35333-74	MIL	2800-24-0009	1
8	MACHINE SCREW, 100 DEG FLAT HEADS, SS	NPS24693-C28	NYLOK	2800-61-6108	2
W1	ASSY, RIBBON CABLE	6002-00-0029	WVTK	6002-00-0029	1

WAVETEK PARTS LIST	TITLE ASSY, REAR PANEL .	ASSEMBLY NO. 1206-00-2618 PAGE 1	REV A

SEE SEPARATE PARTS LIST 1206-00-2618

4. HEAT STAKE SIDE TRIM TO REAR PANEL USING ONLY CENTER TWO BOSSES.

3. HEAT STAKE SIDE TRIM TO REAR PANEL USING ALL SIX BOSSES.

2. INSTALL RS-232-C CABLE/ALIGNMENT FIXTURE TO J105 WHILE TIGHTENING HARDWARE TO ENSURE CORRECT SPACING.

1. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.

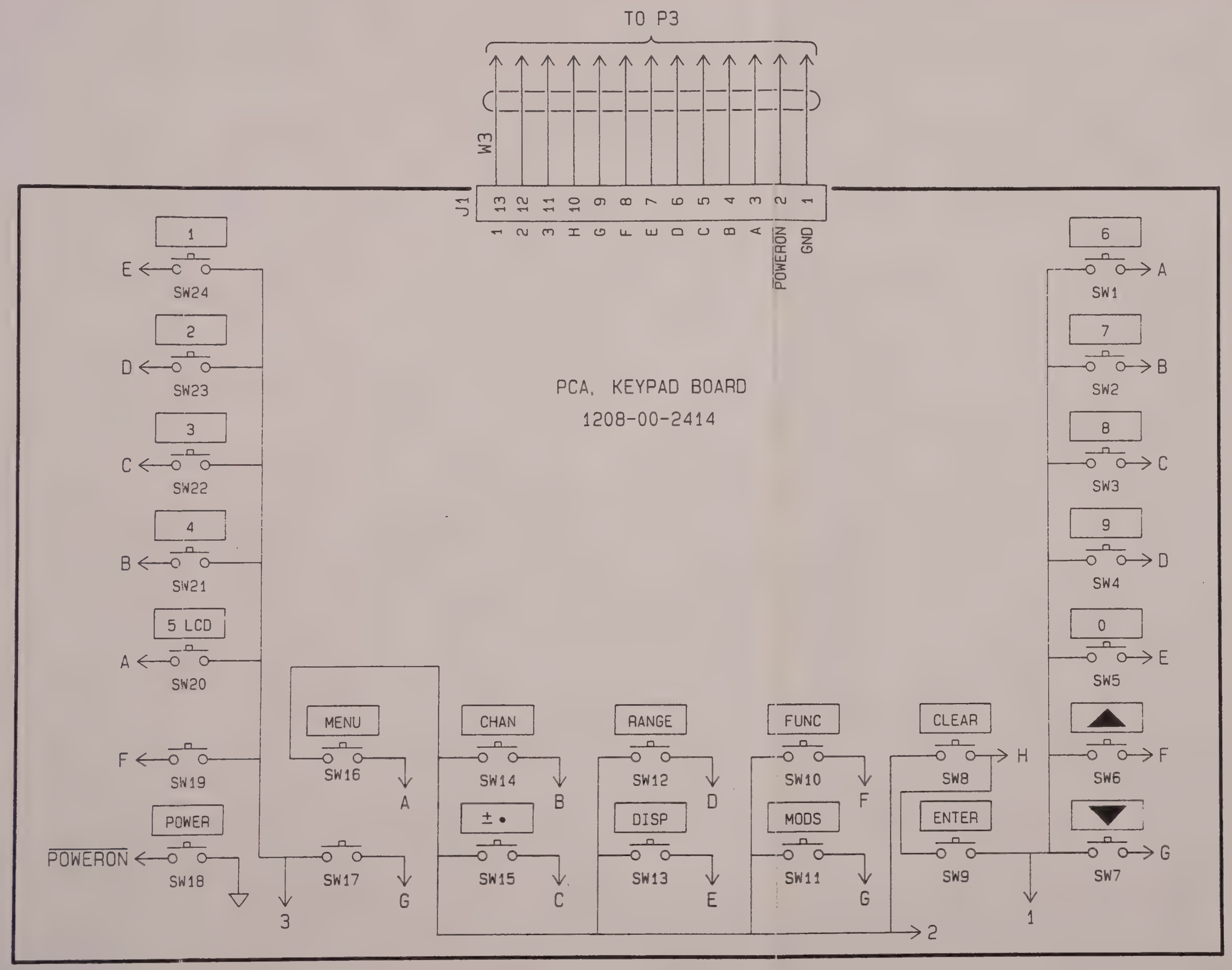
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3/11/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —+—	PROJ ENGR N. S. Miller	3/12/86	TITLE ASSEMBLY, REAR PANEL
	RELEASE APPROV DR Taylor 3/12/86		
FINISH WAVETEK PROCESS —+—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO 51/52
	SCALE NONE		DWG NO 1206-00-2618
			REV A
			CODE IDENT 23338
			SHEET 1 OF 1

1206-00-2618 A

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A2785

REV	ECN	BY	DATE	APP
A	FOR RELEASE		2/25/86	


TO P3
W3
J1
13 12 11 10 9 8 7 6 5 4 3 2 1
1 2 3 H G F E D C B A POWERON GND
PCA, KEYPAD BOARD
1208-00-2414
1
E
SW24
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D
SW23
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SW19
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SW5
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SW6
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SW7
G

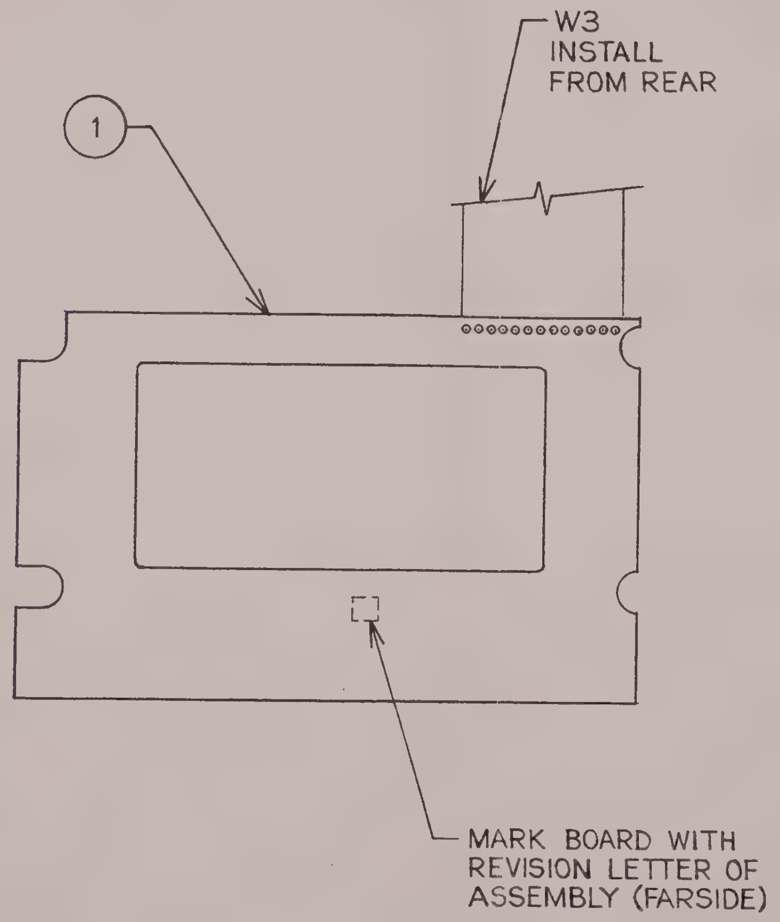
1. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

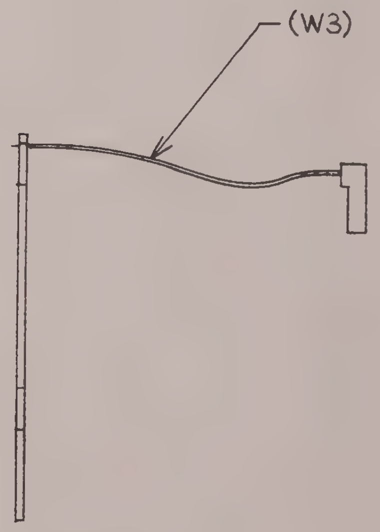
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 2/14/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	2-25-86	TITLE SCHEMATIC, KEYPAD BOARD
	RELEASE APPROV	2-26-86	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 52
	SCALE NONE		DWG NO. 0103-00-2414
			REV A
			CODE IDENT 23338
			SHEET 1 OF 1

0103-00-2414 A

REV	ECN	BY	DATE	APP
A	FOR RELEASE	A.T.	2/...	[illegible]





REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, KEYPAD BOARD	0103-00-2414	WVTK	0103-00-2414	1
1	DRILL DRWG, KEYPAD BD	1700-00-2414	WVTK	1700-00-2414	1
W3	RIBBON CABLE ASSEMBLY, 13 PIN, 4"	6002-00-0042	WVTK	6002-00-0042	1

WAVETEK PARTS LIST	TITLE PCA, KEYBOARD-52	ASSEMBLY NO. 1208-00-2414 PAGE 1	REV A

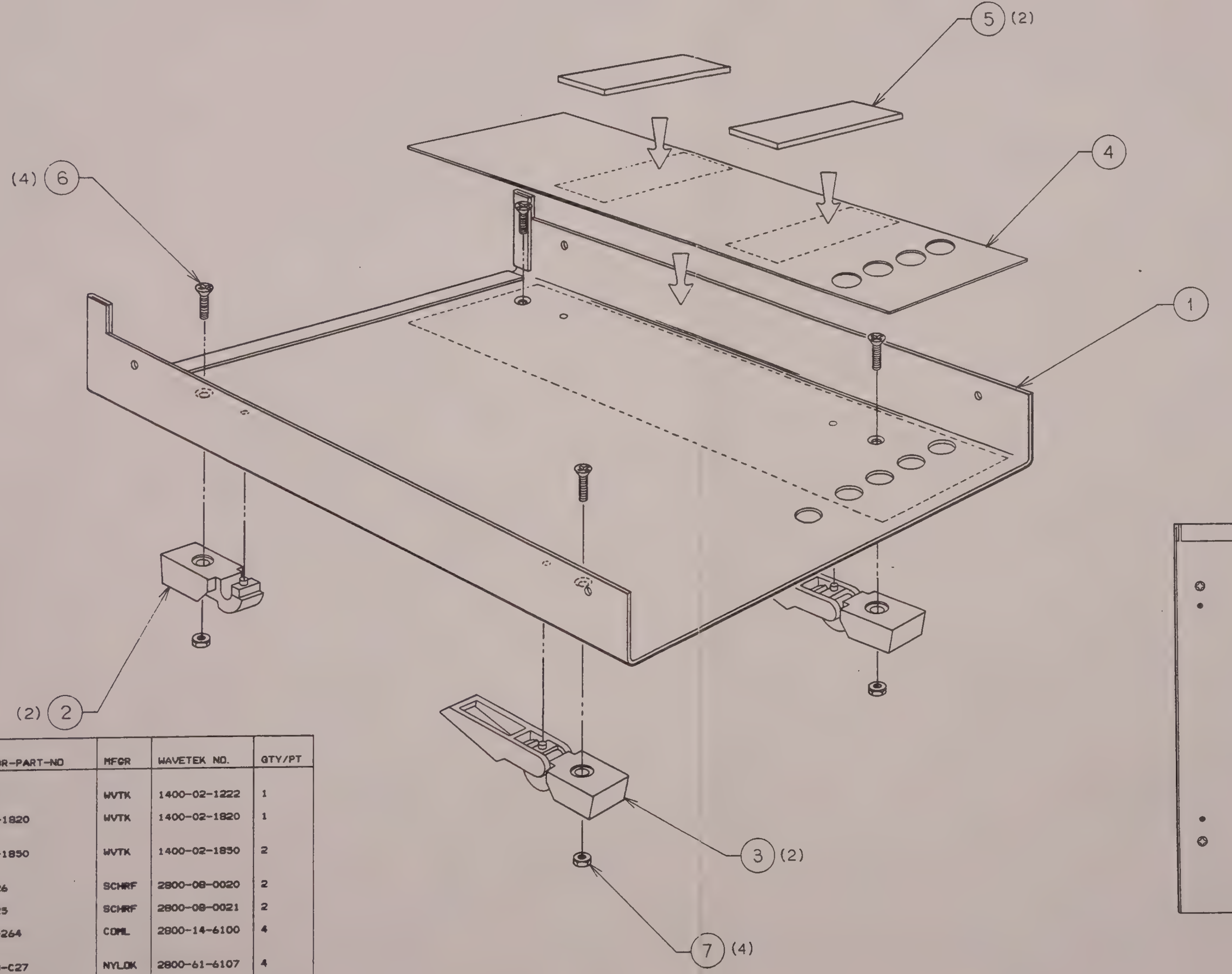
SEE SEPARATE PARTS LIST 1208-00-2414

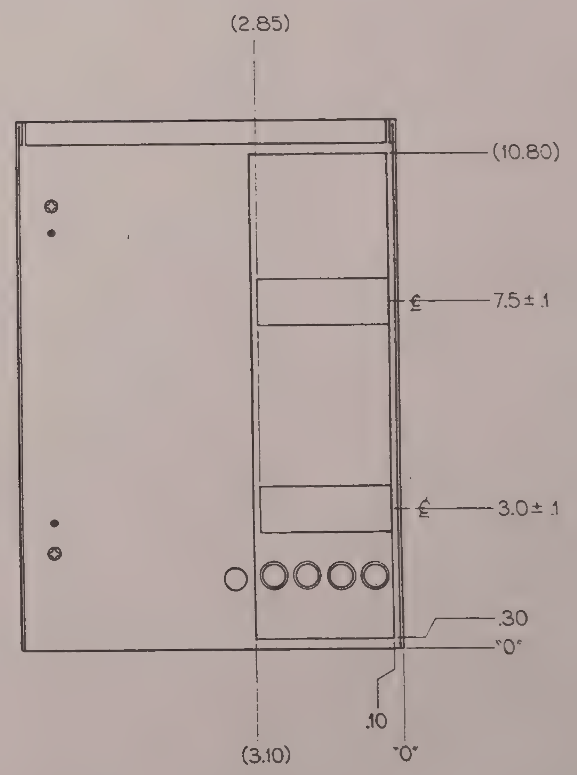
2. SEE 0103-00-2414 FOR SCHEMATIC.
1. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 8/15/85	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL -//-	PROJ ENGR C. [illegible]	2-25-86	TITLE PCA, KEYPAD BOARD
	RELEASE APPROV DK Taylor 2/26/86		
FINISH WAVETEK PROCESS -//-	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		MODEL NO. 52
	DO NOT SCALE DWG		DWG NO. 1208-00-2414
	SCALE FULL		REV A
			CODE IDENT 23338
			SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE	I	3/11/86	T.M
B	7379		4/20/86	





REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	COVER, BOTTOM	52-1222	WVTK	1400-02-1222	1
4	INSULATOR, BOTTOM COVER	1400-02-1820	WVTK	1400-02-1820	1
5	SUPPORT, CHANNEL BD. (2.75")	1400-02-1850	WVTK	1400-02-1850	2
2	FOOT	10603-026	SCHRF	2800-08-0020	2
3	FOOT WITH TIP-UP	10603-025	SCHRF	2800-08-0021	2
7	NUT, HEX, CAD PLATE 6-32	MS35649-264	COML	2800-14-6100	4
6	MACHINE SCREW, 100 DEG FLAT HEAD, SS	NPS24693-C27	NYLOK	2800-61-6107	4

WAVETEK PARTS LIST	TITLE ASSY, BOTTOM COVER	ASSEMBLY NO. 1206-00-2620 PAGE 1	REV B

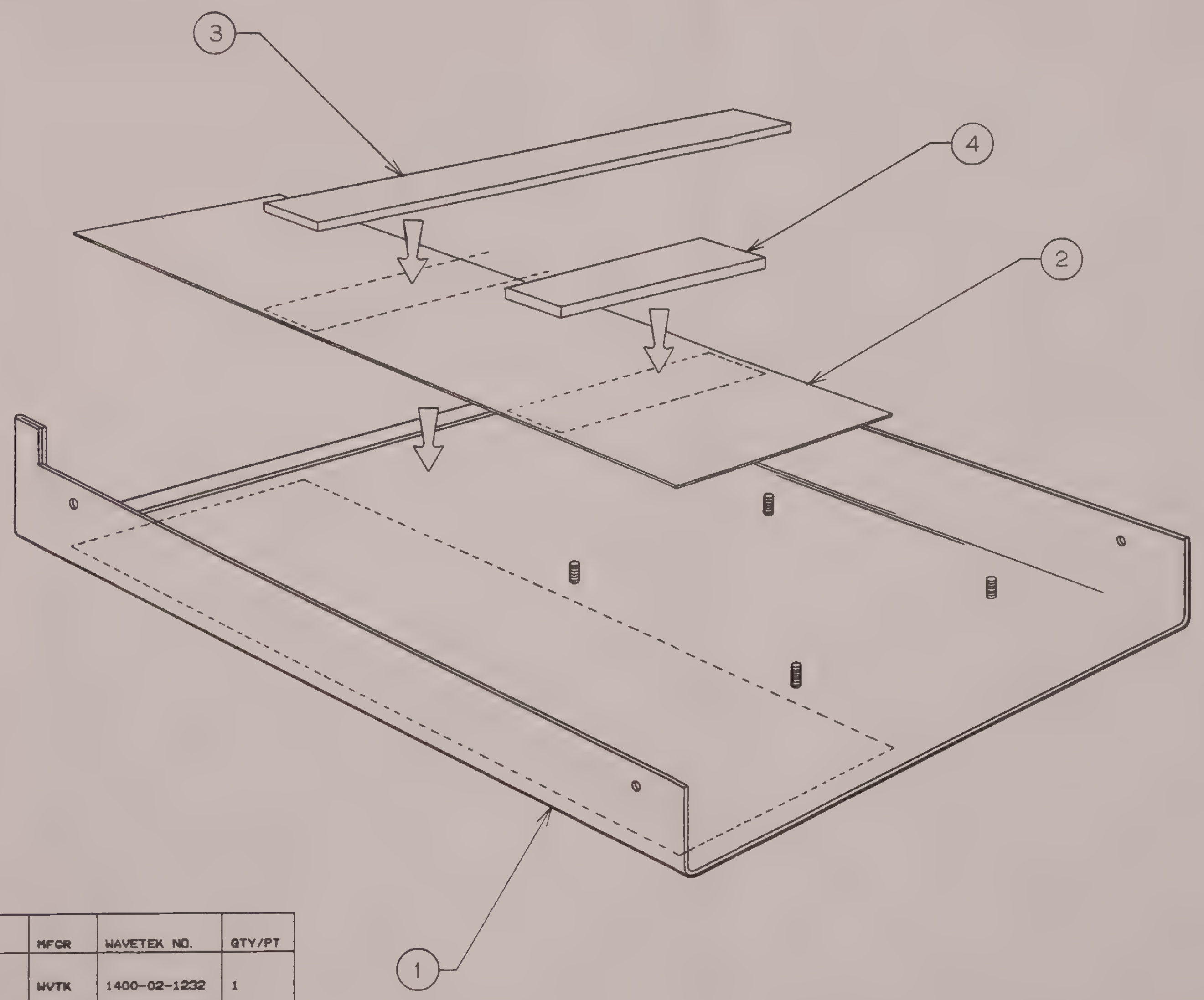
NOTE: UNLESS OTHERWISE SPECIFIED

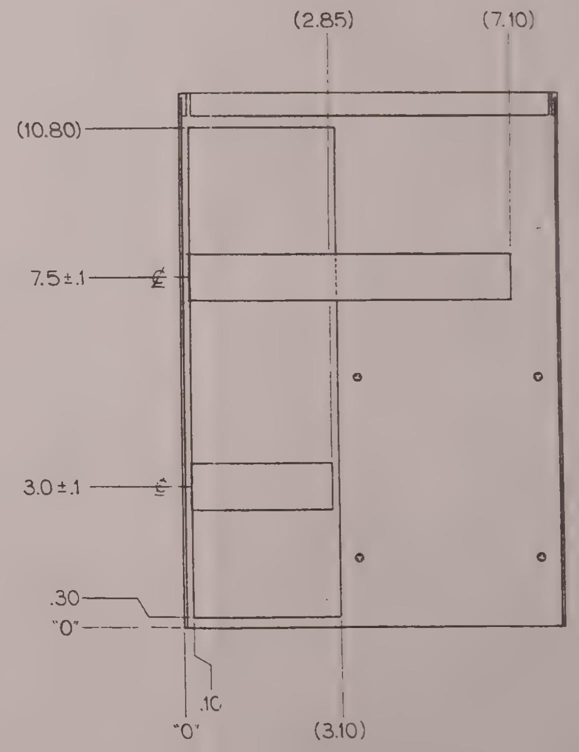
SEE SEPARATE PARTS LIST 1206-00-2620

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3/9/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL — // —	PROJ ENGR N. S. Miller	3/12/86	TITLE ASSEMBLY, BOTTOM COVER
	RELEASE APPROV D. Taylor 3/12/86		
FINISH WAVETEK PROCESS — // —	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO 51/52
	SCALE NONE		DWG NO. 1206-00-2620
			REV B
			CODE IDENT 23338
			SHEET 1 OF 1

1206-00-2620 B

REV	ECN	BY	DATE	APP
A	FOR RELEASE	DT	3/10/86	nm





REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	COVER, TOP	52-1232	WVTK	1400-02-1232	1
2	INSULATOR, TOP COVER	1400-02-1830	WVTK	1400-02-1830	1
3	SUPPORT, CHANNEL BD. (7.00")	1400-02-1840	WVTK	1400-02-1840	1
4	SUPPORT, CHANNEL BD. (2.75")	1400-02-1850	WVTK	1400-02-1850	1

WAVETEK PARTS LIST	TITLE ASSY, TOP COVER	ASSEMBLY NO. 1206-00-2621 PAGE 1	REV A

NOTE UNLESS OTHERWISE SPECIFIED

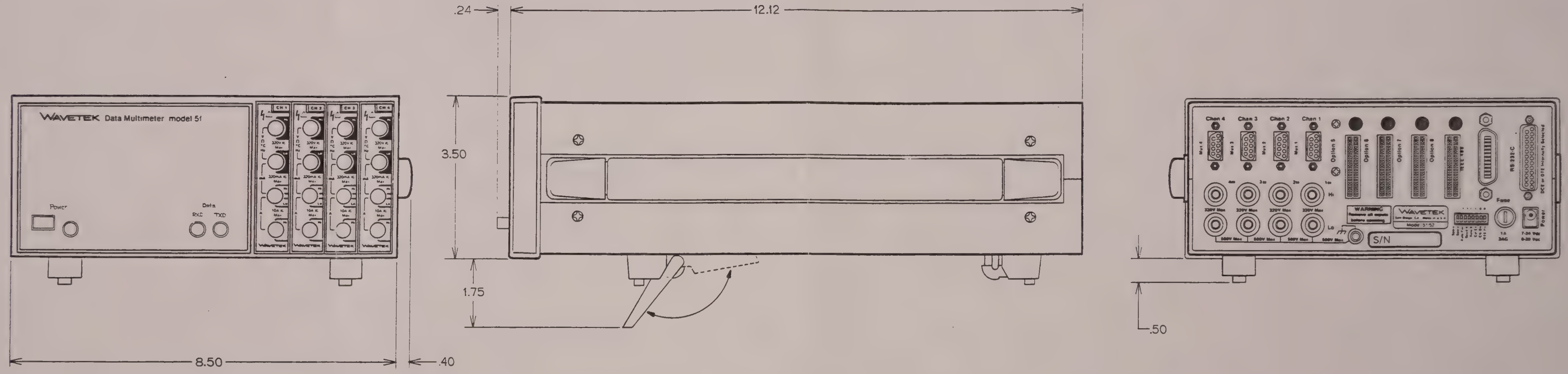
SEE SEPARATE PARTS LIST 1206-00-2621

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D COOPER	DATE 3/10/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —/—	PROJ ENGR N. E. Miller	3/12/86	TITLE ASSEMBLY, TOP COVER
	RELEASE APPROV R Taylor 3/12/86		
FINISH WAVETEK PROCESS —/—	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 51/52
	SCALE NONE		DWG NO. 1206-00-2621
			REV A
			CODE IDENT 23338
			SHEET 1 OF 1

1206-00-2621 A

BISHOP GRAPHICS/ACCUPRESS
REORDER NO [illegible]

REV	ECN	BY	DATE	APP
A	FOR RELEASE	AT	9/29 86	NM


.24
12.12
3.50
1.75
8.50
.40
.50
WAVETEK Data Multimeter model 51
Power
Data
RXD
TXD
CH 1
CH 2
CH 3
CH 4
Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
IEEE 488
RS 232-C
DCE or DTE Internally Selected
Hi
Lo
WARNING
WAVETEK
S/N
Fuse
1A
3AG
Power
7-36 Vdc

1. UNIT WEIGHT: 3.40 KG. (7.5 LBS.) NET,
(WITH BATTERY OPTION ADD 1.25 KG. (2.75 LBS.);
SHIPPING (WITHOUT BATTERY): 4.5 KG. (10.00 LBS.).

NOTE: UNLESS OTHERWISE SPECIFIED

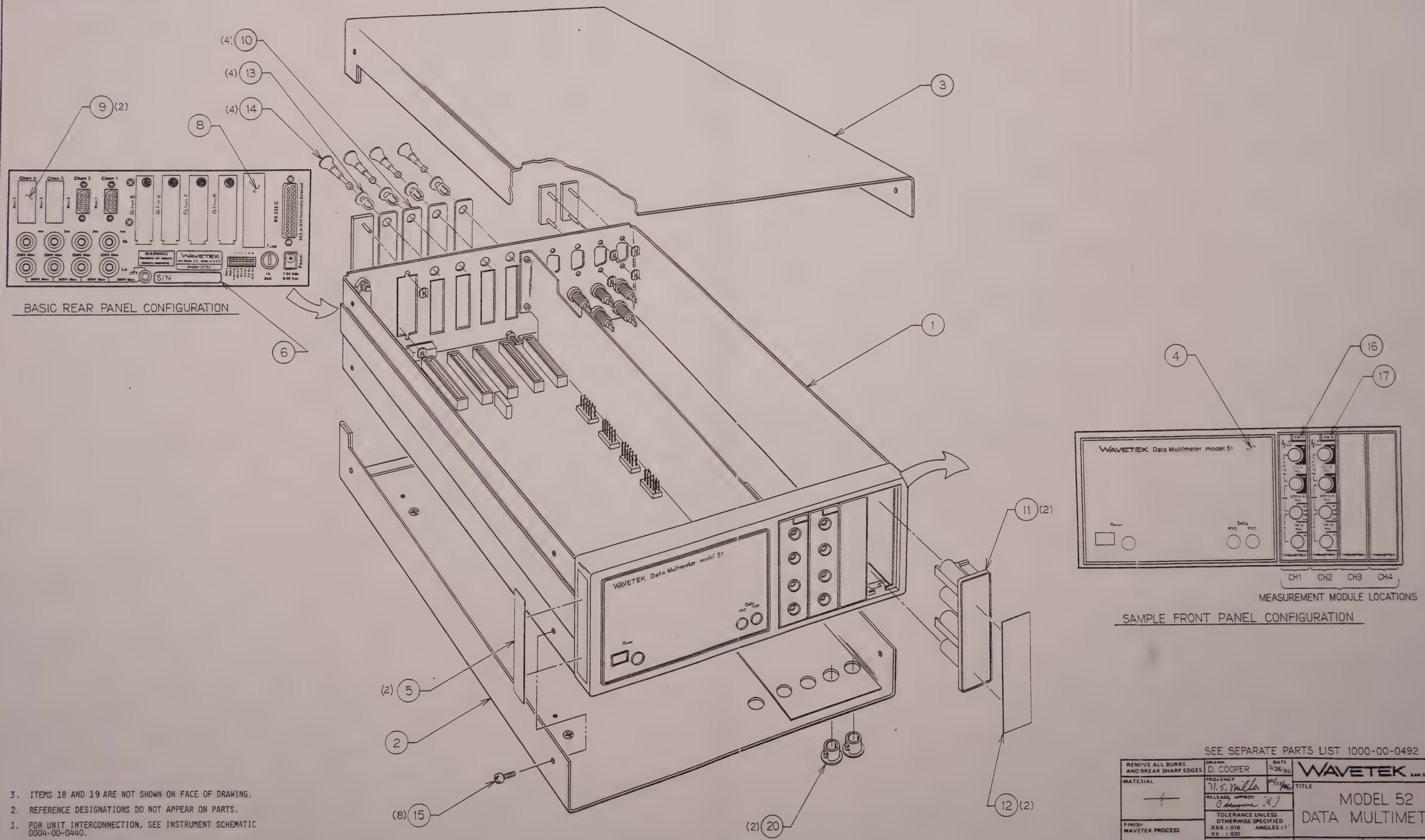
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
—//—
FINISH
WAVETEK PROCESS
—//—
DRAWN A.TALMADGE DATE 9/3/86
PROJ ENGR N. E. Miller 10/7/86
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.050
DO NOT SCALE DWG
SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
OUTLINE DRAWING,
MODEL 51
MODEL NO 51
DWG NO. 0002-00-0492
REV A
CODE IDENT 23338
SHEET 1 OF 1

0002-00-0492 A

REV	ECN	BY	DATE	APP
A	FOR RELEASE	ACT	[illegible]	[illegible]

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.


(4) 10
(4) 13
(4) 14
9 (2)
8
3
1
6
4
16
17
11 (2)
(2) 5
2
(8) 15
(2) 20
12 (2)
Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS 232 C
DCE or DTE Internally Selected
Hi
Lo
WARNING
WAVETEK
S/N
Fuse
Power
WAVETEK Data Multimeter model 51
Power
Data
RXD
TXD
CH1
CH2
CH3
CH4

BASIC REAR PANEL CONFIGURATION

MEASUREMENT MODULE LOCATIONS

SAMPLE FRONT PANEL CONFIGURATION

3. ITEMS 18 AND 19 ARE NOT SHOWN ON FACE OF DRAWING.
2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0492

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN D. COOPER
DATE 3/26/86
PROJ ENGR M. S. Miller 10/17/86
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
MODEL 52
DATA MULTIMETER
MODEL NO 51
DWG NO 1000-00-0492
REV A
CODE IDENT 23338
SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	OUTLINE DRAWING-51	0002-00-0492	WVTK	0002-00-0492	1
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
1	ASSY, CHASSIS-51	1101-00-2853	WVTK	1101-00-2853	1
2	ASSY, BOTTOM COVER	1206-00-2620	WVTK	1206-00-2620	1
3	ASSY, TOP COVER	1206-00-2621	WVTK	1206-00-2621	1
NONE	MODEL 52 INSTRUCTION MANUAL	1300-00-0440	WVTK	1300-00-0440	1 5
6	SERIAL TAG MODEL 602	602-6950	WVTK	1400-01-6950	1
11	FRONT PANEL, BLANK	52-0860	WVTK	1400-02-0860	2
16	LABEL CHANNEL 1	52-1110	WVTK	1400-02-1110	1
17	LABEL, CHANNEL 2	52-1120	WVTK	1400-02-1120	1
18	LABEL CHANNEL, 3	52-1130	WVTK	1400-02-1130	1
19	LABEL CHANNEL, 4	52-1140	WVTK	1400-02-1140	1
12	DECAL, BLANK CHANNEL	52-1150	WVTK	1400-02-1150	2
5	DECAL, SIDE TRIM	52-1200	WVTK	1400-02-1200	2
10	COVER, DIGITAL I/O	1400-02-1593	WVTK	1400-02-1593	4
4	DECAL, FRONT PANEL-51	1400-02-2140	WVTK	1400-02-2140	1

WAVETEK
PARTS LIST
TITLE
MODEL 51 DATA MULTIMETER
ASSEMBLY NO.
1000-00-0492
PAGE 1
REV
A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
15	MACHINE SCREW, PANHEAD, PHLPS, W/NYLOCK PATCH	6-32X3/16 PAN LOK BLK	CMRCL	2800-23-6103	8
20	PLUG BUTTON, NYLON, 17/32 HEAD, BLACK	2633	HEYCO	2800-35-0007	2
13	NYLATCH GROMMET, 1/4 HOLE ONE OF TWO PARTS	HN4G43-1	HART	2800-60-0004	4
14	NYLATCH PLUNGER, 1/4 HOLE, ONE OF TWO PARTS	HN4P43-4-1	HART	2800-60-0005	4
NONE	TEST LEAD SET, 48 INCH	3000-00-0156	WVTK	3000-00-0156	1
NONE	INSERT	101-18	WVTK	3300-00-0015	1
NONE	CARTON	101-18A	WVTK	3300-01-0012	1
8	COVER, CONNECTOR CUT-OUT	12-24R BLACK	PEPER	3300-03-0002	1
9	COVER, CONNECTOR CUT-OUT	10-9 BLACK	PEPER	3300-03-0003	2

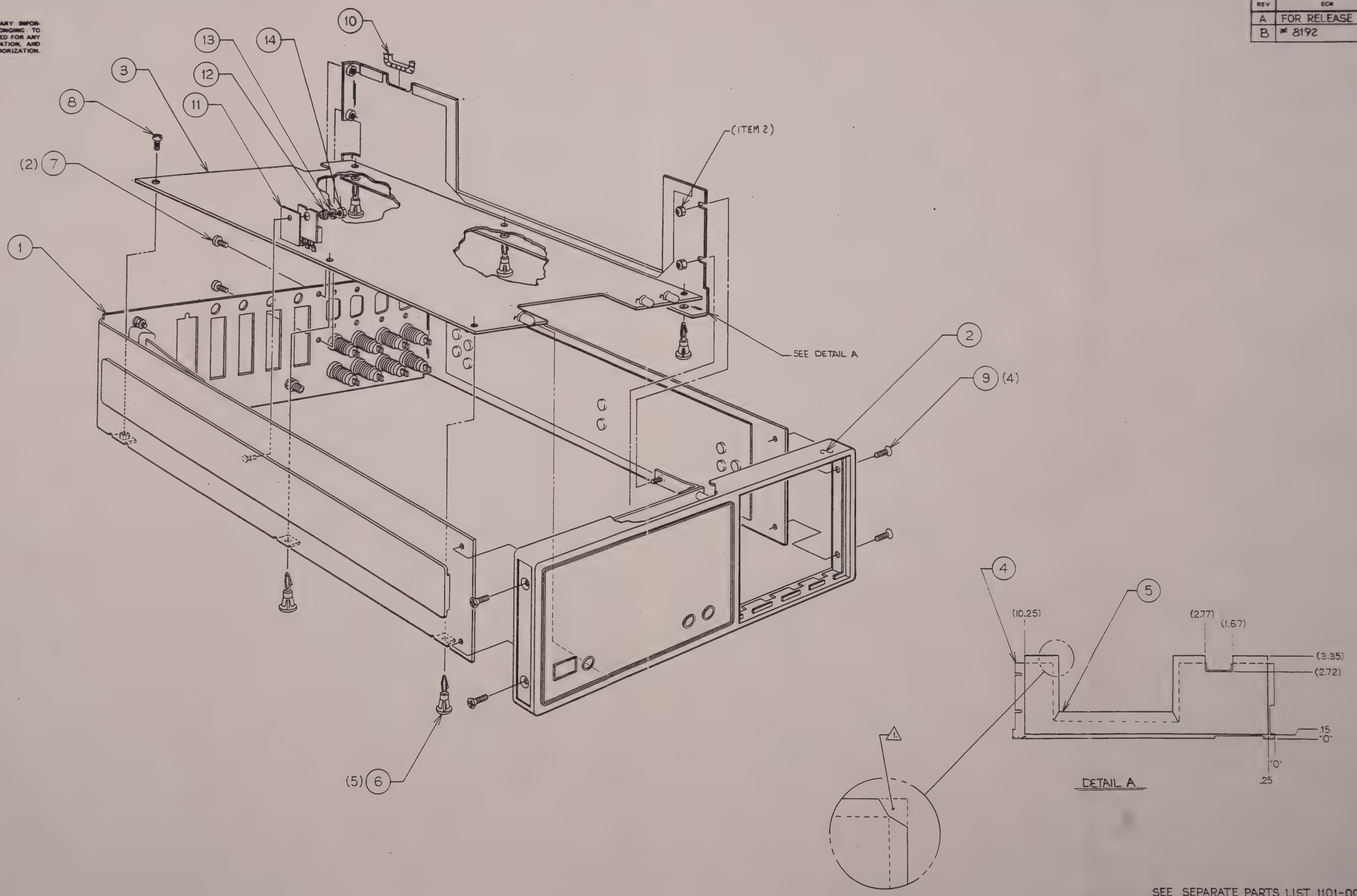
WAVETEK
PARTS LIST
TITLE
MODEL 51 DATA MULTIMETER
ASSEMBLY NO.
1000-00-0492
PAGE 2
REV
A

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
MODEL 51
DATA MULTIMETER
SIZE D
FSCM NO. 23338
DWG. NO. 1000-00-0492
REV A
SCALE
MODEL 51
SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE	AT	[illegible]	DM
B	# 8192	R.C. 4-22-87	4-24-87	A.R.T.


10
13
14
3
12
8
11
(2) 7
1
(ITEM 2)
SEE DETAIL A
2
9 (4)
4
5
(10.25)
(2.77)
(1.67)
(3.35)
(2.72)
.15
"0"
"0"
.25
1.
DETAIL A
(5) 6

SEE SEPARATE PARTS LIST 1101-00-2853

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL —

FINISH WAVETEK PROCESS —

DRAWN D. COOPER DATE 3/12/86

PROJ ENGR N. E. Miller 10/17/86

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE ASSEMBLY, CHASSIS

MODEL NO 51

DWG NO. 1101-00-2853

REV B

CODE IDENT 23338

SHEET 1 OF 1

1101-00-2853 B

1. SMOOTH INSULATOR (ITEM 5) OVER EDGES OF CENTER SHIELD (ITEM 4) AND FOLD IT DOWN ON TO REAR SIDE, FOLD CORNER OVER FIRST THEN FOLD ADJACENT SIDES OVER ON TOP OF CORNER, HOLDING IT DOWN.

NOTE. UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO [illegible]

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC PCA, MOTHER BOARD	0103-1808	WVTK	0103-00-1808	1
NONE	ASSY, GATE ARRAY PIGGYBACK	1208-00-2951	WVTK	1208-00-2951	1
C29	CAP, CER, MON, .47UF, 20%, 50V, 25U	CRC230Z5U474M050	CORNG	1500-04-7406	1
C15 C24 C36 C51 C52 C53 C54	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	7
C35	CAP, ELECT, 220MF/10V	ECEA1AU221	PANAS	1500-32-2001	1
C4 C5 C55 C6 C7	CAP, ELECT, 22MF/25V	SRA25VB22MC	UNCON	1500-32-2002	5
C21	CAP, ELECT, 2200MF, 25V RADIAL LEAD	ECEA1EV222S	PANAS	1500-32-2202	1
C22 C31	SMD, CAP, CER, 2%, 50V, 1000PF	C1206C102J2GAC	KEMET	1500-81-0201	2
C13 C14 C16 C19 C20 C23 C25 C26 C27 C28 C3 C32 C33 C37 C38 C39 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C8 C9	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	28
C12 C2	SMD, CAP, CER, 2%, 50V, 15PF	C1206C150J2GAC	KEMET	1500-81-5001	2
C1	SMD, CAP, CER, 2%, 50V, 20PF	C1206C200G5GAC	KEMET	1500-82-0001	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD-51
ASSEMBLY NO. 1100-00-2822
REV E
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C10 C11	SMD, CAP, CER, 2%, 50V, 33PF	C1206C330J2GAC	KEMET	1500-83-3001	2
C30	SMD, CAP, CER, 2%, 50V, 56PF	C1206C560J2GAC	KEMET	1500-85-6001	1
L1	CHOKE, TORROIDAL, 1MH	4294	CASYS	1800-00-0025	1
J6	CONNECTOR, HEADER (4 PIN)	102202-1	AMP	2100-02-0131	1
J1 J2	CONN, HEADER 26 PIN/2 ROW	929836-01-13	A/P	2100-02-0156	2
J10 J11 J7 J8 J9	CONNECTOR, EDGE 36 PIN	ETC18DRXN	SULL	2100-02-0191	5
J5	CONNECTOR POWER JACK	16PJ032	MOUSR	2100-02-0192	1
J12 J13 J14 J15	CONNECTOR, HEADER, DOUBLE 5 PIN ROWS, 0.1X0.1	929836-01-05	APTRN	2100-02-0212	4
P6	JUMPER, FEMALE, 2 POSITION, 0.1 SPACE	929950-00	APTRN	2100-02-0213	1
5	SKT, IC, 40PIN	DILB40P-108T	BURND	2100-03-0030	2
3	SOCKET, IC, 28 PIN	DILB28P-108T	BURND	2100-03-0081	1
TP1 TP2 TP3 TP4	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	4
Y2	CRYSTAL 32.768KHZ	KF38G	KYCRA	2300-99-0020	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD-51
ASSEMBLY NO. 1100-00-2822
REV E
PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Y1	CRYSTAL 4.915MHZ	C1700	MIDRD	2300-99-0021	1
F1	FUSE, 1A, 250V	312001	LITFU	2400-05-0007	1
2	FUSE HOLDER, PCB MOUNT	345101	LITFU	2400-05-0043	1
6	MOUNTING SPACER .10 L(.085 OD X .028 ID)	901-100	BIVAR	2800-11-0025	6
4	BATTERY HOLDER	BH 2/3A	MPD	3000-00-0137	1
LS1	PIEZO	PKM24-4A0	MURAT	3000-00-0141	1
BT1	BATTERY, 3V LITHIUM	BR-2/3A	PANAS	4000-02-0008	1
R29 R30 R31	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 10K OHM	MCR18EZH103JW5%	ROHM	4703-20-1035	3
R27	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 150K OHM	MCR18EZH154JW5%	ROHM	4703-20-1545	1
R73 R74	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 160 OHM	MCR18EZH161JW5%	ROHM	4703-20-1615	2
R24 R25 R26	RES, SMD GP 1/8 LONG 200PPM 5% 1.8K OHM	MCR18EZH182JW5%	ROHM	4703-20-1825	3
R62	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 22K	MCR18EZH223JW5%	ROHM	4703-20-2235	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD-51
ASSEMBLY NO. 1100-00-2822
REV E
PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	OHM				
R11 R3 R5 R58 R65	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 220K OHM	9C12063A2203JLR	MEPCO	4703-20-2245	5
R1 R12 R2 R20 R4 R50 R53 R54 R55 R56 R6 R61 R69 R7 R70	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 470K OHM	MCR18EZH474JW5%	ROHM	4703-20-4745	15
R10 R8 R9	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 6.2K OHM	MCR18EZH622JW5%	ROHM	4703-20-6225	3
R48 R51 R52 R57 R60 R66	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 1M OHM	MCR18FXTA1004F	ROHM	4703-21-0041	6
R59	RES, SMD 1/8 LONG, 100PPM, 1%, 140K OHM	CRCW1206-1403FB	DALE	4703-21-4031	1
R64	SMD, RESISTOR, 1/8 LONG, 100PPM, 1% 14.3K OHM	9C12063A1432FKR	MEPCO	4703-21-4321	1
R49	RES, SMD, 1/8 LONG, 100PPM, 1%, 332K OHM	CRCW1206-3323FB	DALE	4703-23-3231	1
R63	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 51.1K OHM	9C12063A5112FKR	MEPCO	4703-25-1121	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD-51
ASSEMBLY NO. 1100-00-2822
REV E
PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R28	RES, CC, 1/8W 5% 5.6M	BB5655	AB	4704-05-5604	1
CR16	ZENER DIODE, LEAD LESS, 27V, 10%, 1W	MLL4750	MOT	4801-02-0002	1
CR20	RECTIFIER, GEN PURP, 400V, 1A	IN4004	MOT	4806-01-4004	1
CR11	DIODE, RECTIFIER, DUAL IN-LINE	VSB54	VARO	4806-02-0054	1
CR12 CR13	DIODE, STTKY	SB130	GI	4806-02-0130	2
CR19	DIODE, 3A, 200V, FR	MR852	MOT	4806-02-0852	1
CR1 CR14 CR15 CR17 CR18 CR2 CR21 CR3 CR4	SMD, DIODE, LEADLESS EQUIVALENT IN4148, 500MW	RLS4148	ROHM	4807-01-4148	9
CR5 CR6 CR7	DIODE	5082-2811	HP	4809-02-2811	3
DS7	LED	TIL-220	TI	4899-00-0006	1
DS1 DS2	LED, AMBER, 2MA	HLMP-4719	HP	4899-00-0039	2
DS3	LED, LOW CURRENT, GRN, T-1 3/4	HLMP-4740	HP	4899-00-0052	1
Q1	TRANS	2N3904	FAIR	4901-03-9040	1
Q2	TRANSISTOR, POWER FET, P-CHAN ENHANCMNT	RFP6P08	RCA	4902-00-6081	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD-51
ASSEMBLY NO. 1100-00-2822
REV E
PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	MODE				
Q3	TRANSISTOR	IRFD9123	IR	4902-09-1230	1
S2	SWITCH, 2PDT, MOM.	5102-00-0010	WVTK	5102-00-0010	1
7	BUTTON, BONE GRAY	B-305	CRL	5103-04-0009	1
S1	SWITCH, DIP PIANO LEVER	76PSB08	GRAHL	5199-00-0005	1
U12	IC, REG, COMP	LT1020	LINTE	7000-10-2000	1
U16	IC, REGULATOR SWITCHING, VARIABLE	RC4193NB	RAYTH	7000-41-9300	1
U4 U7	SMD, 8X8192 RAM, CMOS	SRM2064M15	S-MOS	8000-20-6400	2
U15	FLIP-FLOP, DUAL D, CMOS, SMD	HEF4013BTD	SIG	8000-40-1341	1
U13	GATE, NAND, S/TRIG, QUAD 2-INP, CMOS, SMD	HEF4093BTD	SIG	8000-40-9341	1
U1	IC	HD63B03RP	HTACH	8000-63-0301	1
U14 U22	GATE, NOR QUAD 2 INPUT POS HCMOS SMD	74HC02D	SIG	8000-74-0241	2
U19 U28 U29	HEX INVERTER	74HC04D	SIG	8000-74-0442	3
U20	SMD, QUAD 2-INPUT OR GATE, HCMOS	74HC32D	SIG	8000-74-3241	1

WAVETEK PARTS LIST
TITLE PCA, MOTHER BOARD-51
ASSEMBLY NO. 1100-00-2822
REV E
PAGE 6

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN | DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE PARTS LIST
MOTHER BOARD-51
SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-2822
REV E
SCALE
MODEL 51
SHEET 1 OF 2

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U23 U24	SMD, 1 OF 8 DECODER/DEMUX, HCMOS	74HC138D	SIG	8007-41-3841	2
U18	SMD, IC, DUAL 2-TO-4 DECODER DEMUX	74HC139D	SIG	8007-41-3941	1
U10 U26	SMD, OCTAL BUFFER/LN DRIVER, TRISTATE, HCMOS	74HC241D	SIG	8007-42-4140	2
U25	SMD, OCTAL BUSS TRANCEIVER, TRISTATE HCMOS	74HC245D	SIG	8007-42-4541	1
U2	SMD, OCTAL, D-TRANSPARENT LATCH; TRISTATE, HCMOS	74HC373D	SIG	8007-43-7341	1
U3	IC, SJ	HD146818FP	HTACH	8014-68-1800	1
U6	SMD, RECEIVER/TRANSMITTER, RS-232 +5V, 16 PIN	MAX232EWE	MAXIM	8100-00-0012	1
U5	IC PROGRAMMED REF: 8002-75-1201	8600-00-0375	WVTK	8600-00-0375	1
U27	LSI, CUSTOM GATE ARRAY, CMOS, 4 CHAN UNIV	8700-51-5201	WVTK	8700-51-5201	1

WAVETEK PARTS LIST	TITLE PCA, MOTHER BOARD-51	ASSEMBLY NO. 1100-00-2822 PAGE 7	REV E

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN | DATE

CHECKED

PROJ. ENGR.

RELEASE APPROV.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PARTS LIST
MOTHER BOARD-51

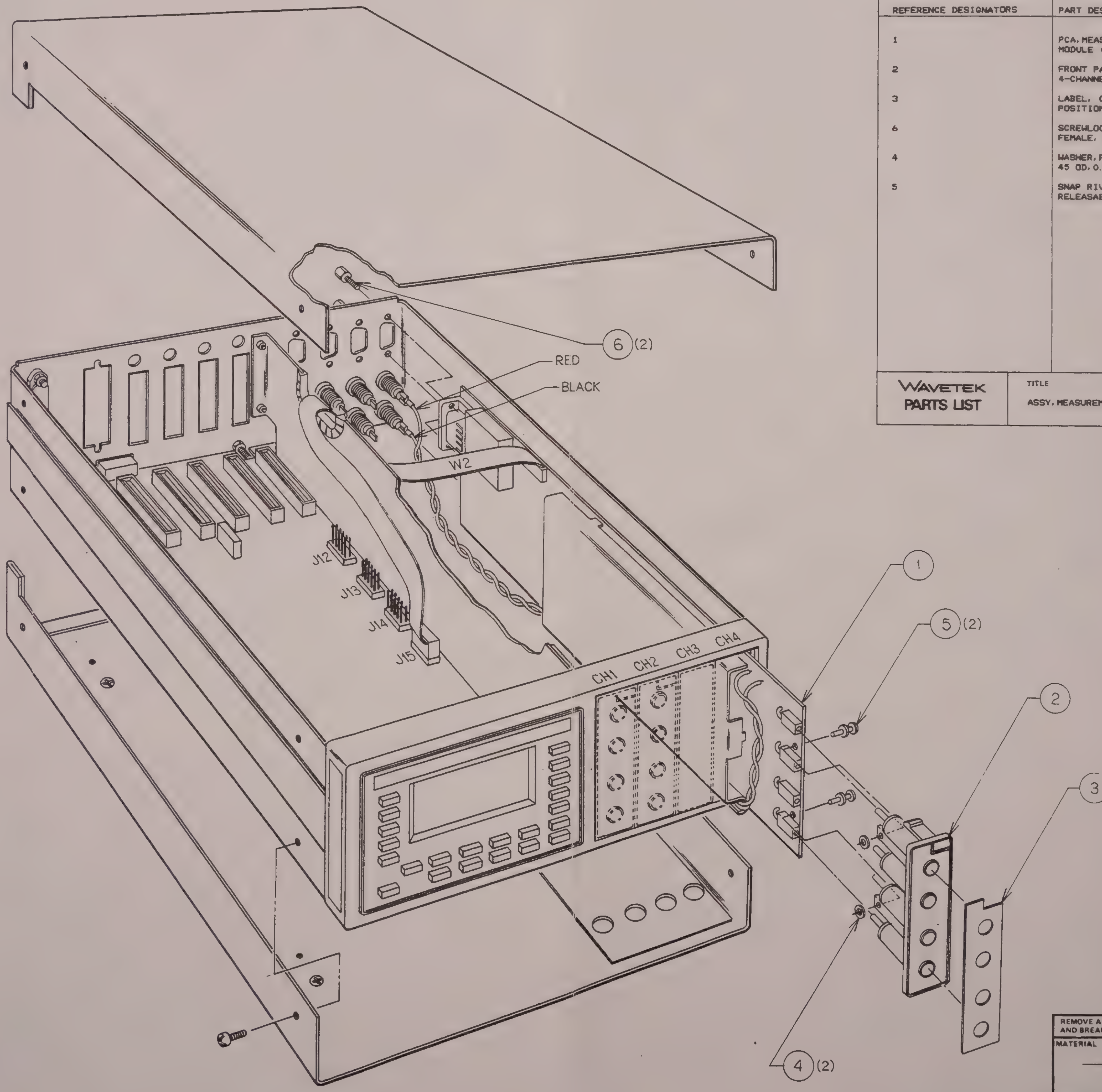
SIZE D | FSCM NO. 23338 | DWG. NO. 1100-00-2822 | REV E

SCALE | MODEL 51 | SHEET 2 OF 2

REV	ECN	BY	DATE	APP
A	FOR RELEASE			

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCA, MEASUREMENT MODULE (50-1)	52-1811	WVTK	1100-00-1811	1
2	FRONT PANEL, 4-CHANNEL	1400-02-0840	WVTK	1400-02-0840	1
3	LABEL, CHANNEL, 4 POSITION	52-1090	WVTK	1400-02-1090	1
6	SCREWLOCK, CONNECTOR, FEMALE, SHORT	205818-2	AMP	2100-07-0007	2
4	WASHER, FLAT, NYLON, 0.245 OD, 0.128 ID	5610-55-20	SESTM	2800-26-0026	2
5	SNAP RIVIT SHOULDER, RELEASABLE, NYLON	SR 3065 B	RICH	2800-60-0002	2

WAVETEK PARTS LIST	TITLE ASSY, MEASUREMENT MODULE 50-1	ASSEMBLY NO. 1000-00-0464 PAGE 1	REV A



3. MEASUREMENT MODULE 50-1 MAY BE INSTALLED IN CHANNEL 1, CHANNEL 2, CHANNEL 3, OR CHANNEL 4. SPECIFIC LOCATION(S) IS DEPENDENT UPON TOTAL INSTRUMENT CONFIGURATION.
2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0464

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3/25/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR N. E. Mull	4/14/86	TITLE ASSEMBLY, MEASUREMENT MODULE 50-1
	RELEASE APPROV C.		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52
	SCALE NONE		DWG NO. 1000-00-0464
			REV A
			CODE IDENT 23338
			SHEET 1 OF 1

A 1000-00-0464

SIPO Control Signals

Signal Name	Source & Location		Destination & Location	
A/D-A (see also FEN)	U30-4	2C6	U12-12 U20-2	1C2 2D5
A/D-B	U30-5	2C6	U12-13	1C2
LEDEN	U30-6	2C6	U20-13	2D3
FOUTA	U30-7	2C6	U31-11	3B1
FOUTB	U30-14	2C6	U31-10	3B1
FOUTC	U30-13	2C6	U31-9 U32-10	3B1 3B2
K5RST	U30-12	2C6	U8-3	2B7
K5SET	U30-11	2C6	U8-2	2B7
MUX A	U34-4	2A3	J6-1	2A4
MUX B	U34-5	2A3	J6-2	2A4
MUX C	U34-6	2A3	J6-3	2A4
MUX D	U34-7	2A3	J6-4	2A4
MUX E	U34-14	2A3	J6-5	2A4
MUX F	U34-13	2A3	J6-9	2A4
THRESHA	U34-12	2A3	J6-7 U19-10	2A4 3B5, 3A5
THRESHB	U34-11	2A3	U19-11	3B5, 3A5

SIPO Control Signals, continued

Signal Name	Source & Location		Destination & Location	
GAINA	U13-4	2A5	U6-10	1C4, 1D3
GAINB	U13-5	2A5	U6-9	1C4, 1D3
GAINC	U13-6	2A5	CR2-K U14-5	3C4 3B7
GAIND	U13-7	2A5	U18-8 U17-9 U14-8	3D4 3C6 3C7
(A/DINA), (OHMS)	U13-14	2A5	U8-4	2B7
(A/DINB), (OHMSA)	U13-13	2A5	U8-5	2B7
ACAMPS, (OHMSB)	U13-12 U13-12	2A5 2A5	U14-2 U8-6	3C7 2B7
$\overline{\text{DCCOUP}}$, (OHMSC)	U13-11 U13-11	2A5 2A5	U18-1 U8-7	3D3 2B7

Note: Signals in parenthesis () are inverted by U8 before being used by the measurement module.

Signal Name	Source & Location		Destination & Location	
$\overline{\text{A/DINA}}$, OHMS	U8-13 U8-13	2B7 2B7	U7B-9 U7A-9	1C5 4D5
$\overline{\text{A/DINB}}$, OHMSA	U8-12 U8-12	2B7 2B7	U7B-10 U7A-10	1C5 4D5
$\overline{\text{OHMSB}}$	U8-11	2B7	U2-10	4C4
$\overline{\text{OHMSC}}$	U8-10	2B7	U2-9	4C4
RP*MUX-S	U10-4	2A6	U9-1	2C7
AC-S	U10-5	2A6	U9-2	2C7
OHMS-S	U10-6	2A6	U9-3	2C7
DC-S	U10-7	2A6	U9-4	2C7
RP*MUX-R	U10-14	2A6	U9-5	2C7
AC-R	U10-13	2A6	U9-6	2C7
OHMS-R	U10-12	2A6	U9-7	2C7
DC-R	U10-11	2A6	U8-1	2C7

Other Signals

Signal Name	Source & Location		Destination & Location	
OHMSRC	K2-9	4B7	J1	1D7
VREF	VR1-K	1C3	U4-3 U12-9	4C7 1C2
AC1	K1-13	1D7	AC2 (If 50-2 module)	1D6
AC1	K1-13	1D7	K3-13 (If 50-1 module)	3D7
AC2	K3-11 (If 50-1 module)	3D8	R6	1D6
MA-IN	R14 (R3)	4B1	U7-12	1C6
A-IN	R13 (R4)	4B1	U7-14	1C6
mA-Lo	mA-Lo	1B6	R3-top	4C2
A/DMUX	U7-13	1C5	U17-6	3C6
ACOUT	U16-14	3C2	U6-4	1D3
$\overline{\text{FEN}}$ (see also A/D-A)	U30-4	2C6	U31-7 U20-2	3B1 2D5
OUT	U12-14	1C2	U20-1	2D5
FOUT	U31-6	3B1	U20-4	2D5

Table 7-1. Measurement Module Signal Sources and Destinations

+6VRAW

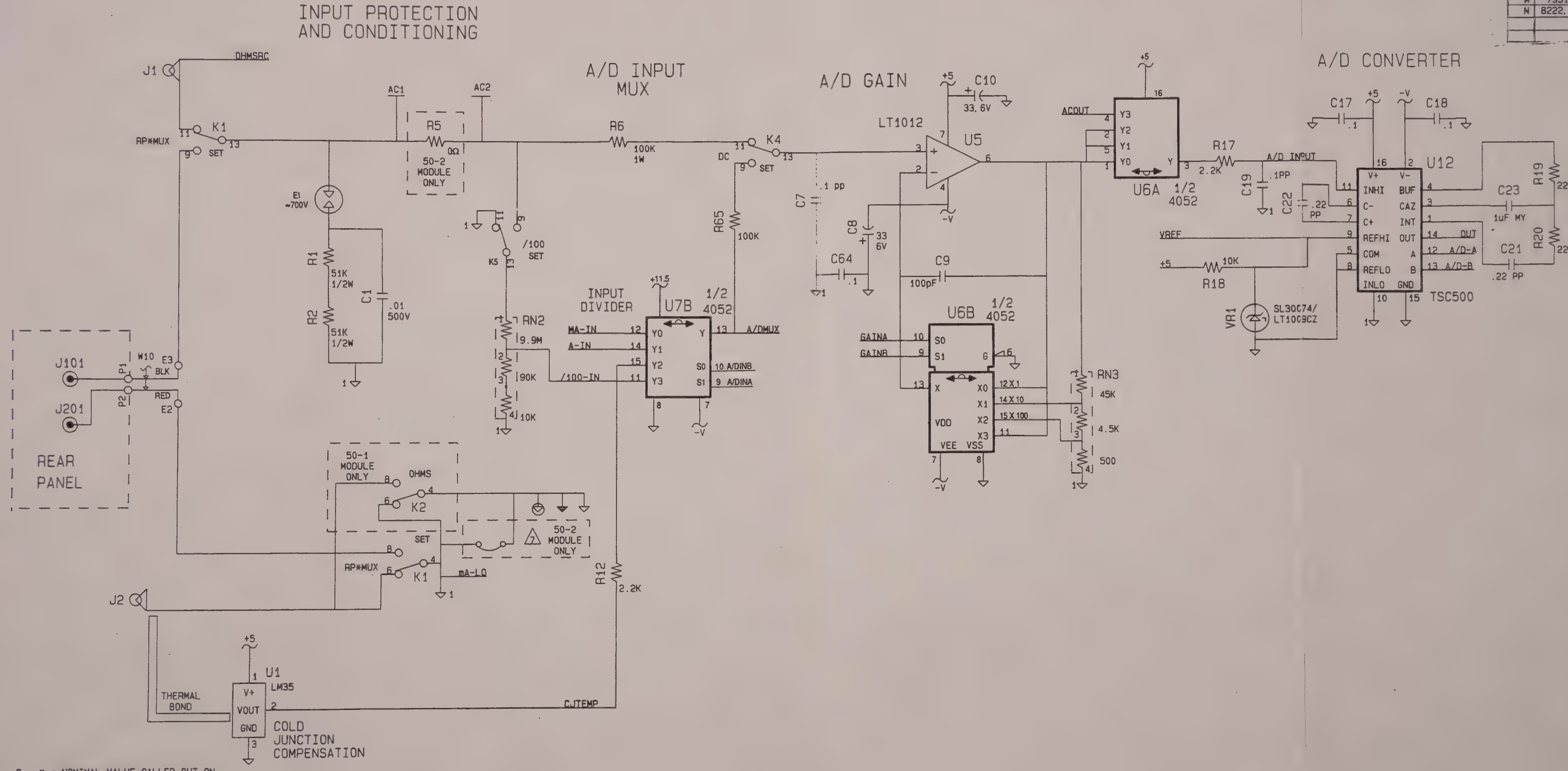
Devices: Relay coils of K1, K2, K3, K4, K5. U9-9.

Location: Sheet 2, zone 8

Voltage	Device	Location
+5	U1-1	1B7
	U5-7	1D4
	U6-16	1D3, 1C4
	R18	1C3
	U12-16	1D2
	U30-16	2D6
	U10-16	2B6
	U13-16, -15	2B5
	J6-6	2A4
	U34-16, -15	2B3
	U28-14	2C5
	U32-14	2C4, 3B2
	U29-14	Sheet 2
	R57	2D5
	U20-14, -9	Sheet 2
	U22-2	2D2
	U24-8	2C2, 2B2
	R55	2B2
	U23-8	2B2
	R53	2B2
	U14-14	3C7, 3B7
	U17-12	3C6, 3C5
	U18-12	3D4, 3C4, 3D3
	U19-16	3B5
	U27-14	3B3
	R49	3B4
	R48	3B4
	U33-16	3B2
	U32-14	3B2
	U31-16	3B1
-V	U5-4	1C4
	U6-7	1D3, 1C4
	U7-7	4C5, 1C5
	U12-2	1C2
	CR3-K (CR3-A feeds U17, U18)	3D5
	U19-7	3B5
+11.5V	U7-16	1C5, 4D5
	U8-9	2B7
	K3-4	3B8
	U3-8, -7	4B6
	U4-8	4C6, 4C4
	U7-16	4D5, 1C5
	U2-16	4C5, 4B4
	U17-13	3D6, 3C6, 3C5
	U18-13	3D4, 3C4, 3D3
+12VSW	U11-8	3A6
	U15-4	3D2, 3C4, 3D5, 3C7
	U21-11	3B4
	U16-11	3D2
-12	U15-11	3D2, 3C4, 3D5, 3C7
	U21-6	3B4
	U16-10	3C2
	CR4-K (CR4-A feeds U17, U18)	3D5

Table 7-2. Measurement Module Power Line Destinations

REV	ECN	BY	DATE	APP
E	FOR RELEASE	OT		
F	7403	OT	8/27/86	
G	7596	OT	8/25/86	
H	7700	OT	9/26/86	
J	7769	OT	10/31/86	
K	7780	OT	12/22/86	
L	7896	OT	12/22/86	
M	7951	N.C.	2/4/87	
N	8222, 8410	OT	6/30/87	A.R.T.


INPUT PROTECTION AND CONDITIONING
A/D INPUT MUX
A/D GAIN
A/D CONVERTER
J1
OHMSRC
RP*MUX
K1
SET
AC1
AC2
R5
0Ω
50-2 MODULE ONLY
R6
100K 1W
DC
K4
E1 ≈700V
R1
51K 1/2W
R2
51K 1/2W
C1
.01 500V
K5
/100 SET
RN2
9.9M
90K
10K
INPUT DIVIDER
U7B
1/2 4052
+11.5
MA-IN
A-IN
/100-IN
A/DMUX
10 A/DINB
9 A/DINA
R65
100K
C7
.1 pp
C8
33 6V
C64
.1
C9
100pF
LT1012
U5
C10
33, 6V
+5
-V
U6B
1/2 4052
GAINA
GAINB
VDD
VEE VSS
12 X1
14 X10
15 X100
RN3
45K
4.5K
500
ACOUT
U6A 1/2 4052
R17
2.2K
A/D INPUT
C19
.1PP
C22
.22 PP
C17
.1
C18
.1
U12
TSC500
INHI
C-
C+
REFHI
COM
REFLO
INLO
BUF
CAZ
INT
OUT
A
B
GND
VREF
R18
10K
VR1
SL30074/ LT1009CZ
C23
1uF MY
C21
.22 PP
R19
220K
R20
22
OUT
A/D-A
A/D-B
J101
J201
W10
BLK
RED
P1
P2
E3
E2
REAR PANEL
50-1 MODULE ONLY
OHMS
K2
50-2 MODULE ONLY
mA-LO
R12
2.2K
J2
U1
LM35
V+
VOUT
GND
THERMAL BOND
CJTEMP
COLD JUNCTION COMPENSATION

8. * = NOMINAL VALUE CALLED OUT ON PARTS LIST.

△7 FOR 50-2 MODULE: INSTALL JUMPER BETWEEN PIN 4 & 6 OF K2.

△6 FOR 50-2 MODULE: INSTALL JUMPER BETWEEN PIN 2 & 3 OF VR3.

△5 (n) INDICATES CHANNEL NUMBER; E.G., IF J5 IS CONNECTED TO J13 THAN +LATCH (n) = +LATCH2 = +LATCH SIGNAL FOR CHANNEL 2 MODULE.

4. DIODES ARE RLS4148.

3. CAPACITORS VALUED IN MICROFARADS (uF).

2. RESISTORS VALUED IN OHMS, 1/8W, 5%.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

11. BEVELLED SIDE OF S.O. IC'S IDENTIFIES PIN 1 SIDE.

10. R5 IS A 0-OHM CHIP RESISTOR.

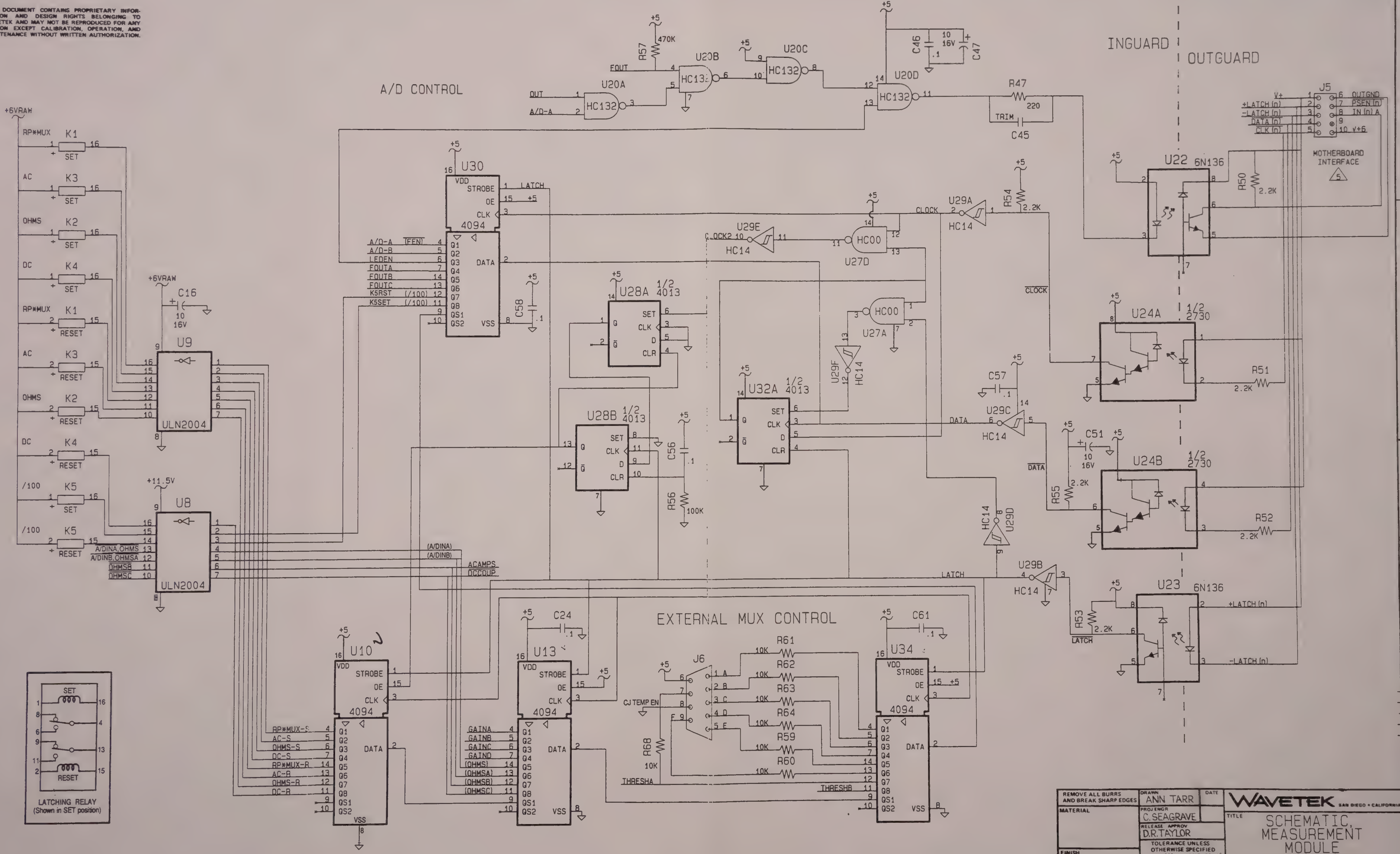
9. ON SHEET 2, CONTROL SIGNALS IN PARENTHESIS ARE INVERTED BEFORE BEING USED BY OTHER CIRCUITRY.

NOTE: UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO A2708

0103-00-1811 N

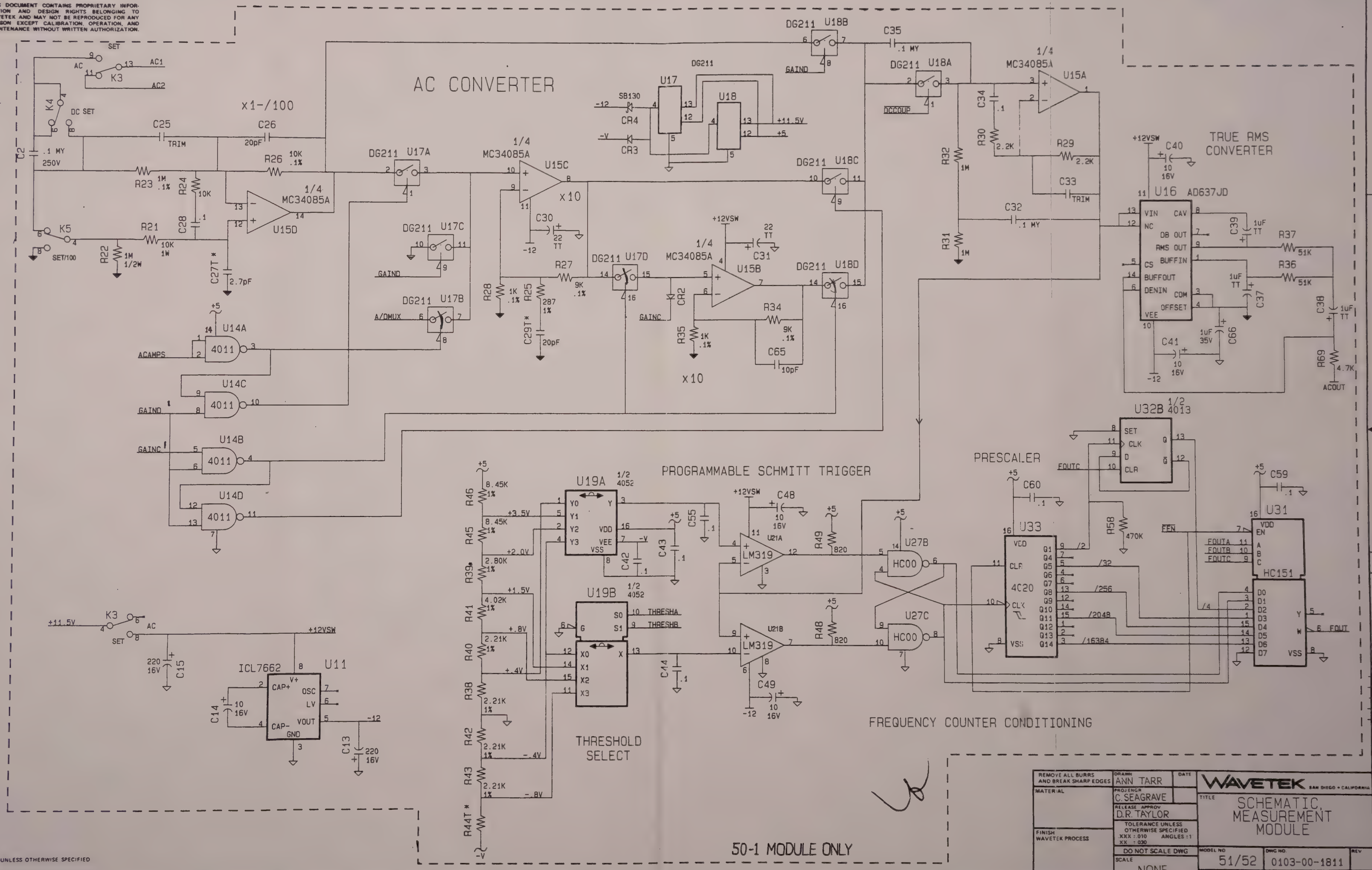
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ANN TARR	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR C. SEAGRAVE		TITLE SCHEMATIC, MEASUREMENT MODULE
	RELEASE APPROV D.R. TAYLOR		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 .XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO. 51/52
	SCALE NONE		DWG NO. 0103-00-1811
			REV N
			CODE IDENT 23338
			SHEET 1 OF 5


A/D CONTROL
EXTERNAL MUX CONTROL
INGUARD
OUTGUARD
+6VRAW
RP*MUX
AC
OHMS
DC
/100
K1
K3
K2
K4
K5
SET
RESET
C16
10 16V
U9
ULN2004
+11.5V
U8
ULN2004
A/DINA,OHMS
A/DINB,OHMSA
OHMSB
OHMSC
U30
4094
VDD
STROBE
OE
CLK
DATA
VSS
LATCH
A/D-A
A/D-B
LEDEN
FOUTA
FOUTB
FOUTC
K5RST
K5SET
(FEN)
(/100)
C58
OUT
FOUT
U20A
U20B
U20C
U20D
HC132
R57
470K
C46
C47
10 16V
R47
220
TRIM
C45
J5
V+
+LATCH (n)
-LATCH (n)
DATA (n)
CLK (n)
OUTGND
PSEN (n)
IN (n) A
V+6
MOTHERBOARD INTERFACE
U22
6N136
R50
2.2K
U29A
HC14
R54
2.2K
CLOCK
U29E
CLOCK2
U27D
HC00
U28A
1/2 4013
U28B
U32A
U27A
U29F
C57
U29C
DATA
C56
R56
100K
U24A
1/2 2730
R51
2.2K
U24B
C51
R55
R52
U29D
U29B
U23
R53
+LATCH (n)
-LATCH (n)
(A/DINA)
(A/DINB)
ACAMPS
DCCOUP
U10
U13
U34
C24
C61
J6
CJ TEMP EN
R61
R62
R63
R64
R59
R60
10K
R68
THRESHA
THRESHB
RP*MUX-S
AC-S
OHMS-S
DC-S
RP*MUX-R
AC-R
OHMS-R
DC-R
GAINA
GAINB
GAINC
GAIND
(OHMS)
(OHMSA)
(OHMSB)
(OHMSC)
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
QS1
QS2
LATCHING RELAY
(Shown in SET position)
REV
ECN
BY
DATE
APP
8
7
6
5
4
3
2
1
D
C
B
A

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ANN TARR	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR C. SEAGRAVE		TITLE SCHEMATIC, MEASUREMENT MODULE
	RELEASE APPROV D.R.TAYLOR		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 51/52	DWG NO 0103-00-1811 REV.
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 5

0103-00-1811


AC CONVERTER
x1-/100
K3
K4
K5
AC1
AC2
SET
AC
DC SET
SET/100
C2 .1 MY 250V
C25 TRIM
C26 20pF
R26 10K .1%
R23 1M .1%
R24 10K
C28 .1
R21 10K 1W
R22 1M 1/2W
C27T* 2.7pF
1/4 MC34085A U15D
DG211 U17A
DG211 U17B
DG211 U17C
DG211 U17D
1/4 MC34085A U15C
x10
C30 22 TT
R27 9K .1%
R28 1K .1%
R25 287 1%
C29T* 20pF
U14A 4011
U14B 4011
U14C 4011
U14D 4011
ACAMPS
GAIND
GAINC
A/DMUX
U17
U18
DG211
SB130 CR4
CR3
-12
-V
+11.5V
+5
1/4 MC34085A U15B
C31 22 TT
+12VSW
CR2
R34 9K .1%
R35 1K .1%
C65 10pF
DG211 U18A
DG211 U18B
DG211 U18C
DG211 U18D
C35 .1 MY
DCCOUP
1/4 MC34085A U15A
C34 .1
R30 2.2K
R29 2.2K
C33 TRIM
R32 1M
R31 1M
C32 .1 MY
TRUE RMS CONVERTER
U16 AD637JD
C40 10 16V
C39 1uF TT
C37 1uF TT
C38 1uF TT
C41 10 16V
C66 1uF 35V
R37 51K
R36 51K
R69 4.7K
ACOUT
VIN NC CAV DB OUT RMS OUT BUFFIN CS BUFFOUT DENIN COM OFFSET VEE
PROGRAMMABLE SCHMITT TRIGGER
U19A 1/2 4052
U19B 1/2 4052
THRESHA
THRESHB
R46 8.45K 1%
R45 8.45K 1%
R39 2.80K 1%
R41 4.02K 1%
R40 2.21K 1%
R38 2.21K 1%
R42 2.21K 1%
R43 2.21K 1%
R44T*
+3.5V
+2.0V
+1.5V
+.8V
+.4V
-.4V
-.8V
THRESHOLD SELECT
C55 .1
C42 .1
C43 .1
C44 .1
U21A LM319
U21B LM319
C48 10 16V
C49 10 16V
R49 820
R48 820
U27B HC00
U27C HC00
PRESCALER
U33 4020
C60 .1
R58 470K
U32B 1/2 4013
SET CLK D CLR Q
FOUTC
/2
/32
/256
/2048
/16384
/4
U31 HC151
C59 .1
FEN
FOUTA
FOUTB
FOUTC
FOUT
FREQUENCY COUNTER CONDITIONING
K3
+11.5V
+12VSW
C15 220 16V
U11 ICL7662
CAP+ CAP- GND OSC LV VOUT V+
C14 10 16V
C13 220 16V
-12
50-1 MODULE ONLY
0103-00-1811
REV ECN BY DATE APP

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN ANN TARR

DATE

PROJ ENGR C. SEAGRAVE

RELEASE APPROV D.R. TAYLOR

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
MEASUREMENT
MODULE

MODEL NO 51/52

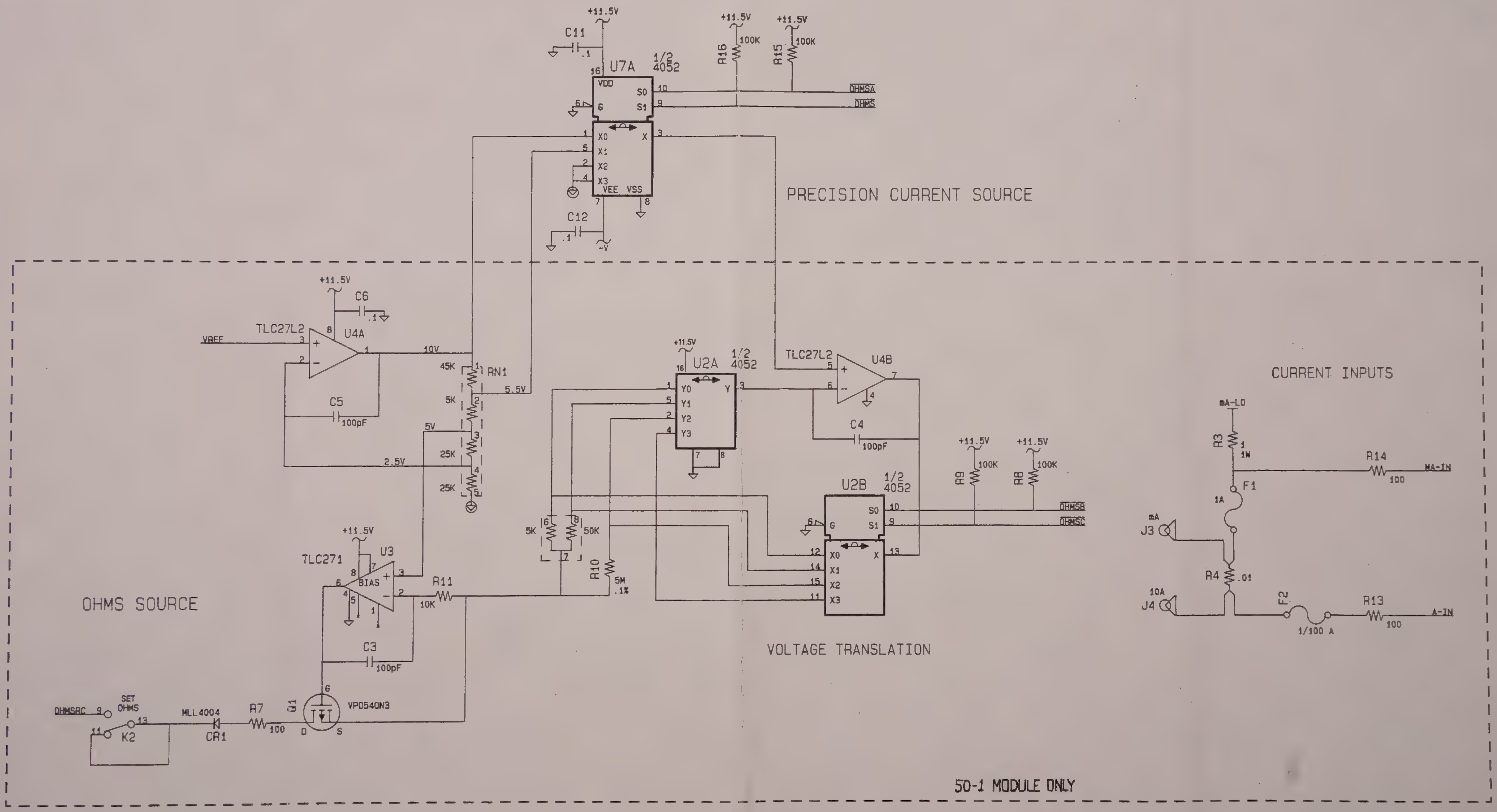
DWG NO. 0103-00-1811

REV

CODE IDENT 23338

SHEET 3 OF 5

REV	ECN	BY	DATE	APP

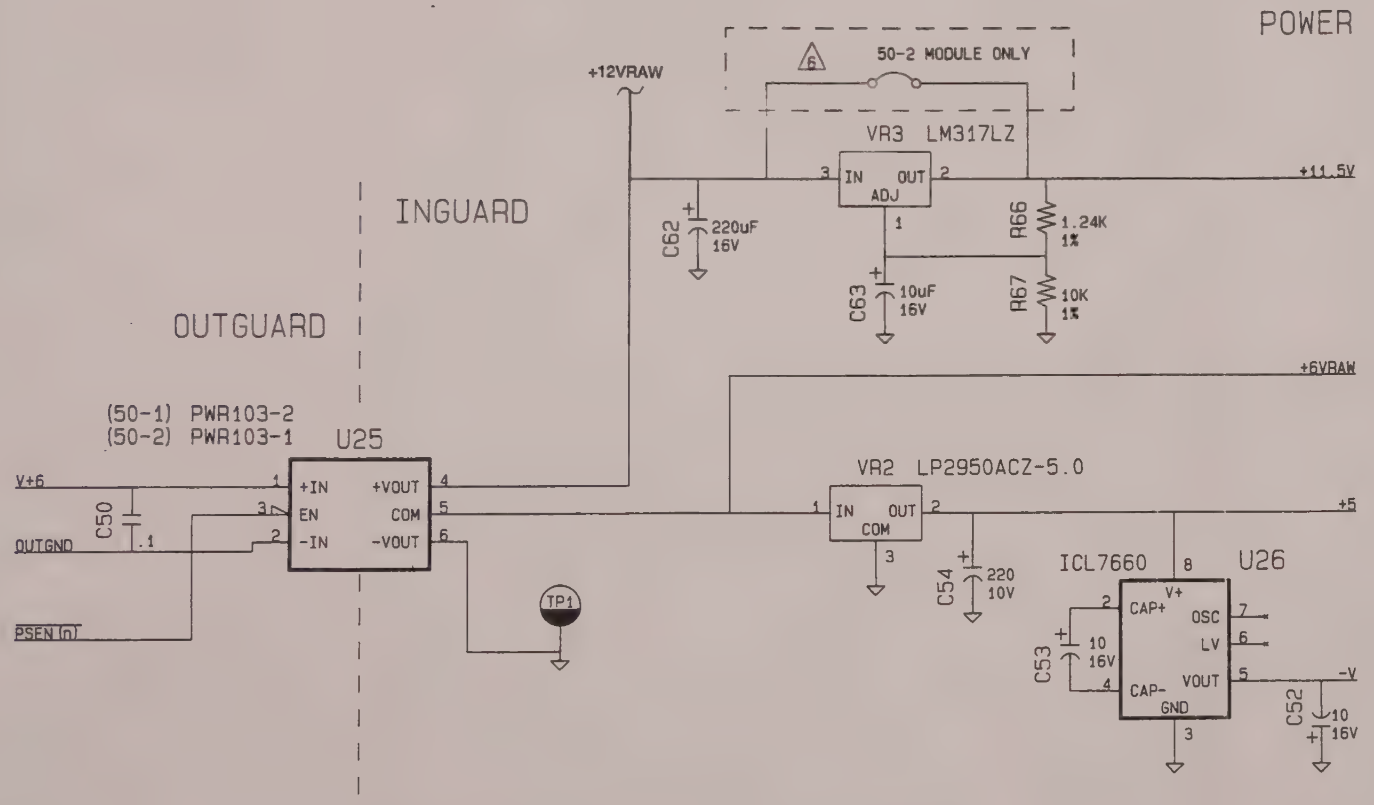

PRECISION CURRENT SOURCE
+11.5V
C11
.1
U7A
1/2
4052
16
VDD
S0
S1
G
6
10
9
R16
100K
R15
100K
OHMSA
OHMS
X0
X1
X2
X3
X
VEE
VSS
1
5
2
4
3
7
8
C12
.1
-V
OHMS SOURCE
TLC27L2
U4A
C6
.1
VREF
10V
RN1
45K
5K
25K
25K
5.5V
5V
2.5V
C5
100pF
TLC271
U3
BIAS
R11
10K
C3
100pF
Q1
VP0540N3
G
D
S
R7
100
MLL4004
CR1
OHMSRC
SET
OHMS
K2
9
13
11
VOLTAGE TRANSLATION
U2A
1/2
4052
Y0
Y1
Y2
Y3
Y
5K
50K
R10
5M
.1%
TLC27L2
U4B
C4
100pF
U2B
1/2
4052
S0
S1
G
X0
X1
X2
X3
X
12
14
15
11
13
R9
100K
R8
100K
OHMSB
OHMSC
CURRENT INPUTS
mA-LO
R3
1
1W
R14
100
MA-IN
F1
1A
mA
J3
R4
.01
10A
J4
F2
1/100 A
R13
100
A-IN
50-1 MODULE ONLY

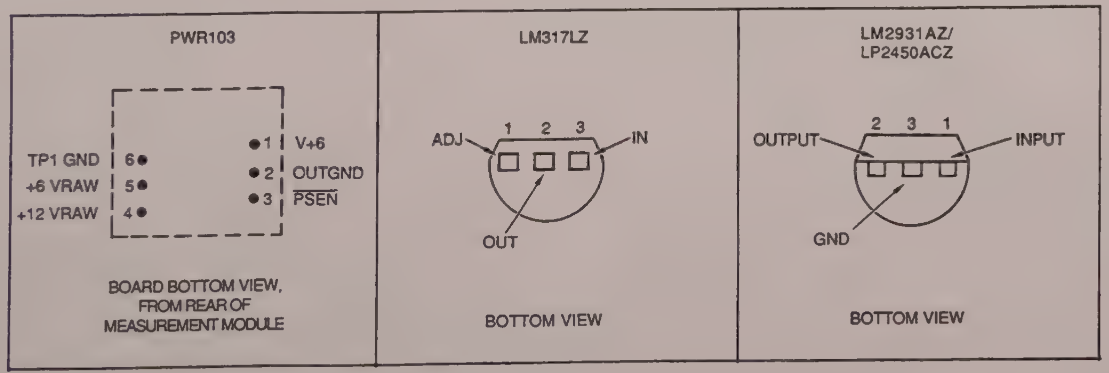
..TE: UNLESS OTHERWISE SPECIFIED

0103-00-1811

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ANN TARR	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR C. SEAGRAVE		TITLE SCHEMATIC, MEASUREMENT MODULE
	RELEASE APPROV D.R.TAYLOR		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52 — DWG NO. 0103-00-1811 — REV ---
	SCALE NONE		CODE IDENT 23338 — SHEET 4 OF 5

REV	ECN	BY	DATE	APP


POWER SUPPLY
50-2 MODULE ONLY
6
+12VRAW
VR3 LM317LZ
IN
OUT
ADJ
3
2
1
+11.5V
C62
220uF
16V
C63
10uF
16V
R66
1.24K
1%
R67
10K
1%
INGUARD
OUTGUARD
+6VRAW
(50-1) PWR103-2
(50-2) PWR103-1
U25
+IN
EN
-IN
+VOUT
COM
-VOUT
1
3
2
4
5
6
V+6
C50
.1
OUTGND
PSEN (n)
TP1
VR2 LP2950ACZ-5.0
IN
OUT
COM
1
2
3
+5
C54
220
10V
ICL7660
U26
8
V+
CAP+
CAP-
GND
OSC
LV
VOUT
2
4
3
7
6
5
C53
10
16V
-V
C52
10
16V

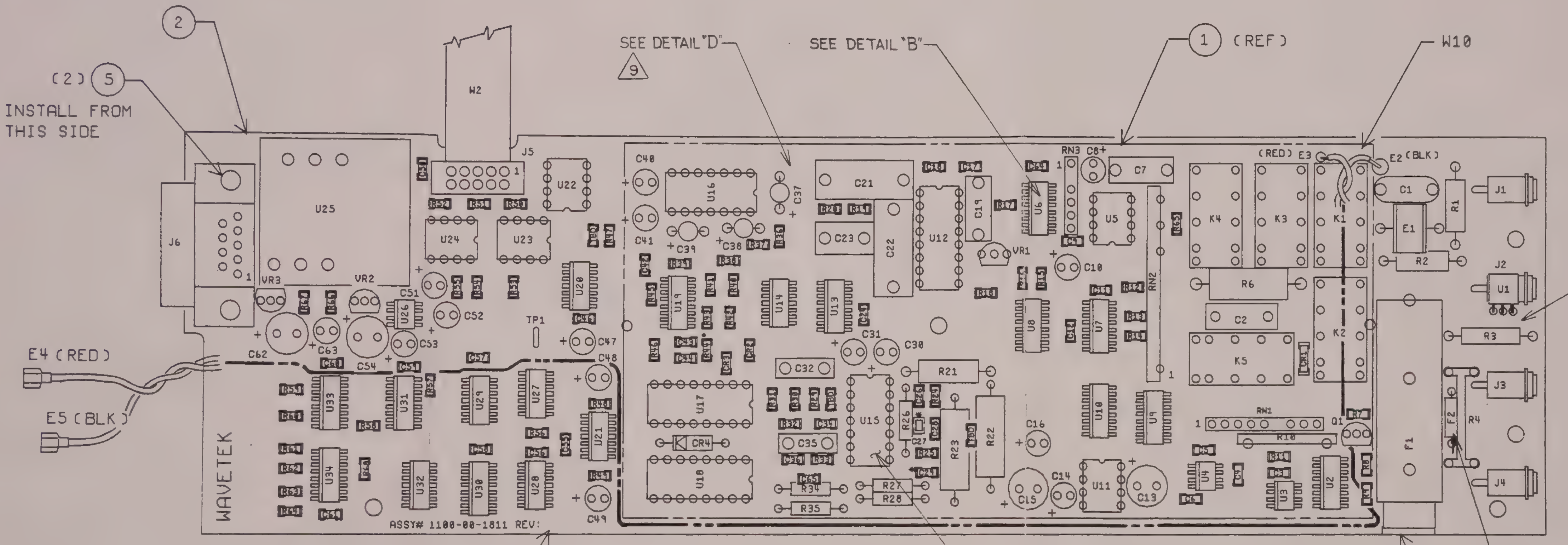

PWR103
TP1 GND
+6 VRAW
+12 VRAW
6
5
4
1
2
3
V+6
OUTGND
PSEN
BOARD BOTTOM VIEW, FROM REAR OF MEASUREMENT MODULE
LM317LZ
ADJ
1
2
3
IN
OUT
BOTTOM VIEW
LM2931AZ/ LP2450ACZ
OUTPUT
2
3
1
INPUT
GND
BOTTOM VIEW

0103-00-1811

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN ANN TARR
DATE
PROJ ENGR C. SEAGRAVE
RELEASE APPROV D.R. TAYLOR
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE SCHEMATIC, MEASUREMENT MODULE
MODEL NO. 51/52
DWG NO. 0103-00-1811
REV
CODE IDENT 23338
SHEET 5 OF 5

REV	ECN	BY	DATE	APP
E	FOR RELEASE	B.R.	4/3/86	N.M.
F	7403	A.T.	5/21/86	A.R.T.
G	7593	[illegible]	7/11/86	A.R.T.
H	7596	[illegible]	9/25/86	A.R.T.
J	7700	[illegible]	9/29/86	A.R.T.
K	7769	[illegible]	11/3/86	A.R.T.
L	7789	[illegible]	12/22/86	A.R.T.
M	7896	[illegible]	12/22/86	A.R.T.
N	7951	N.C.	2/4/87	A.R.T.
P	8222	[illegible]	6/30/87	A.R.T.



2
(2) 5
INSTALL FROM THIS SIDE
W2
SEE DETAIL "D"
9
SEE DETAIL "B"
1 (REF)
W10
J5
J6
U25
U22
U24
U23
U16
U12
U5
K4
K3
K1
K2
K5
C1
E1
E2 (BLK)
E3
(RED)
R1
R2
R3
R4
R6
F1
F2
J1
J2
J3
J4
U1
RN1
RN2
RN3
C8
C7
C2
C21
C22
C23
C19
U6
VR1
VR2
VR3
C10
C18
U8
U7
U9
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C13
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C40
C41
C47
C48
C49
C51
C52
C53
C54
C62
C63
CR4
R10
R21
R22
R23
R26
R27
R28
R34
R35
TP1
Q1
E4 (RED)
E5 (BLK)
WAVETEK
ASSY# 1100-00-1811 REV:

4

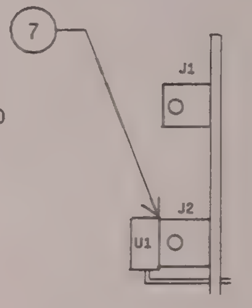
SEE DETAIL "C"

8

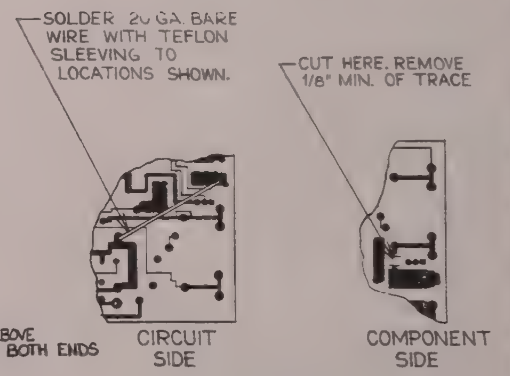
INSTALL F2 APPROX. 1/4" ABOVE BOARD AND TEFLON SLEEVE BOTH ENDS

3

BOND U1 TO J2 USING THERMAL ADHESIVE (1600-03-0019)

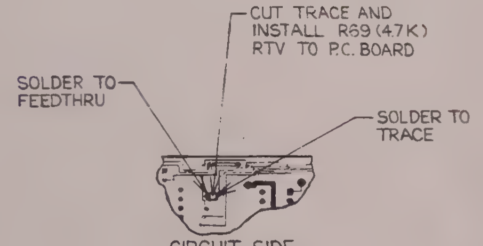


SEE DETAIL "A"



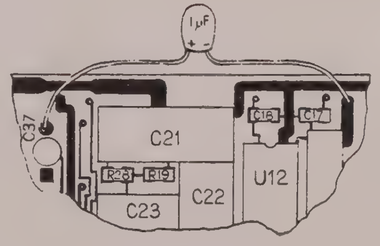
SOLDER 20 GA BARE WIRE WITH TEFLON SLEEVING TO LOCATIONS SHOWN.
CUT HERE, REMOVE 1/8" MIN. OF TRACE
CIRCUIT SIDE
COMPONENT SIDE

DETAIL "A"



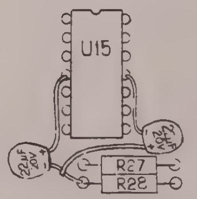
CUT TRACE AND INSTALL R69 (4.7K) RTV TO P.C. BOARD
SOLDER TO FEEDTHRU
SOLDER TO TRACE
CIRCUIT SIDE

DETAIL "B"

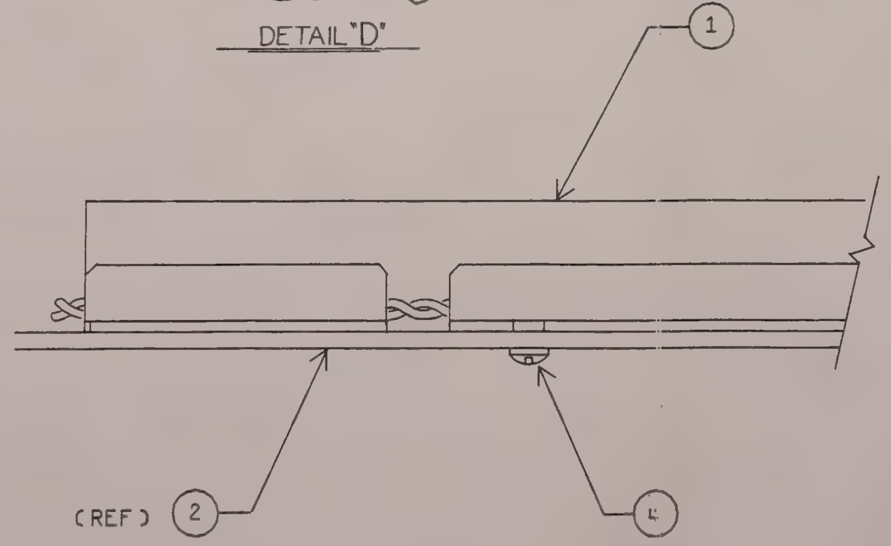


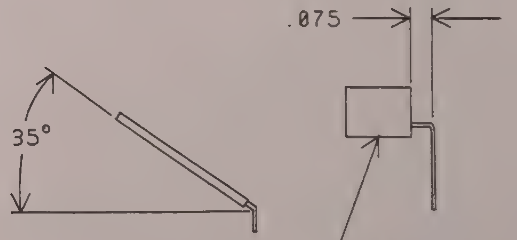
1µF
C37
C21
C18
C17
C22
C23
U12

DETAIL "D"



DETAIL "C"





RN2

U1

SPECIAL COMPONENT PREP

SCALE: NONE

9 ADD A 22GA BARE WIRE WITH TEFLON SLEEVING TO (+) LEAD OF 1UF CAP, SOLDER TO (-) LEAD OF C37 TOPSIDE; SOLDER (-) LEAD OF 1UF CAP TO GROUND HOLE NEAR C19. RTV THE BODY OF 1UF CAP TO P.C. BOARD. (SEE DETAIL "D".)

8 BEND LEADS OF 2 CAPS ABOUT 1/4" HIGH, SOLDER (+) LEAD TO PIN 4, (-) LEAD TO PIN 11 OF U15. SOLDER 2 REMAINING LEADS TOGETHER, BEND 1/4" HIGH, SOLDER TO R28. (SEE DETAIL "C".)

7. ✱ = NOMINAL VALUE CALLED OUT ON PARTS LIST.

6. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.

5. TRIM COMPONENT LEADS TO A MAXIMUM HEIGHT OF .045 FROM BOARD SURFACE.

4 MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.

3. SEE INSTRUMENT SCHEMATIC 0004-00-0040 FOR ASSEMBLY INTERCONNECTION.

2. SEE 0103-00-1811 FOR CIRCUIT SCHEMATIC.

1. SEE PARTS LIST 1100-00-1811.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1101-00-1811

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B.REDMAN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	PROJ ENGR C.SEAGRAVE	4/23/86	TITLE PCA, MEASUREMENT MODULE (50-1)
	RELEASE APPROV D.R.TAYLOR		
FINISH WAVETEK PROCESS —//—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52
	SCALE 2/1		DWG NO 1100-00-1811
			REV P
			CODE IDENT 23338
			SHEET 1 OF 1

1100-00-1811 P

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PCA, CHANNEL BOARD	0103-1811	WVTK	0103-00-1811	1
W10	ASSY, CABLE (W-10)	1207-00-2806	WVTK	1207-00-2806	1
1	SHIELD, AC CONVERTER	1400-02-0733	WVTK	1400-02-0733	1
C1	CAP, CER, .01/500V	ECK-D2H103ZEE	PANAS	1500-01-0306	1
C14 C16 C40 C41 C47 C48 C49 C51 C52 C53 C63	CAP, ELECT, 10MF, 20%, 16V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	11
C54	CAP, ELECT, 220MF/10V	ECEA1AU221	PANAS	1500-32-2001	1
C13 C15 C62	CAP, ELECT, 220 MF, 20%, 16V	SSM220M16S	ITT	1500-32-2104	3
C2	CAP, MET, POLY, .1MF, 250V	160-.1-J250D	WEST	1500-41-0405	1
C19 C7	CAP, MET POLY, .1PP, 160V	171-.1-J160D	WEST	1500-41-0434	2
C23	CAP, MET POLY, 1MF/63V	167-1-J63D	WEST	1500-41-0503	1
C21 C22	CAP, MET POLY, 022PP, 160V	171-.22-J160H	WEST	1500-42-2025	2
C32 C35	CAP, MET, POLY, .1MF, 63V, 5% RAD LEAD SP .3	167/.1/J/63/A	WEST	1500-43-0413	2
C37 C38 C39 C66	CAP, TANT, 1MF, 35V	196D105X0035HA1	SPRAG	1500-71-0512	4

WAVETEK
PARTS LIST
TITLE
PCA, MEASUREMENT MODULE (50-1)
ASSEMBLY NO.
1100-00-1811
REV
P
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C30 C31	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	2
C10 C8	CAP, TANT, 33MFD, 6V, RADIAL, LS .125	199033696R3CA1	SPRAG	1500-73-3602	2
C65	SMD, CAP, CER, NPO, 10PF 5% 50V	C1206C100D2GAC	KEMET	1500-81-0001	1
C3 C4 C5 C9	SMD, CAP, CER, 2%, 50V, NPO 100PF	C1206C101J2GAC	KEMET	1500-81-0101	4
C11 C12 C17 C18 C24 C28 C34 C42 C43 C44 C46 C50 C55 C56 C57 C58 C59 C6 C60 C61 C64	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	21
C26	SMD, CAP, CER, 2%, 50V, 20PF	C1206C200G5GAC	KEMET	1500-82-0001	1
C27T	SMD, CAP CERAM, NPO, 0805 STD SIZE, 2.7PF+-0.5	C0805C279D2GAC	KEMET	1500-82-7901	1
C29T	SMD, CAP, CER, 2%, 50V, 33PF	C1206C330J2GAC	KEMET	1500-83-3001	1
7	ADHESIVE, THERMAL, EPOXY	00241	LKTIT	1600-03-0019	1
2	DRILL DRWG, PCA, CHANNEL BOARD	1700-1811	WVTK	1700-00-1811	1
J1 J2 J3 J4	PC JACK	09-9094-1-04	CONCD	2100-02-0190	4

WAVETEK
PARTS LIST
TITLE
PCA, MEASUREMENT MODULE (50-1)
ASSEMBLY NO.
1100-00-1811
REV
P
PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
J6	CONNECTOR, RT ANGLE PC MOUNT, 9 PIN	745394-2	AMP	2100-02-0200	1
TP1	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	1
F1	FUSE, 1A, 250V	312001	LITFU	2400-05-0007	1
3	FUSE HOLDER, PCB MOUNT	345101	LITFU	2400-05-0043	1
E1	SPARK GAP	BZ-B600	SIEM	2400-05-0046	1
F2	FUSE, AXIAL LEAD MOUNT, 10MA	GFA1/100A	BUSS	2400-05-0054	1
4	SCREW, SELF LOCKING, PAN HEAD 4-40X3/16	4-40 X 3/16	CMRCL	2800-23-4103	1
5	PIN SNAPLOCK, NYLON, PERMANENT, 1/8 HOLE	SLP-125.01	RICH	2800-60-0003	2
K1 K2 K3 K4 K5	RELAY, 2 FORMC	DS2E-SL2-DC5V	ARROW	4500-00-0028	5
R22	RES, C, 1/2W, 2%, 1M	DCS-1/2	DALE	4700-24-1004	1
R28 R35	RES, MF, 1/8W, .1%, 1K	RN55E-1001B	MEPCO	4701-02-1001	2
R26	RES, MF, 1/8W, .1%, 10K	RN55E-1002B	MEPCO	4701-02-1002	1
R27 R34	RES, MF, 1/8W, .1%, 9K	5023ZE9K00B	MEPCO	4701-02-9001	2
R23	RESISTOR, FIXED VALUE METAL FILM, 1 MEG,	CMF-65 1004 B T-9	DALE	4701-32-1004	1

WAVETEK
PARTS LIST
TITLE
PCA, MEASUREMENT MODULE (50-1)
ASSEMBLY NO.
1100-00-1811
REV
P
PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	0.1%				
R21	RES, MF, 1W, 5%, 10K	RSF1B	MICRO	4701-35-1002	1
R10	RES, MF, .33W, .1%, 5M	TF626R	CADD	4701-82-5004	1
R3	RES, WW, 1W, 1%, 1	RS1A 1 OHM 1%	DALE	4702-33-1009	1
R4	RES, WW, 10W, .5%, .01	SPR-676	DALE	4702-79-0107	1
R13 R14 R7	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 100 OHM	9C12063A1000JLR	MEPCO	4703-20-1015	3
R11 R18 R24 R59 R60 R61 R62 R63 R64 R68	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 10K OHM	MCR18EZH103JW5%	ROHM	4703-20-1035	10
R15 R16 R56 R65 R8 R9	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 100K OHM	MCR18EZH104JW5%	ROHM	4703-20-1045	6
R31 R32	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 1M OHM	MCR18EZH105JW5%	ROHM	4703-20-1055	2
R20	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5% 22 OHM	MCR18EZH220JW5%	ROHM	4703-20-2205	1
R12 R17 R29 R30 R50 R51 R52 R53 R54 R55	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5% 2.2K OHM	MCR18EZH222JW5%	ROHM	4703-20-2225	10
R19	SMD, GP RESISTOR, 1/8	9C12063A2203JLR	MEPCO	4703-20-2245	1

WAVETEK
PARTS LIST
TITLE
PCA, MEASUREMENT MODULE (50-1)
ASSEMBLY NO.
1100-00-1811
REV
P
PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	LONG, 200PPM, 5%, 220K OHM				
R47	RES, SMD, GP, 1/8 LONG, 200PPM, 5%, 470	0108-00-2766	WVTK	4703-20-4715	1
R69	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 4.7K OHM	MCR18EZH472JW5%	ROHM	4703-20-4725	1
R57 R58	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 470K OHM	MCR18EZH474JW5%	ROHM	4703-20-4745	2
R36 R37	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 51K OHM	MCR18EZH513JW5%	ROHM	4703-20-5135	2
R48 R49	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 820 OHM	MCR18EZH821JW5%	ROHM	4703-20-8215	2
R67	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 10K OHM	9C12063A1002FKR	MEPCO	4703-21-0021	1
R66	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 1.24K OHM	MCR18FXTA1241F	ROHM	4703-21-2411	1
R38 R40 R42 R43	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 2.21K OHM	9C12063A2211FKR	MEPCO	4703-22-2111	4

WAVETEK
PARTS LIST
TITLE
PCA, MEASUREMENT MODULE (50-1)
ASSEMBLY NO.
1100-00-1811
REV
P
PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R44T	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 23.7K OHM	9C12063A2372FKR	MEPCO	4703-22-3721	1
R39	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 2.80K OHM	9C12063A2801FKR	MEPCO	4703-22-8011	1
R25	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 287 OHM	MCR18FXTA2870F	ROHM	4703-22-8701	1
R41	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 4.02K OHM	MCR18FXTA4021F	ROHM	4703-24-0211	1
R45 R46	SMD, RESISTOR, 1/8 LONG, 100PPM, 1%, 8.45K OHM	9C12063A8451FKR	MEPCO	4703-28-4511	2
RN2	RES NETWORK	1776-8	CADDO	4770-00-0040	1
RN3	RES NETWORK	T1794-180-2	CADDO	4770-00-0041	1
RN1	RES NETWORK	T1794-181	CADDO	4770-00-0042	1
R6	RES, CC, 1W, 10%, 100K	GB1041	AB	4799-00-0092	1
R1 R2	RES, CC, 1/2W, 5%, 51K	EB5131	AB	4799-00-0093	2
CR4	DIODE, STTKY	SB130	GI	4806-02-0130	1

WAVETEK
PARTS LIST
TITLE
PCA, MEASUREMENT MODULE (50-1)
ASSEMBLY NO.
1100-00-1811
REV
P
PAGE 6

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
WAVETEK SAN DIEGO, CALIFORNIA
TITLE
PARTS LIST
MEASUREMENT MODULE
SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-1811
REV P
SCALE
MODEL 50-1
SHEET 1 OF 2

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR1	SMD, G.P. RECTIFIER 400V, 1A LEADLESS IN4004	MLL4004	MOT	4806-03-4004	1
CR2 CR3	SMD, DIODE, LEADLESS EQUIVALENT IN4148, 500MW	RLS4148	ROHM	4807-01-4148	2
Q1	TRANS, FET, P-CHANNEL	VP0540N3	SUPER	4902-05-4000	1
W2	RIBBON CABLE ASSEMBLY, 10 PIN, 10"	6002-00-0043	WVTK	6002-00-0043	1
U1	IC, CENTIGRADE TEMP SENSOR	LM35DZ	NAT	7000-00-3500	1
U3	SMD, IC, PROGRAM OP AMP	TLC271ACD	TI	7000-02-7101	1
U4	SMD, IC, DUAL OPERATIONAL AMPLIFIER	TLC27L2ACD	TI	7000-02-7210	1
VR3	VOLTAGE REGULATOR	LM317LZ	MOT	7000-03-1701	1
U21	SMD, DUAL DIFFERENTIAL COMPARATOR	LM319D	SIG	7000-03-1900	1
U12	IC, ANALOG PROCESSOR	TSC500L	TELE	7000-05-0000	1
U16	IC, RMS TO DC	AD637JD	ANDEV	7000-06-3700	1
U5	IC, PICOAMP INPUT MIC VOLT OFFSET LOW NOISE	LT1012CN8	LINTE	7000-10-1200	1

WAVETEK PARTS LIST
TITLE PCA, MEASUREMENT MODULE (50-1)
ASSEMBLY NO. 1100-00-1811
REV P
PAGE 7

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U25	IC, POWER SUPPLY	PWR103-2	BUR	7000-10-3201	1
U8 U9	SMD, DARLINGTON TRANSISTOR ARRAY	ULN2004D	SIG	7000-20-0001	2
VR2	REGULATOR, MICROPOWER VOLTAGE, 3 PIN	LP2950ACZ-5.0V	NSC	7000-29-5000	1
U19 U2 U6 U7	MUL/DEMUL, DUAL 4 CHANNEL ANALOG, SMD	HEF4052BTD	SIG	7000-40-5200	4
U26	SMD, DC TO DC CONVERTER, CMOS, 300MW	ICL7660CBA	INTSL	7000-76-6041	1
U11	DC TO DC CONVERTER, CMOS, 500MW, 8 PIN DIP	ICL7662CPA	INTSL	7000-76-6201	1
VR1	IC, VOLTAGE REFERENCE	7003-00-7400	WVTK	7003-00-7400	1
U15	IC, QUAD HIGH SPEED OP AMP	MC34085AP	MOT	7003-40-8500	1
U22 U23	OPTO CPLP, FAST	6N136	SPECT	7100-00-0001	2
U17 U18	CMOS, SW, QUAD ANALOG	DG211CJ	SILX	8000-02-1100	2
U24	IC, DUAL, LOW INPUT, HIGH GAIN OPTOCOUPL	HCLP2730	HP	8000-27-3000	1

WAVETEK PARTS LIST
TITLE PCA, MEASUREMENT MODULE (50-1)
ASSEMBLY NO. 1100-00-1811
REV P
PAGE 8

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U14	GATE, NAND, SG, QUAD 2-INPUT, SMD	HEF 4011BTD	SIG	8000-40-1102	1
U28 U32	FLIP-FLOP, DUAL D, CMOS, SMD	HEF4013BTD	SIG	8000-40-1341	2
U33	COUNTER, CMOS, BINARY, 14-STAGE, RIPPLE-CARRY, SMD	HEF4020BTD	SIG	8000-40-2041	1
U10 U13 U30 U34	REG/LATCH 8-BIT SHIFT CMOS, SMD	HEF4094BTD	SIG	8000-40-9441	4
U27	NAND, QUAD 2INP POS	74HC00D	SIG	8000-74-0041	1
U20	IC, SMD, QUAD 2-INPUT NAND SCHMITT TRIGGER	74HC132D	SIG	8000-74-1320	1
U29	SMD, HEX SCHMITT TRIGGER/INVERTER, HCMOS	74HC14D	SIG	8000-74-1441	1
U31	CMOS, MUX, 8INP	74HC151D	SIG	8007-41-5141	1

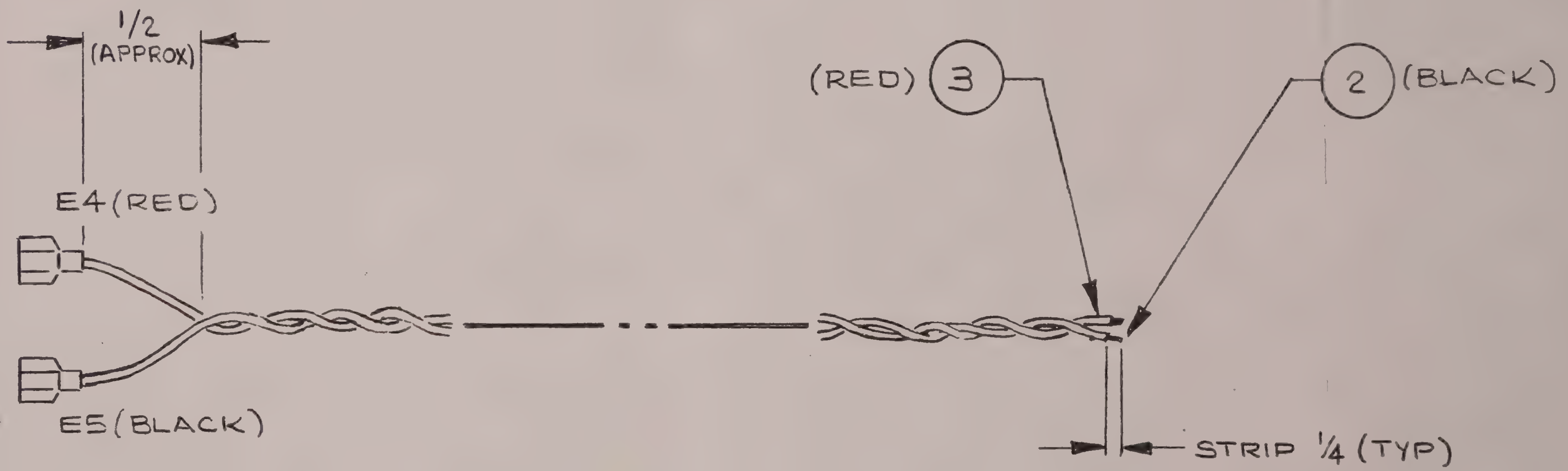
WAVETEK PARTS LIST
TITLE PCA, MEASUREMENT MODULE (50-1)
ASSEMBLY NO. 1100-00-1811
REV P
PAGE 9

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± .XXX ± ±
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
MEASUREMENT MODULE
SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-1811
REV P
SCALE
MODEL 50-1
SHEET 2 OF 2

1207-00-2806 B

REV	ECN	BY	DATE	APP
A	RED WIRE WAS 13 5/8 LG BLK WIRE WAS 14 LG	BR	3/19/86	NM
B	7591 - WIRE WAS 22 AWG		7/14/86	A.R.T.



WIRE LIST			
REF DES	AWG	COLOR	LENGTH
W10	20	RED	15
	20	BLACK	14 1/2

NOTE: USE #20 AWG TEFLON (600V) INSULATED WIRE
6000-10-2000 (BLACK)
6000-10-2002 (RED)

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
E4, E5	RECEPTACLE, LAB, SOLDERLESS,	23.5201	INLOK	2100-03-0084	2
2	WIRE, TEFLON, 20GA (BLACK)	6000-10-2000	WVTK	6000-10-2000	14.5
3	WIRE, TEFLON, 20GA (RED)	6000-10-2002	WVTK	6000-10-2002	15

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	ASSY, CABLE (W-10)	1207-00-2806 PAGE 1	B

∴ SEE PARTS LIST 1207-00-2806

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL —//—
FINISH WAVETEK PROCESS —//—

DRAWN B. REDMAN DATE 2/19/86
PROJ ENGR N. E. Miller 4/10/86
RELEASE APPROV C. Deagrone
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE

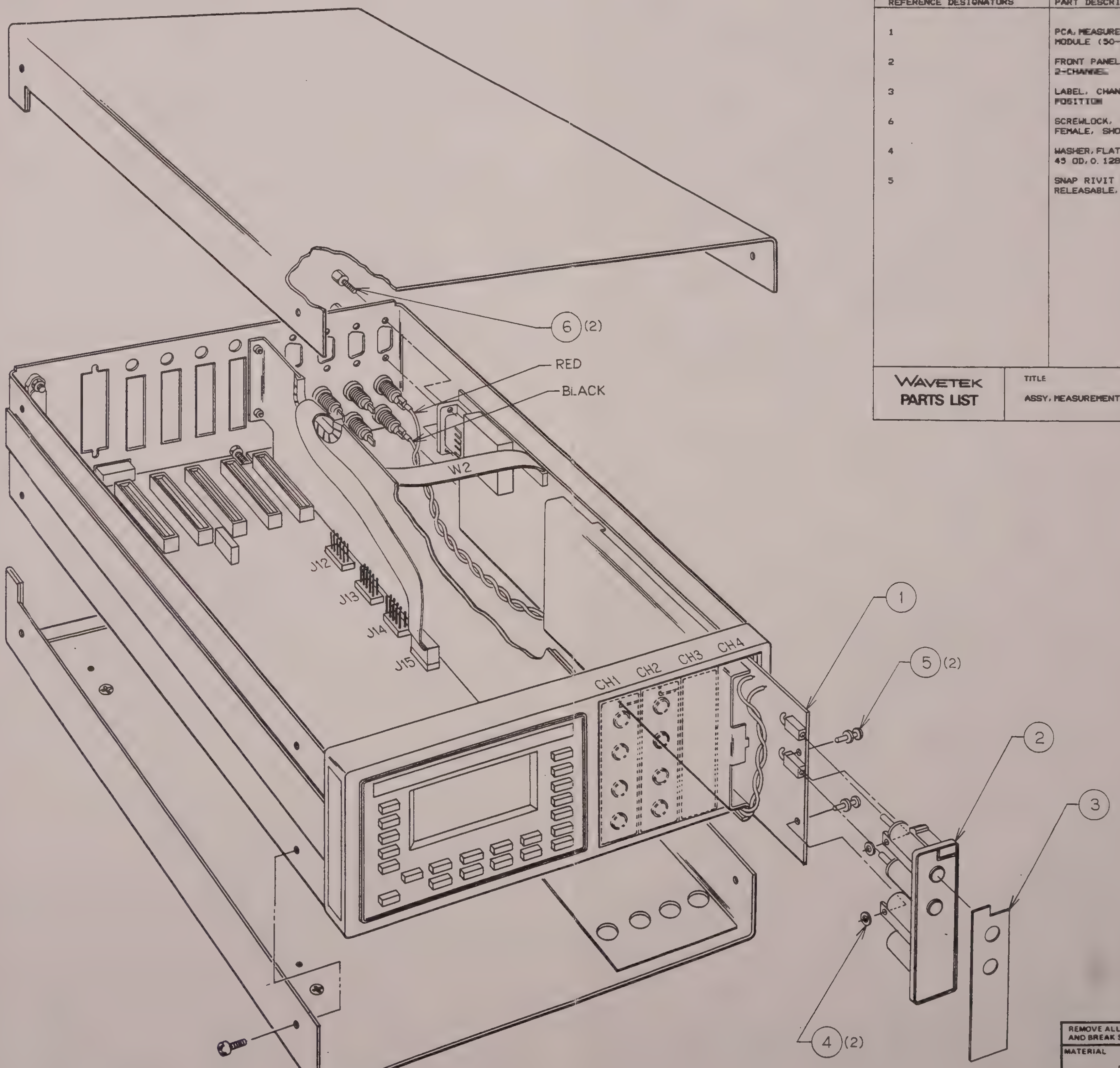
WAVETEK SAN DIEGO • CALIFORNIA
TITLE ASSEMBLY— CABLE (W10)
MODEL NO. 51/52
DWG NO. 1207-00-2806
REV B
CODE IDENT 23338
SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4829

REV	ECN	BY	DATE	APP
A	FOR RELEASE	ACT	3/27/86	NM

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCA, MEASUREMENT MODULE (50-2)	52-2615	WVTK	1100-00-2615	1
2	FRONT PANEL, 2-CHANNEL	52-0850	WVTK	1400-02-0850	1
3	LABEL, CHANNEL, 2 POSITION	52-1100	WVTK	1400-02-1100	1
6	SCREWLOCK, CONNECTOR, FEMALE, SHORT	205818-2	AMP	2100-07-0007	2
4	WASHER, FLAT, NYLON, 0.245 OD, 0.128 ID	5610-55-20	SESTM	2800-26-0026	2
5	SNAP RIVIT SHOULDER, RELEASABLE, NYLON	SR 3065 B	RICH	2800-60-0002	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	ASSY, MEASUREMENT MODULE 50-2	1000-00-0465 PAGE 1	A



3. MEASUREMENT MODULE 50-2 MAY BE INSTALLED IN CHANNEL 1, CHANNEL 2, CHANNEL 3, OR CHANNEL 4. SPECIFIC LOCATION(S) IS DEPENDENT UPON TOTAL INSTRUMENT CONFIGURATION.

2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

1. FOR [illegible] INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-[illegible]0.

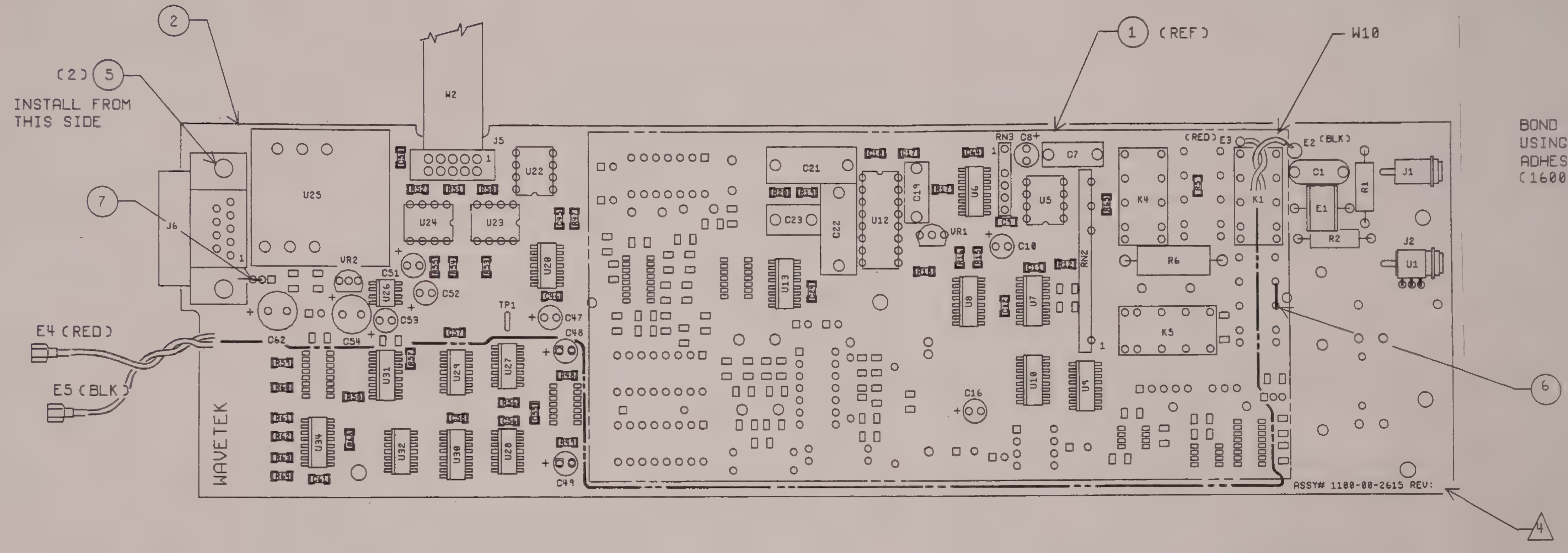
NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0465

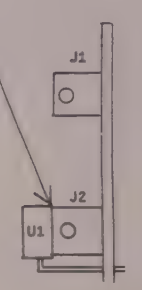
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3/25/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —/—	PROJ ENGR N. E. Mills	4/14/86	TITLE ASSEMBLY, MEASUREMENT MODULE 50-2
	RELEASE APPROV		
FINISH WAVETEK PROCESS —/—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52
	SCALE NONE		DWG NO. 1000-00-0465
			REV A
			CODE IDENT 23338
			SHEET 1 OF 1

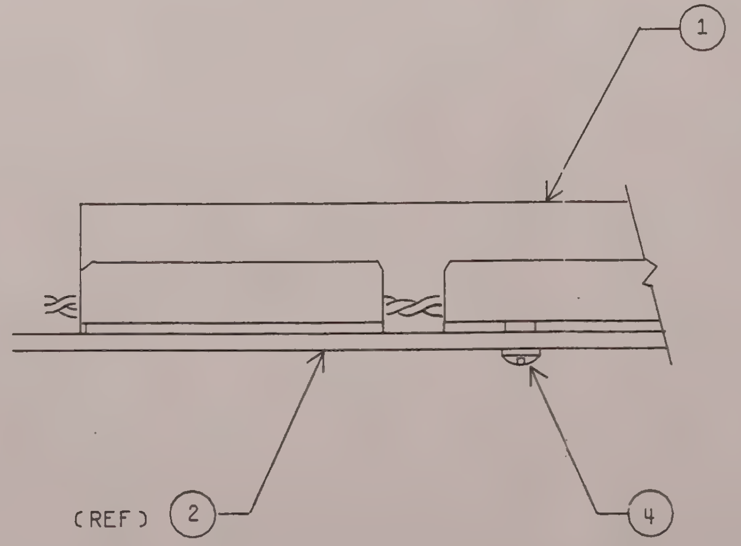
1000-00-0465 A

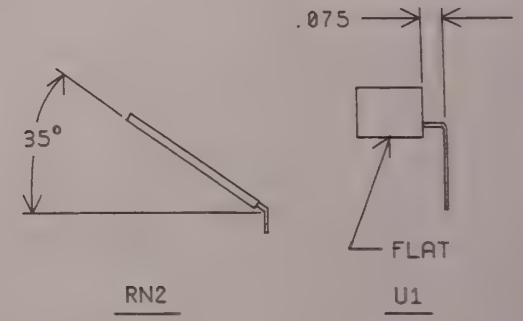
REV	ECN	BY	DATE	APP
E	FOR RELEASE	B.R.	4/3/86	N.M.
F	7403	A.T.	5/27/86	A.R.T.
G	7507	AT	7/1/86	A.R.T.
H	7596	AT	9/26/86	A.R.T.
J	7789	AT	12/22/86	A.R.T.
K	7951	K.C.	2/5/87	A.R.T.
L	8222	AT	7/9/87	A.R.T.


②
(2) ⑤
INSTALL FROM THIS SIDE
⑦
J6
U25
VR2
W2
J5
U22
U24
U23
C51
U26
C52
C53
TP1
C47
C48
C62
C54
E4 (RED)
E5 (BLK)
WAVETEK
U31
U29
U27
U20
U34
U32
U30
U28
C49
① (REF)
W10
C21
C23
C22
U12
C19
U13
U6
RN3
C8
C7
U5
VR1
C10
U8
U7
RN2
U10
U9
C16
(RED) E3
E2 (BLK)
K4
K1
C1
E1
R1
R2
J1
J2
U1
R6
K5
⑥
ASSY# 1100-00-2615 REV:
④

BOND U1 TO J2 USING THERMAL ADHESIVE (1600-03-0019)






.075
35°
FLAT
RN2
U1

SPECIAL COMPONENT PREP

SCALE: NONE

6. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
5. TRIM COMPONENT LEADS TO A MAXIMUM HEIGHT OF .045 FROM BOARD SURFACE.
△4 MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
3. SEE INSTRUMENT SCHEMATIC 0004-00-0040 FOR ASSEMBLY INTERCONNECTION.
2. SEE 0103-00-1811 FOR SCHEMATIC.
1. SEE PARTS LIST 1100-00-2615.

NOTE. UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1101-00-2615

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
—/—
FINISH
WAVETEK PROCESS
—/—
DRAWN B. REDMAN
DATE
PROJ ENGR SEAGRAVE
RELEASE APPROV D.R.TAYLOR
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE 2/1
WAVETEK SAN DIEGO • CALIFORNIA
TITLE PCA, MEASUREMENT MODULE (50-2)
MODEL NO. 51/52
DWG NO. 1100-00-2615
REV L
CODE IDENT 23338
SHEET 1 OF 1

1100-00-2615 L

BISHOP GRAPHICS/ACCUPRESS REORDER NO.

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PCA, CHANNEL BOARD	0103-1811	WVTK	0103-00-1811	1
W10	ASSY, CABLE (W-10)	1207-00-2806	WVTK	1207-00-2806	1
1	SHIELD, AC CONVERTER	1400-02-0733	WVTK	1400-02-0733	1
C1	CAP, CER, .01/500V	ECK-D2H103ZEE	PANAS	1500-01-0306	1
C16 C47 C51 C52 C53	CAP, ELECT, 10MF, 20%, 16V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	5
C54	CAP, ELECT, 220MF/10V	ECEA1AU221	PANAS	1500-32-2001	1
C62	CAP, ELECT, 220 MF, 20%, 16V	SSM220M16S	ITT	1500-32-2104	1
C19 C7	CAP, MET POLY, .1PP, 160V	171-.1-J160D	WEST	1500-41-0434	2
C23	CAP, MET POLY, 1MF/63V	167-1-J63D	WEST	1500-41-0503	1
C21 C22	CAP, MET POLY, 022PP, 160V	171-.22-J160H	WEST	1500-42-2025	2
C10 C8	CAP, TANT, 33MFD, 6V, RADIAL, LS .125	199033696R3CA1	SPRAG	1500-73-3602	2
C9	SMD, CAP, CER, 2%, 50V, NPO 100PF	C1206C101J2GAC	KEMET	1500-81-0101	1
C11 C12 C17 C18 C20 C24 C46 C50 C56 C57 C58 C61 C64	CAP, SMD CER +80-20% Z5U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	13

WAVETEK PARTS LIST
TITLE PCA, MEASUREMENT MODULE (50-2)
ASSEMBLY NO. 1100-00-2615
REV L
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
7	ADHESIVE, THERMAL, EPOXY	00241	LKTIT	1600-03-0019	1
2	DRILL DRWG, PCA, CHANNEL BOARD	1700-1811	WVTX	1700-00-1811	1
J1 J2	PC JACK	09-9094-1-04	CONCD	2100-02-0190	2
J6	CONNECTOR, RT ANGLE PC MOUNT, 9 PIN	745394-2	AMP	2100-02-0200	1
TP1	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	1
E1	SPARK GAP	B2-B600	SIEM	2400-05-0046	1
6	JUMPER, .100	J 0.100X0.125 B22	SQIRS	2800-12-0049	1
7	JUMPER, .200	J 0.200X0.125 B22	SQIRS	2800-12-0050	1
4	SCREW, SELF LOCKING, PAN HEAD 4-40X3/16	4-40 X 3/16	CMRCL	2800-23-4103	1
5	PIN SNAPLOCK, NYLON, PERMANENT, 1/8 HOLE	SLP-125.01	RICH	2800-60-0003	2
K1 K4 K5	RELAY, 2 FORMC	DS2E-SL2-DC5V	ARROW	4500-00-0028	3
R5	SMD, ZERO OHM JUMPER, 1/8 BODY LENGTH, 2 AMP	MCR18-JPW	ROHM	4703-20-0000	1

WAVETEK PARTS LIST
TITLE PCA, MEASUREMENT MODULE (50-2)
ASSEMBLY NO. 1100-00-2615
REV L
PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R18 R59 R60 R61 R62 R63 R64 R68	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 10K OHM	MCR18EZH103JW5%	ROHM	4703-20-1035	8
R15 R16 R56 R65	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 100K OHM	MCR18EZH104JW5%	ROHM	4703-20-1045	4
R20	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 22 OHM	MCR18EZH220JW5%	ROHM	4703-20-2205	1
R12 R17 R50 R51 R52 R53 R54 R55	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 2.2K OHM	MCR18EZH222JW5%	ROHM	4703-20-2225	8
R19	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 220K OHM	9C12063A2203JLR	MEPCO	4703-20-2245	1
R47	RES, SMD, GP, 1/8 LONG, 200PPM, 5%, 470	0108-00-2766	WVTK	4703-20-4715	1
R57 R58	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 470K OHM	MCR18EZH474JW5%	ROHM	4703-20-4745	2
R48 R49	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 820 OHM	MCR18EZH821JW5%	ROHM	4703-20-8215	2
RN2	RES NETWORK	1776-8	CADDO	4770-00-0040	1
RN3	RES NETWORK	T1794-180-2	CADDO	4770-00-0041	1

WAVETEK PARTS LIST
TITLE PCA, MEASUREMENT MODULE (50-2)
ASSEMBLY NO. 1100-00-2615
REV L
PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R6	RES, CC, 1W, 10%, 100K	GB1041	AB	4799-00-0092	1
R1 R2	RES, CC, 1/2W, 5%, 51K	EB5131	AB	4799-00-0093	2
W2	RIBBON CABLE ASSEMBLY, 10 PIN, 10"	6002-00-0043	WVTK	6002-00-0043	1
U1	IC, CENTIGRADE TEMP SENSOR	LM35DZ	NAT	7000-00-3500	1
U12	IC, ANALOG PROCESSOR	TSC500L	TELE	7000-05-0000	1
U5	IC, PICOAMP INPUT MIC VOLT OFFSET LOW NOISE	LT1012CN8	LINTE	7000-10-1200	1
U25	IC, POWER SUPPLY	PWR103-1	BUR	7000-10-3100	1
U8 U9	SMD, DARLINGTON TRANSISTOR ARRAY	ULN2004D	SIG	7000-20-0001	2
VR2	REGULATOR, MICROPOWER VOLTAGE, 3 PIN	LP2950ACZ-5.0V	NSC	7000-29-5000	1
U6 U7	MUL/DEMUL, DUAL 4 CHANNEL ANALOG, SMD	HEF4052BTD	SIG	7000-40-5200	2
U26	SMD, DC TO DC CONVERTER, CMOS, 300MW	ICL7660CBA	INTSL	7000-76-6041	1
VR1	IC, VOLTAGE REFERENCE	7003-00-7400	WVTK	7003-00-7400	1

WAVETEK PARTS LIST
TITLE PCA, MEASUREMENT MODULE (50-2)
ASSEMBLY NO. 1100-00-2615
REV L
PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U22 U23	OPTO CPLP, FAST	6N136	SPECT	7100-00-0001	2
U24	IC, DUAL, LOW INPUT, HIGH GAIN OPTOCOUPL	HCLP2730	HP	8000-27-3000	1
U28 U32	FLIP-FLOP, DUAL D, CMOS, SMD	HEF4013BTD	SIG	8000-40-1341	2
U10 U13 U30 U34	REG/LATCH 8-BIT SHIFT CMOS, SMD	HEF4094BTD	SIG	8000-40-9441	4
U27	NAND, QUAD 2INP POS	74HC00D	SIG	8000-74-0041	1
U20	IC, SMD, QUAD 2-INPUT NAND SCHMITT TRIGGER	74HC132D	SIG	8000-74-1320	1
U29	SMD, HEX SCHMITT TRIGGER/INVERTER, HCMOS	74HC14D	SIG	8000-74-1441	1

WAVETEK PARTS LIST
TITLE PCA, MEASUREMENT MODULE (50-2)
ASSEMBLY NO. 1100-00-2615
REV L
PAGE 5

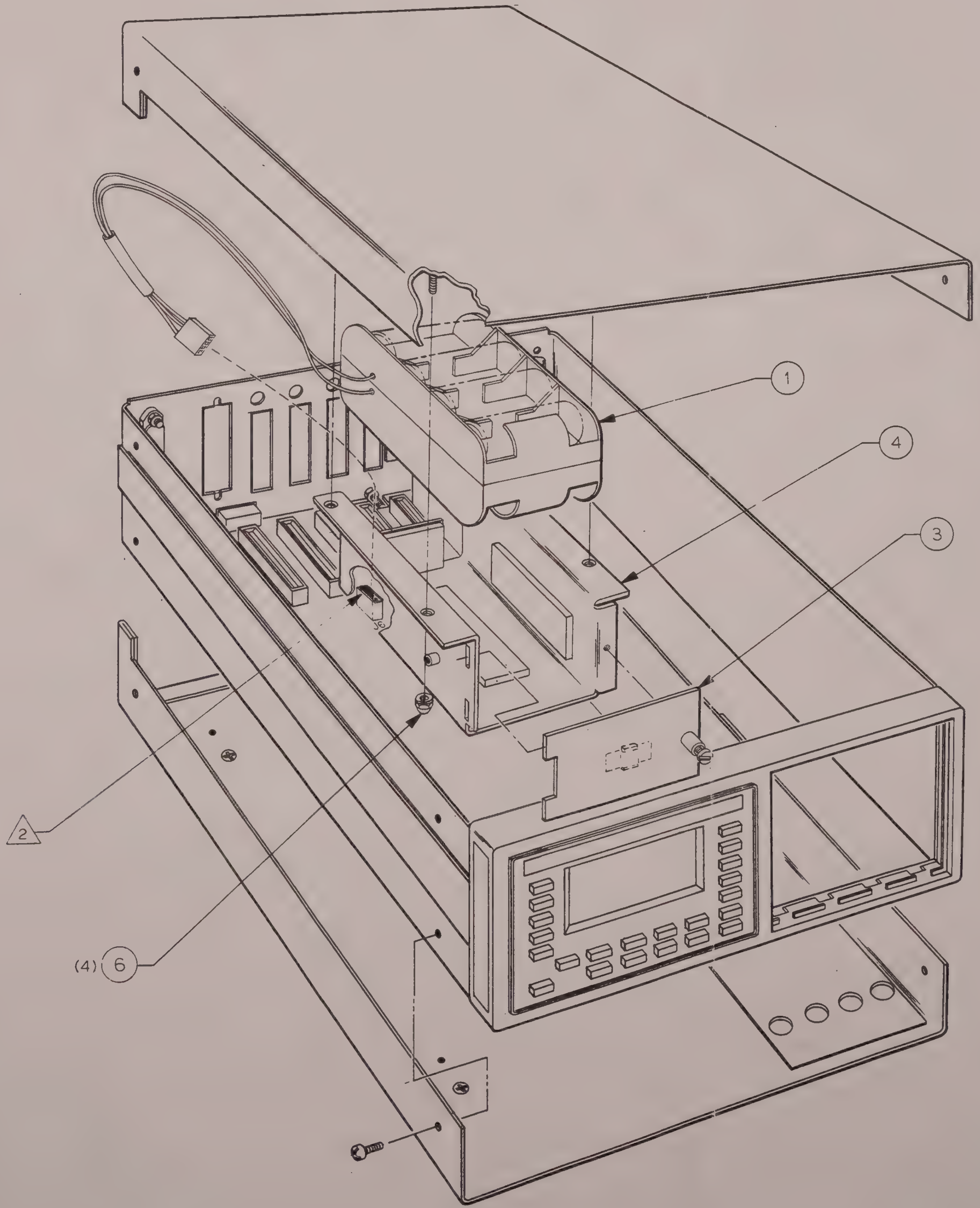
NOTE: UNLESS OTHERWISE SPECIFIED

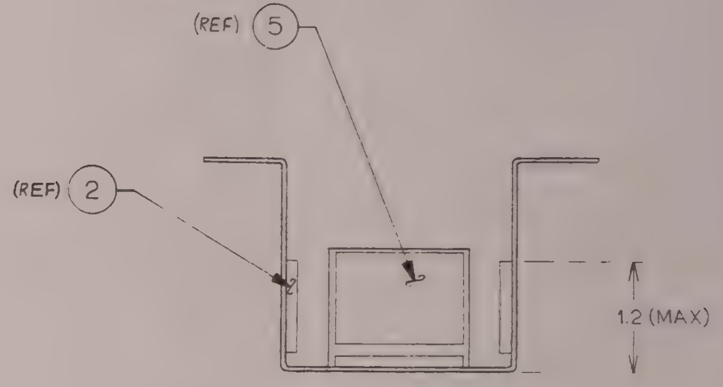
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
MM PC BOARD

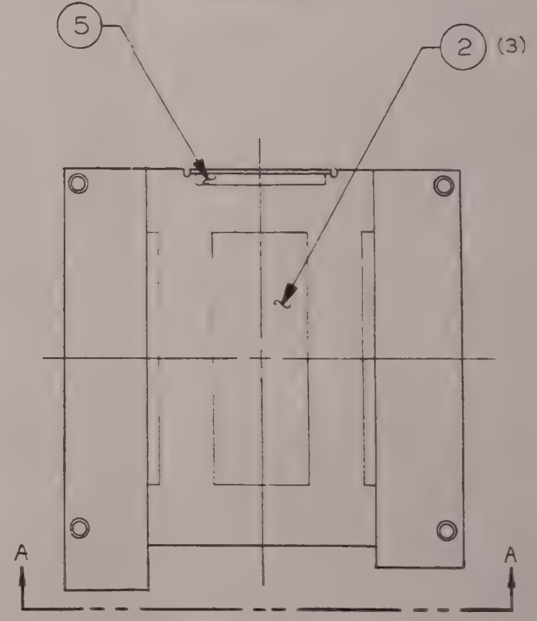
SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-2615
REV L
SCALE
MODEL 50-2
SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE	JT	7/16/86	NM
B	#7751	JT	10/28/86	RKT





VIEW A-A



SUPPORT INSTALLATION
(LOCATE SYMMETRICALLY AS SHOWN)

1000-00-0466 B

2. REMOVE JUMPER P6 (2100-02-0213) FROM J6 PINS 1 & 2 AND TAPE TO BRACKET (ITEM 3)

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0466

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 7/16/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	8/19/86	TITLE ASSEMBLY, PRIMARY CELL BATTERY (OPTION 50-10)
	RELEASE APPROV 8/20/86		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52 — DWG NO. 1000-00-0466 — REV B
	SCALE NONE		CODE IDENT 23338 — SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO [illegible]

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
1	ASSY, BATTERY HOLDER	1207-00-2869	WVTK	1207-00-2869	1
2	SUPPORT, CHANNEL BD. (2.75")	1400-02-1850	WVTK	1400-02-1850	3
5	CUSHION SUPPORT, BATTERY (1.38")	1400-02-1859	WVTK	1400-02-1859	1
3	PANEL, BATTERY BRACKET	1400-02-2153	WVTK	1400-02-2153	1
4	BRACKET, PRIMARY CELL BATTERY	1400-02-2163	WVTK	1400-02-2163	1
6	NUT, FLEXLOCK, CAD I 6-32	6-32 NUT F.L.	CMRCL	2800-15-6100	4

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PRIMARY CELL BATT OPT 50-10	1000-00-0466 PAGE 1	B

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

		DATE
DRAWN		
CHECKED		
PROJ. ENGR.		
RELEASE APPROV.		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

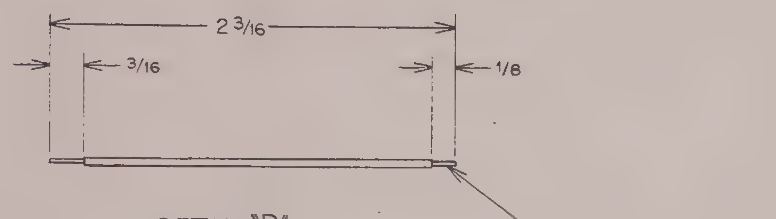
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
Parts List
Primary Battery

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1000-00-0466	B

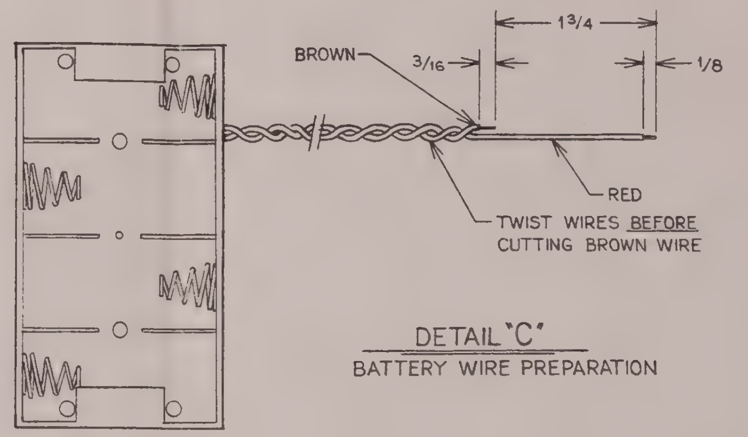
SCALE Option 50-10 SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE	DT	7/23/86	nm

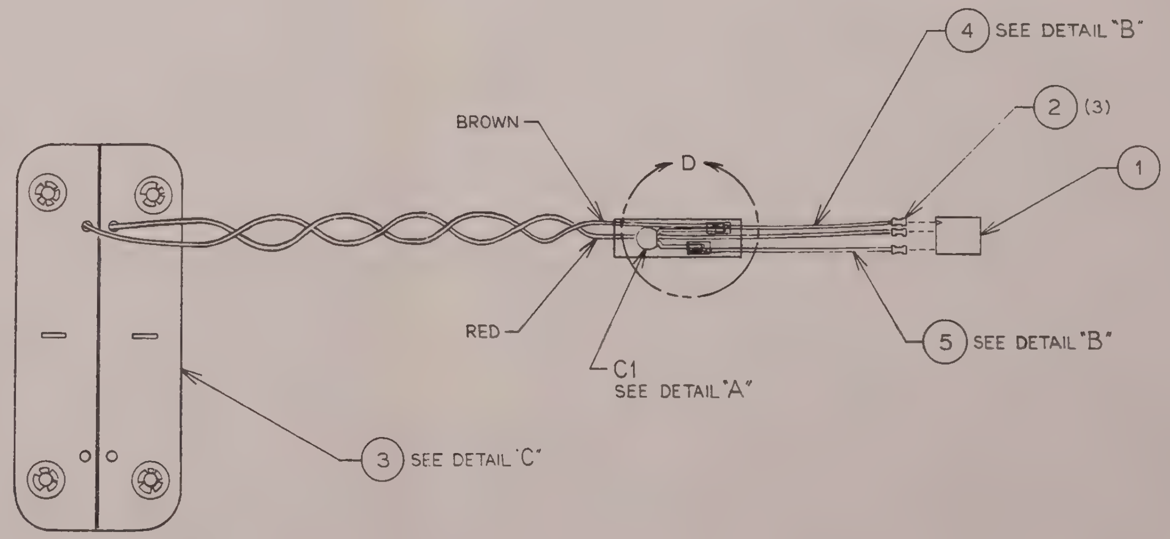


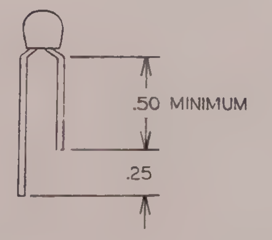
DETAIL "B"
WIRE PREPARATION - ITEMS 4 & 5
(SCALE: 2/1)

THIS END OF WIRE IS FIXED WITH CONNECTOR PINS (ITEM 2)


BROWN
3/16
1 3/4
1/8
RED
TWIST WIRES BEFORE CUTTING BROWN WIRE

DETAIL "C"
BATTERY WIRE PREPARATION

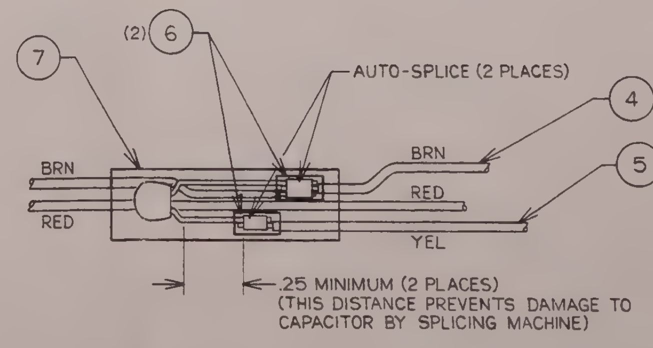

4 SEE DETAIL "B"
2 (3)
1
BROWN
D
RED
C1
SEE DETAIL "A"
5 SEE DETAIL "B"
3 SEE DETAIL "C"


.50 MINIMUM
.25

DETAIL "A"
CAPACITOR PREPARATION
(SCALE: 2/1)

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C1	CAP, CER, MON, .47UF, 20%, 50V, 25U	CRC230Z5U474M050	CORNG	1500-04-7406	1
1	CONN, HOUSING (4 PIN)	102241-2	AMP	2100-02-0129	1
2	PINS, CONN	87667-2	AMP	2100-05-0030	3
3	BATTERY HOLDER	28-1	LZR	4000-04-0001	1
4	WIRE, HU, 22GA	H0101029 (BRN)	JUDD	6000-32-2001	2.188
5	WIRE, HU, 22GA	H0101029 (YEL)	JUDD	6000-32-2004	2.188
6	SHRINK TUBING, 1/8 IN	FIT-221-1/8	ALPHA	6001-20-2000	.5
7	SHRINK TUBING, 3/8 IN	FIT-221-3/8	ALPHA	6001-20-6000	1.25

WAVETEK PARTS LIST	TITLE ASSY, BATTERY HOLDER	ASSEMBLY NO. 1207-00-2869 PAGE 1	REV A


7
(2) 6
AUTO-SPLICE (2 PLACES)
4 (REF)
5 (REF)
BRN
RED
BRN
RED
YEL

.25 MINIMUM (2 PLACES)
(THIS DISTANCE PREVENTS DAMAGE TO CAPACITOR BY SPLICING MACHINE)

DETAIL "D"
(SCALE: 2/1)

1. FRACTIONS ARE ± 1/32.
NOTE UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1207-00-2869

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 7/9/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	8-14-86	TITLE ASSEMBLY, BATTERY HOLDER
	RELEASE APPROV DL Taylor 8/20/86		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52
	SCALE FULL & NOTED		DWG NO. 1207-00-2869
			REV A
			CODE IDENT 23338
			SHEET 1 OF 1

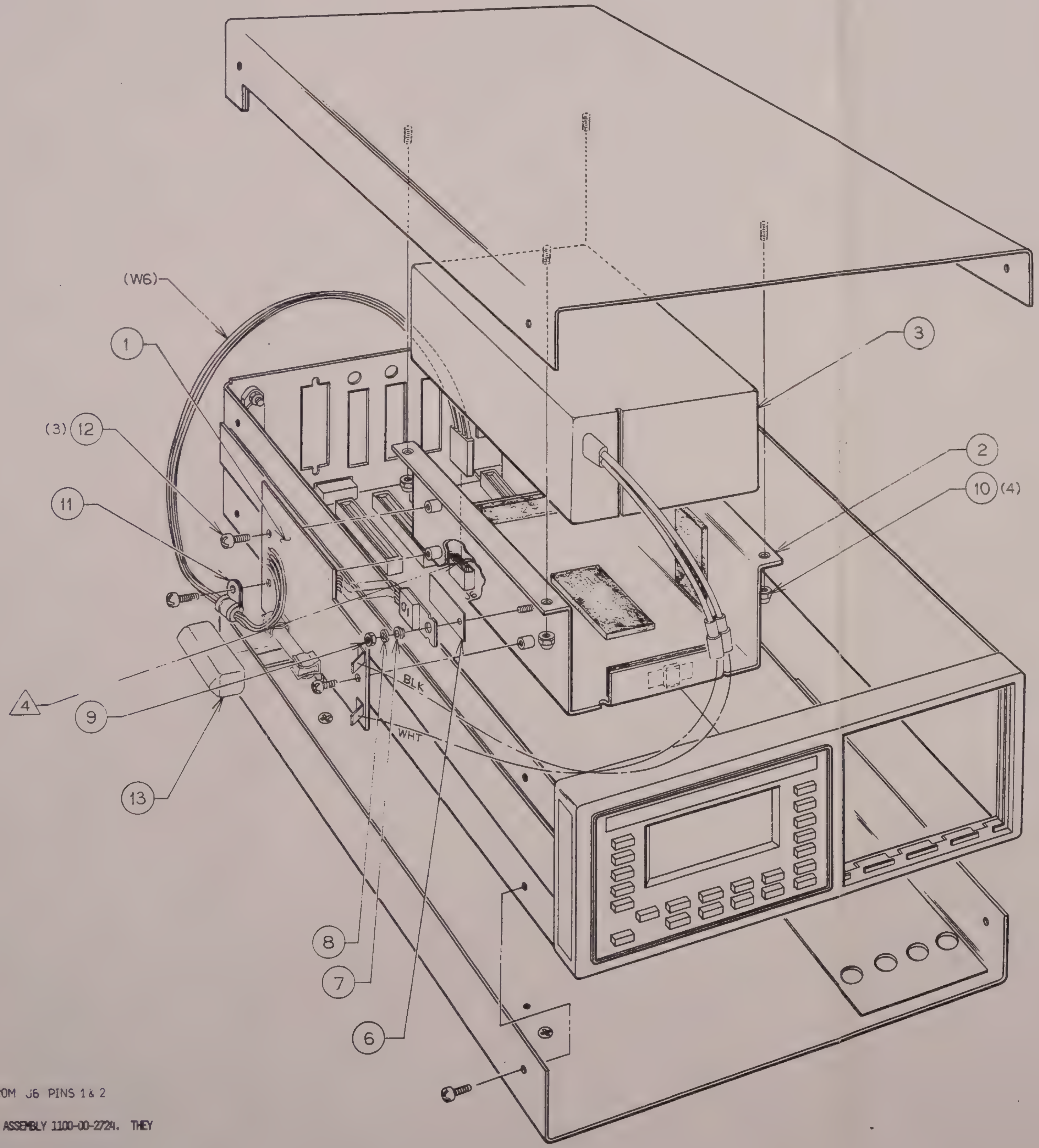
1207-00-2869 A

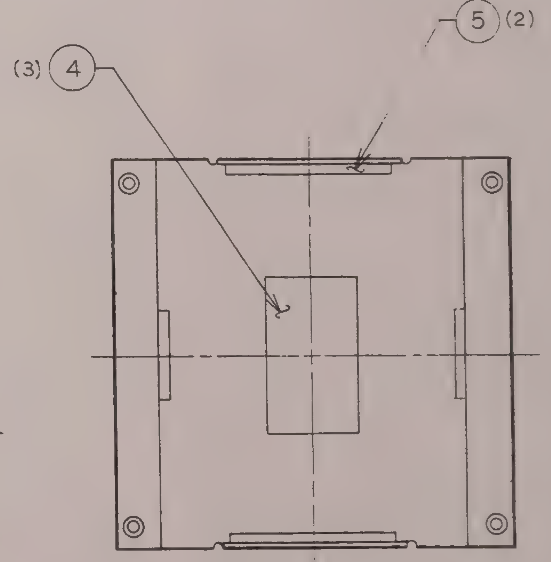
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

REV	ECN	BY	DATE	APP
A	FOR RELEASE	AT	3/25/86	NM
B	7600	AT	7/25/86	
C	775:		8/?/86	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
1	PCA, RECHARGEABLE BATTERY BD	52-2724	WVTK	1100-00-2724	1
3	ASSY, BATTERY	52-2774	WVTK	1200-00-2774	1
2	BRACKET, BATTERY	52-1243	WVTK	1400-02-1243	1
4	CUSHION SUPPORT, BATTERY (1.00 WIDE)	1400-02-1860	WVTK	1400-02-1860	3
5	CUSHION SUPPORT, BATTERY (.50 WIDE)	1400-02-1870	WVTK	1400-02-1870	2
7	WASHER	B31347F015	MOT	2800-11-0015	1
9	NUT, HEX, 4-40	MS35649-244	COML	2800-14-4100	1
10	NUT, FLEXLOCK, CAD I 6-32	6-32 NUT F.L.	CMRCL	2800-15-6100	4
12	SCREW, PAN, CAD I, CROSS RECESS.	MS51957-13	COML	2800-38-4104	3
8	WASHER, SPLIT LOCK, 4	04SSLW	CMRCL	2800-42-4000	1
11	CABLE CLAMP	F2WY-125MA	BRADY	3000-00-0157	1
6	INSULATOR(TO-220)	60-11-8302-1674	CHOMR	3100-00-0010	1
13	FUSE COVER FOR 0.25X1.25 FUSE	840836	RICH	3100-00-0015	1

WAVETEK PARTS LIST	TITLE RECHARGEABLE BATT OPT 50-11	ASSEMBLY NO 1000-00-0467 PAGE 1	REV C





SUPPORT INSTALLATION
(LOCATE SYMMETRICALLY AS SHOWN)

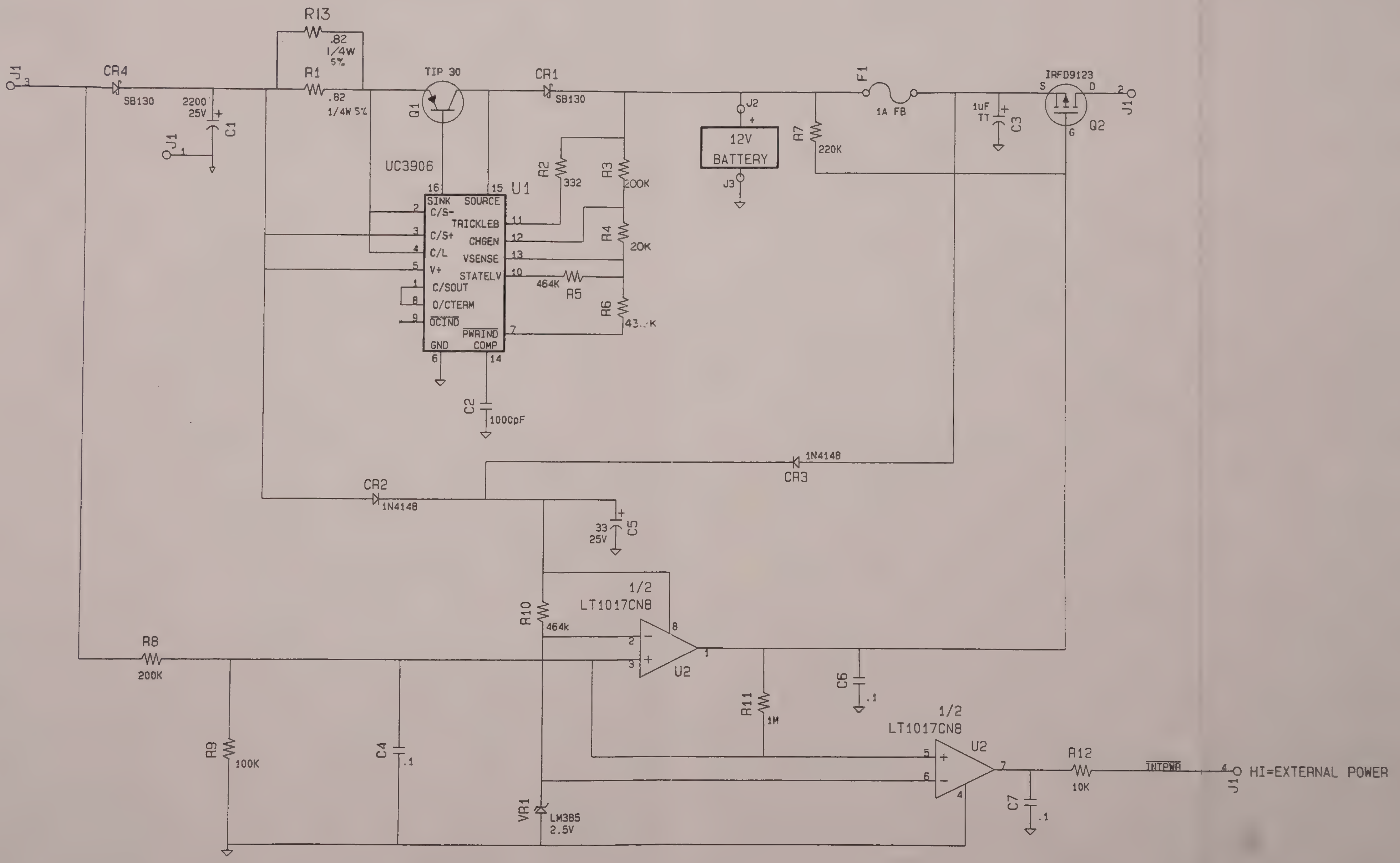
4. REMOVE JUMPER P6 (2100-02-0213) FROM J6 PINS 1 & 2 AND TAPE TO BRACKET (ITEM 2).
3. W6 AND Q1 ARE PART OF BATTERY OPTION BOARD ASSEMBLY 1100-00-2724. THEY ARE NOTED FOR REFERENCE ONLY.
2. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0467

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3/24/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR N. S. Miller	5/5/86	TITLE ASSEMBLY, RECHARGEABLE BATTERY (OPTION 50-11)
	RELEASE APPROV W. Taylor		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52 · DWG NO. 1000-00-0467 · REV C
	SCALE NONE		CODE IDENT 23338 · SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE	JT	4/29/85	N.J.J.
B	7484	JT	6/13/86	A.P.
C	7963	JT	2/5/87	L.C.
D	9021	MAT	9/15/87	HJ


R13
.82
1/4W
5%
R1
.82
1/4W 5%
J1
3
CR4
SB130
2200
25V
+
C1
J1
1
TIP 30
Q1
CR1
SB130
J2
+
12V
BATTERY
J3
R7
220K
F1
1A FB
1uF
TT
+
C3
IRFD9123
S
D
2
J1
6
Q2
UC3906
16
15
U1
SINK
SOURCE
2
C/S-
TRICKLEB
11
3
C/S+
CHGEN
12
4
C/L
VSENSE
13
5
V+
STATELV
10
1
C/SOUT
8
O/CTERM
9
OCIND
PWRIND
7
GND
COMP
6
14
R2
332
R3
200K
R4
20K
464K
R5
R6
43.[illegible]K
C2
1000pF
1N4148
CR3
CR2
1N4148
33
25V
+
C5
1/2
LT1017CN8
R10
464k
8
2
3
1
U2
R8
200K
R11
1M
C6
.1
R9
100K
C4
.1
1/2
LT1017CN8
U2
5
6
7
4
+
-
R12
10K
INTPWR
4
J1
HI=EXTERNAL POWER
C7
.1
VR1
LM385
2.5V

3. RESISTORS VALUED IN OHMS, 1/8W, 1%.
2. CAPACITORS VALUED IN MICROFARADS (uF).
1. FOR UNIT INTECONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

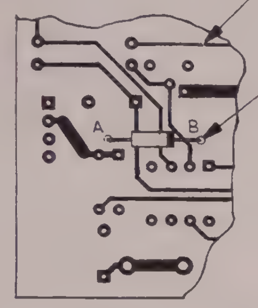
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TARR	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR C.SEAGRAVE		TITLE SCHEMATIC, BATTERY BOARD
	RELEASE APPROV D.R.TAYLOR		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52 · DWG NO. 0103-00-2724 · REV D
	SCALE NONE		CODE IDENT 23338 · SHEET 1 OF 1

0103-00-2724 D

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

REV	ECN	BY	DATE	APP
A	FOR PELEASE	A.T.	4/28/86	nm
B	7484	[illegible]	6/18/86	C.R.T.
C	7963	[illegible]	2/5/87	C.R.T.
D	8096	N.C. 3-12-87	3-12-87	Q.R.T.
E	9021	MAG	9/15/87	H N

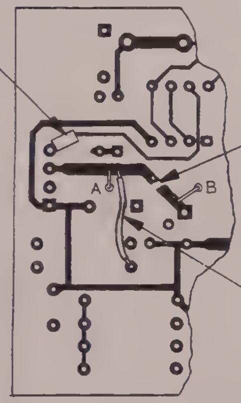


CUT TRACE

DRILL TWO HOLES (#60). INSTALL DIODE (SB130). BEND LEADS AND SOLDER ON CIRCUIT SIDE.

COMPONENT SIDE

CUT TRACE AS SHOWN. SOLDER R12 (SMD 10K RESISTOR) TO PAD AND TO TRACE AS SHOWN. USE RTV TO KEEP R12 IN PLACE.



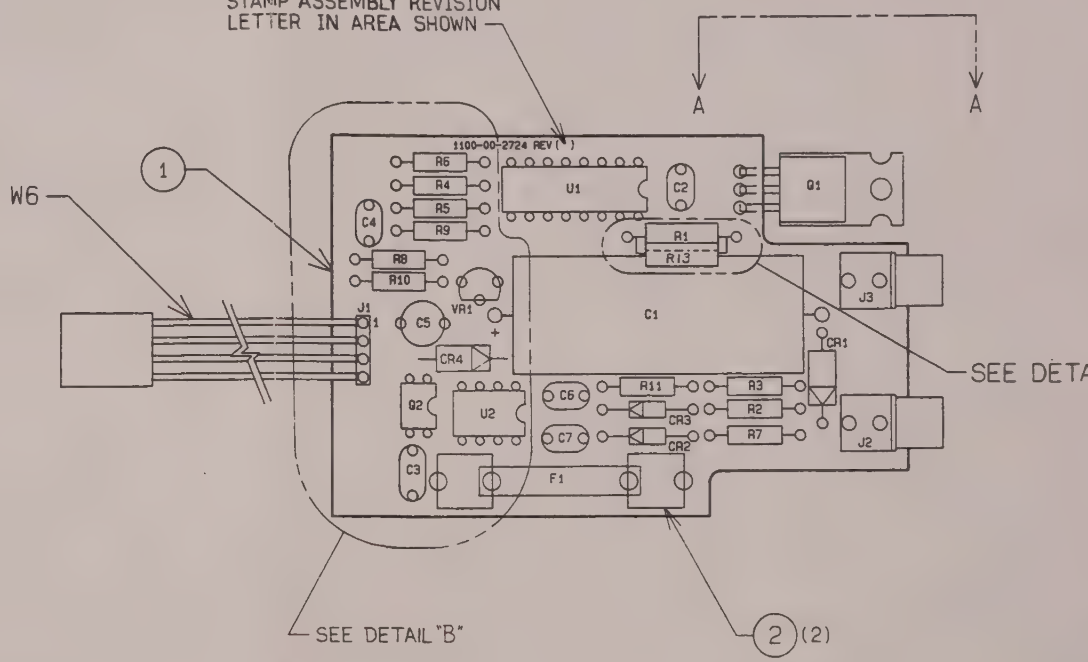
CUT TRACE AND SOLDER CR14 DIODE LEADS FROM HOLES A AND B TO TRACES AS SHOWN.

SOLDER BOTH ENDS OF A 30 GA. INSULATED WIRE TO TRACES AS SHOWN.

CIRCUIT SIDE

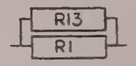
DETAIL "B"

STAMP ASSEMBLY REVISION LETTER IN AREA SHOWN


W6
①
A
A
1100-00-2724 REV( )
R6
R4
R5
R9
C4
R8
R10
U1
C2
Q1
R1
R13
VR1
J1
1
C5
+
C1
CR4
CR1
J3
Q2
U2
C6
C7
R11
CR3
CR2
R3
R2
R7
J2
C3
F1
② (2)

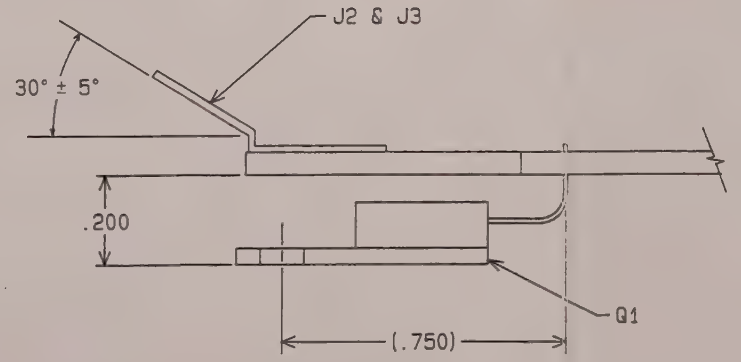
SEE DETAIL "C"

SEE DETAIL "B"



DETAIL "C"

CONNECT R13 (.8 Ω 1/4W) PARALLELY ACROSS R1 ON COMPONENT SIDE AND SOLDER.


J2 & J3
30° ± 5°
.200
Q1
(.750)

VIEW A-A

(SCALE: 4/1)
(ROTATED 180°)

2. SEE 0103-00-2724 FOR SCHEMATIC.

1. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1100-00-2724

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.T.	DATE 4/28/86	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL —‡—	PROJ ENGR C. [illegible]	6-5-86	TITLE PCA, RECHARGEABLE BATTERY BOARD	
	RELEASE APPROV [illegible]			
FINISH WAVETEK PROCESS —‡—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030			
	DO NOT SCALE DWG		MODEL NO. 51/52	DWG NO 1100-00-2724
	SCALE 2/1 & NOTED		CODE IDENT 23338	SHEET 1 OF 1

REV E

1100-00-2724 E

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A2798

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC BATTERY CHARGER BOARD	0103-00-2724	WVTK	0103-00-2724	1
W6	ASSY, BATTERY CHARGER CABLE	52-2773	WVTK	1207-00-2773	1
C2	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-0211	1
C4 C6 C7	CAP CER MON 1MF 50V Z5U +80/-20% RAD LD SP .2	SR215E104ZAA	AVX	1500-01-0420	3
C1	CAP, ELECT, AXIAL, 2200UF, 20%, 25V	NAE2200M25V	NIC	1500-32-2203	1
C5	CAP ELECT, END MOUNT, 0.1 LEAD SPACE 33UF, 20%	ULB1E330M	NICH	1500-33-3003	1
C3	CAP, TANT, 1MF, 35V	196D105X0035HA1	SPRAG	1500-71-0512	1
1	PCB RCH BATT OPT 50-11	52-2724	WVTK	1700-00-2724	1
J2 J3	TERMINAL TAB (FASTON)	62747-1	AMP	2100-04-0038	2
F1	FUSE, 1A, 250V	312001	LITFU	2400-05-0007	1
2 3	FUSE HOLDER, CLIP	102071	LITFU	2400-05-0031	2
R9	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	1
R11	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	1

WAVETEK PARTS LIST	TITLE PCA, RECHARGEABLE BATTERY BD	ASSEMBLY NO. 1100-00-2724 PAGE 1	REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U1	BATTERY CHARGER, FOR SEALED LEAD ACID 0-70	UC3906N	UNITR	7000-39-0601	1

WAVETEK PARTS LIST	TITLE PCA, RECHARGEABLE BATTERY BD	ASSEMBLY NO. 1100-00-2724 PAGE 3	REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R4	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	1
R3 R8	RES, MF, 1/8W, 1%, 200K	RN55D-2003F	MEPCO	4701-03-2003	2
R7	RES, MF, 1/8W, 1%, 221K	RN55D-2213F	TRW	4701-03-2213	1
R2	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	1
R6	RES, MF, 1/8W, 1%, 43.2K	RN55D-4322F	TRW	4701-03-4322	1
R10 R5	RESISTOR, METAL FILM, RN55 SIZE 464K, 1%,	5043ED4643F	MEPCO	4701-03-4643	2
R1 R13	RES FIXED VALUE, METAL FILM, RN50 SIZE	5063JDR8200J	MEPCO	4701-05-0828	2
R12	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 10K OHM	MCR18EZH103JW5%	ROHM	4703-20-1035	1
CR1 CR4	DIODE, STTKY	SB130	GI	4806-02-0130	2
CR2 CR3	DIODE	1N4148	FAIR	4807-02-6666	2
Q1	TRANS	TIP-30	TI	4902-00-0300	1
Q2	TRANSISTOR	IRFD9123	IR	4902-09-1230	1
VR1	IC, MIC POWER VOLT REF	LM385BZ-2.5	LINTE	7000-03-8500	1
U2	DUAL COMPARITOR, MICROPOWER, 8-PIN DIP	LT1017CN8	LINTE	7000-10-1701	1

WAVETEK PARTS LIST	TITLE PCA, RECHARGEABLE BATTERY BD	ASSEMBLY NO. 1100-00-2724 PAGE 2	REV E

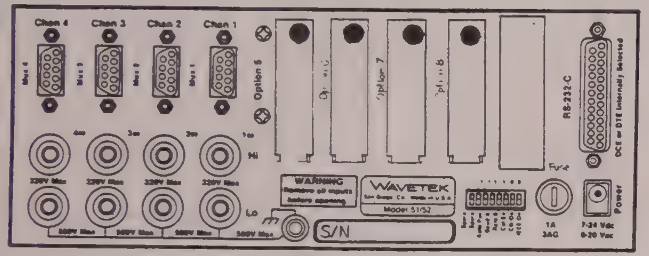
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE PARTS LIST RECHARGE BATTERY
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-2724 · REV E
DO NOT SCALE DRAWING			SCALE Option 50-11 · SHEET 1 OF 1

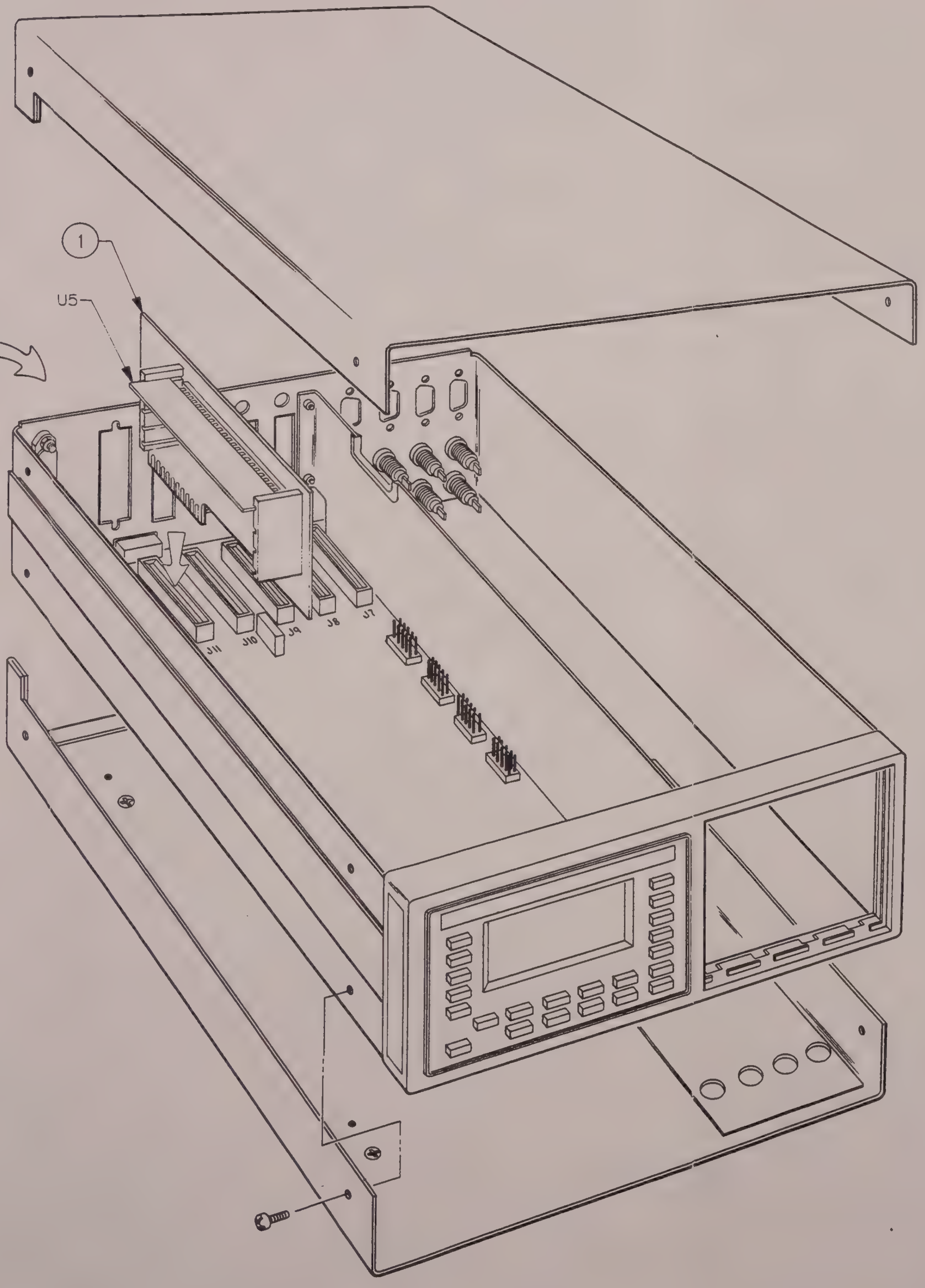
REV	ECN	BY	DATE	APP
A	FOR RELEASE			
B	7600	JT		

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT ✓ 52	0004-00-0440	WVTK	0004-00-0440	1
1	PCA, RAM BD	52-1817	WVTK	1100-00-1817	1
U5	IC, 64KBYTE HYBRID MEMORY, LSI, 38-DECODER 32	[redacted]	S-MOS	8000-22-0001	1

WAVETEK PARTS LIST	TITLE RAM EXPAN BD OPT 50-12-64K	ASSEMBLY NO. 1000-00-0468 PAGE 1	REV B


Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 7
RS-232-C
DCE or DTE Internally Selected
WARNING
WAVETEK
Model 51/52
S/N
Fuse
1A
3AG
Power
7-24 Vdc
6-20 Vac
Lo

SAMPLE REAR PANEL CONFIGURATION


1
U5
J11
J10
J9
J8
J7

3. RAM EXPANSION BOARD ASSEMBLY (OPTION 50-12-64) MAY BE INSTALLED IN EITHER J7 (REAR PANEL OPTION 5), J8, (REAR PANEL OPTION 6), J9 (REAR PANEL OPTION 7), J10 (REAR PANEL OPTION 8), OR J11. SPECIFIC SLOT IS DEPENDENT UPON TOTAL INSTRUMENT CONFIGURATION. RAM ASSEMBLY PHYSICALLY TAKES TWO SLOTS; I.E. WHEN INSTALLED IN J7, NO OTHER OPTION MAY BE INSTALLED IN J8, AND WHEN INSTALLED IN J9, NO OTHER OPTION MAY BE INSTALLED IN J10, ETC.
2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0468

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN D. COOPER
DATE 3/13/86
PROJ ENGR 3/15/86
RELEASE APPROV 3/19/86
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1
.XX ±.030
DO NOT SCALE DWG
SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
ASSEMBLY, RAM
EXPANSION BOARD
OPTION 50-12-64K

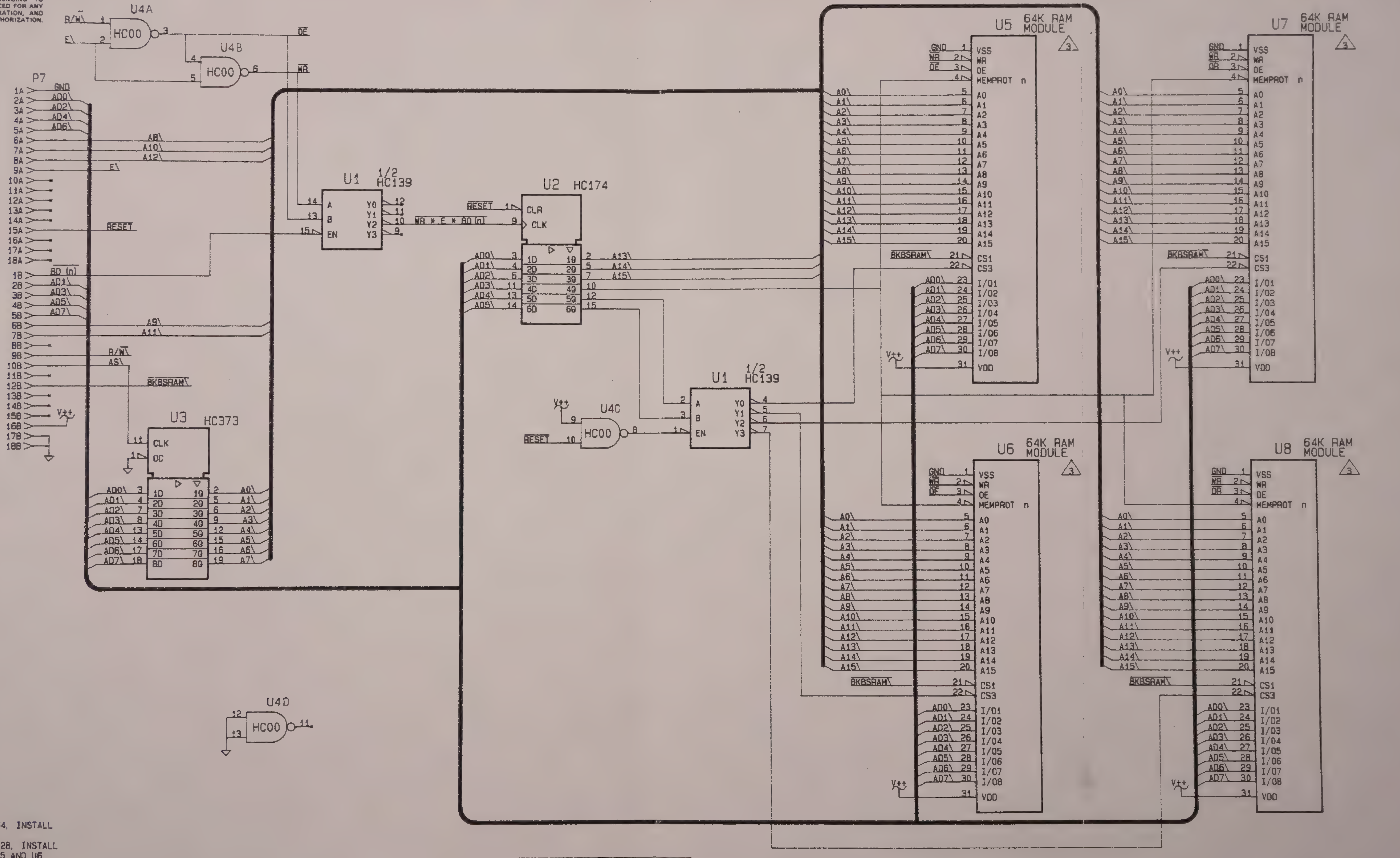
MODEL NO 51/52
DWG NO. 1000-00-0468
REV B
CODE IDENT 23338
SHEET 1 OF 1

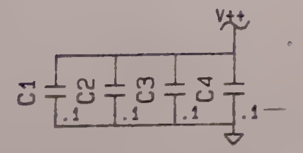
1000-00-0468 B

BISHOP GRAPHICS/ACCUPRESS

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP
A	FOR RELEASE			


U4A HC00
U4B HC00
U4C HC00
U4D HC00
P7
U1 1/2 HC139
U2 HC174
U3 HC373
U5 64K RAM MODULE
U6 64K RAM MODULE
U7 64K RAM MODULE
U8 64K RAM MODULE
R/W\
E\
OE
WR
RESET
BKBSRAM\
WR * E * BD (n)
BD (n)
AS\
V++
GND
VSS
MEMPROT n
CS1
CS3
VDD
CLR
CLK
OC
EN
A0\–A15\
AD0\–AD7\
I/01–I/08


V++
C1 .1
C2 .1
C3 .1
C4 .1
.1

POWER & GROUND TABLE		
REFERENCE DES.	PIN NUMBER V++	GND
U1	16	8
U2	16	8
U3	20	10
U4	14	7

3. FOR OPTION #50-12-64, INSTALL 64K RAM MODULE U5.
FOR OPTION #50-12-128, INSTALL 64K RAM MODULES U5 AND U6.
FOR OPTION #50-12-192, INSTALL 64K RAM MODULES U5, U6 AND U7.
FOR OPTION #50-12-256, INSTALL 64K RAM MODULES U5, U6, U7 AND U8.
(REFERENCE WAVETEK P/N 8000-22-0001)

2. CAPACITORS VALUED IN MICROFARADS (uF).

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0400.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN
DATE
PROJ ENGR
RELEASE APPROV 3/10/86
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

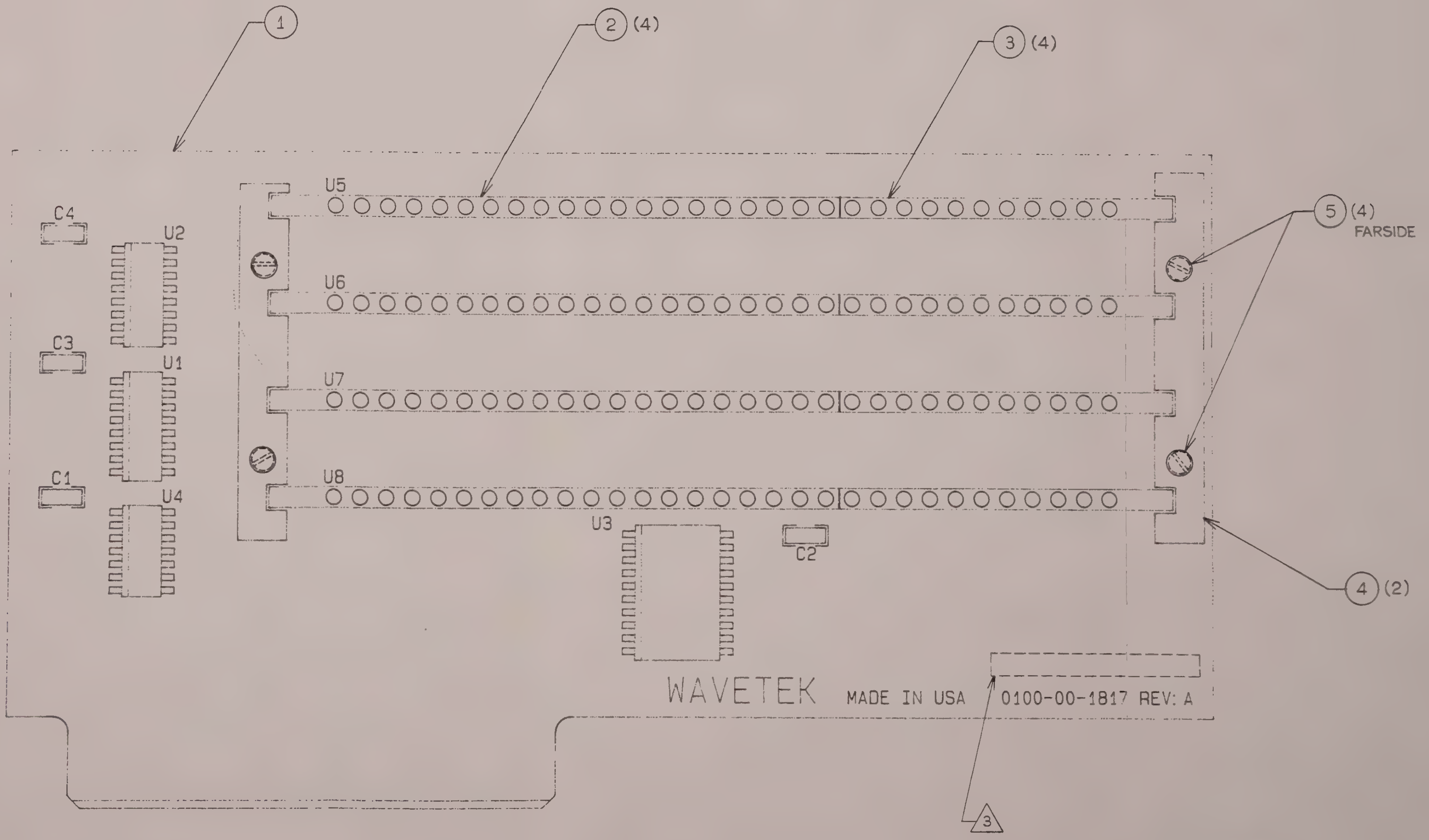
TITLE
SCHEMATIC,
RAM BOARD

MODEL NO. 51/52
DWG NO. 0103-00-1817
REV A
CODE IDENT 23338
SHEET 1 OF 1

0103-00-1817 A

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A27086

REV	ECN	BY	DATE	APP
A	FOR RELEASE	AT	2/.. 96	



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
4	CARD GUIDE, RAM MODULE	1400-02-1600	WVTK	1400-02-1600	2
C1 C2 C3 C4	CAP. SMD CER +80-20% Z5U 50V 0 1MF	C1206C104Z5UAC	KEMET	1500-81-0401	4
1	PCB, RAM BD	1700-1817	WVTK	1700-00-1817	1
2	HEADER, CONN(20 PIN)	643119-1	AMP	2100-02-0131	4
3	SIP STRIP RECEPTACLE, 11 PIN, 0 1 SPACE	643111-1	AMP	2100-02-0206	4
5	SCREW, PAN, SLOTED, TYPE B, 2 X 1/4	2 X 1/4 PAN	CMRCL	2800-22-2104	4
U4	NAND, QUAD 2INP POS	74HC00D	SIG	8000-74-0041	1
U1	SMD, IC, DUAL 2-TO-4 DECODER DEMUX	74HC139D	SIG	8007-41-3941	1
U2	SMD, HEX D-FLIP FLOP, RESET, HCMOS	74HC174D	SIG	8007-41-7441	1
U3	SMD, OCTAL, D-TRANSPARENT LATCH, TRISTATE, HCMOS	74HC373D	SIG	8007-43-7341	1

WAVETEK PARTS LIST	TITLE PCA, RAM BD	ASSEMBLY NO. 1100-00-1817	REV A

PAGE 1

△3 MARK ASSEMBLY NUMBER AND ASSEMBLY REVISION LETTER IN AREA SHOWN.

2. SEE 0103-00-1817 FOR SCHEMATIC.

1. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1100-00-1817

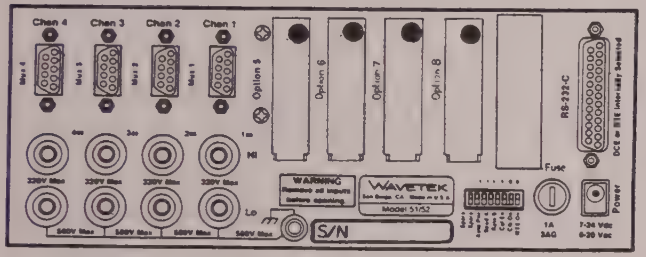
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN O. Tarr	DATE 3/10/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR N. S. Miller	3/10/86	TITLE PCA, RAM BOARD
	RELEASE APPROV R. Taylor 3/10/86		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52 · DWG NO. 1100-00-1817 · REV A
	SCALE 4/1		CODE IDENT 23338 · SHEET 1 OF 1

1100-00-1817 A

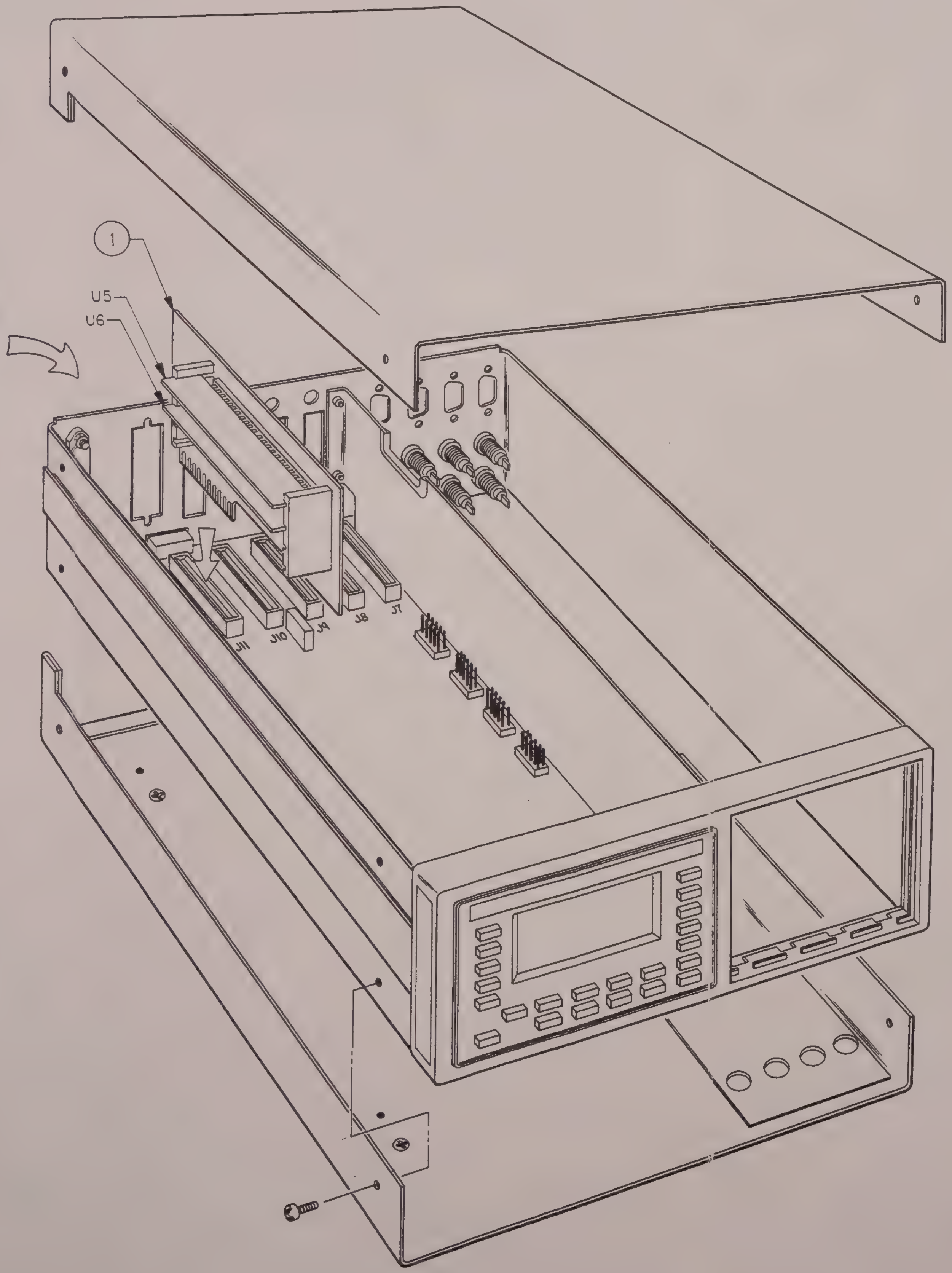
REV	ECN	BY	DATE	APP
A	FOR RELEASE	DT	3/10/86	[illegible]
B	7600	JT	7-9-86	RFT

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
1	PCA, RAM BD	52-1817	WVTK	1100-00-1817	1
U5 U6	IC, 64KBYTE HYBRID MEMORY, LSI, 38-DECODER 32	SHB2200808	S-MOS	8000-22-0001	2

WAVETEK PARTS LIST	TITLE RAM EXPAN BD OPT 50-12-128K	ASSEMBLY NO. 1000-00-0469 PAGE 1	REV B



SAMPLE REAR PANEL CONFIGURATION



3. RAM EXPANSION BOARD ASSEMBLY (OPTION 50-12-128) MAY BE INSTALLED IN EITHER J7 (REAR PANEL OPTION 5), J8, (REAR PANEL OPTION 6), J9 (REAR PANEL OPTION 7), J10 (REAR PANEL OPTION 8), OR J11. SPECIFIC SLOT IS DEPENDENT UPON TOTAL INSTRUMENT CONFIGURATION. RAM ASSEMBLY PHYSICALLY TAKES TWO SLOTS: I.E., WHEN INSTALLED IN J7, NO OTHER OPTION MAY BE INSTALLED IN J8, AND WHEN INSTALLED IN J9, NO OTHER OPTION MAY BE INSTALLED IN J10, ETC.
2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

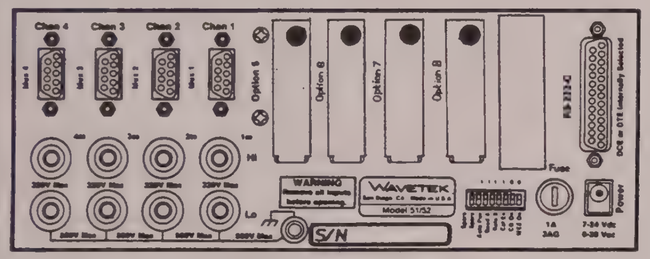
SEE SEPARATE PARTS LIST 1000-00-0469

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3/13/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —/—	PROJ ENGR DL Taylor	3/19/86	TITLE ASSEMBLY, RAM EXPANSION BOARD OPTION 50-12-128K
	RELEASE APPROV DL Taylor	3/19/86	
FINISH WAVETEK PROCESS —/—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO 51/52
	SCALE NONE		DWG NO. 1000-00-0469 REV B
			CODE IDENT 23338 SHEET 1 OF 1

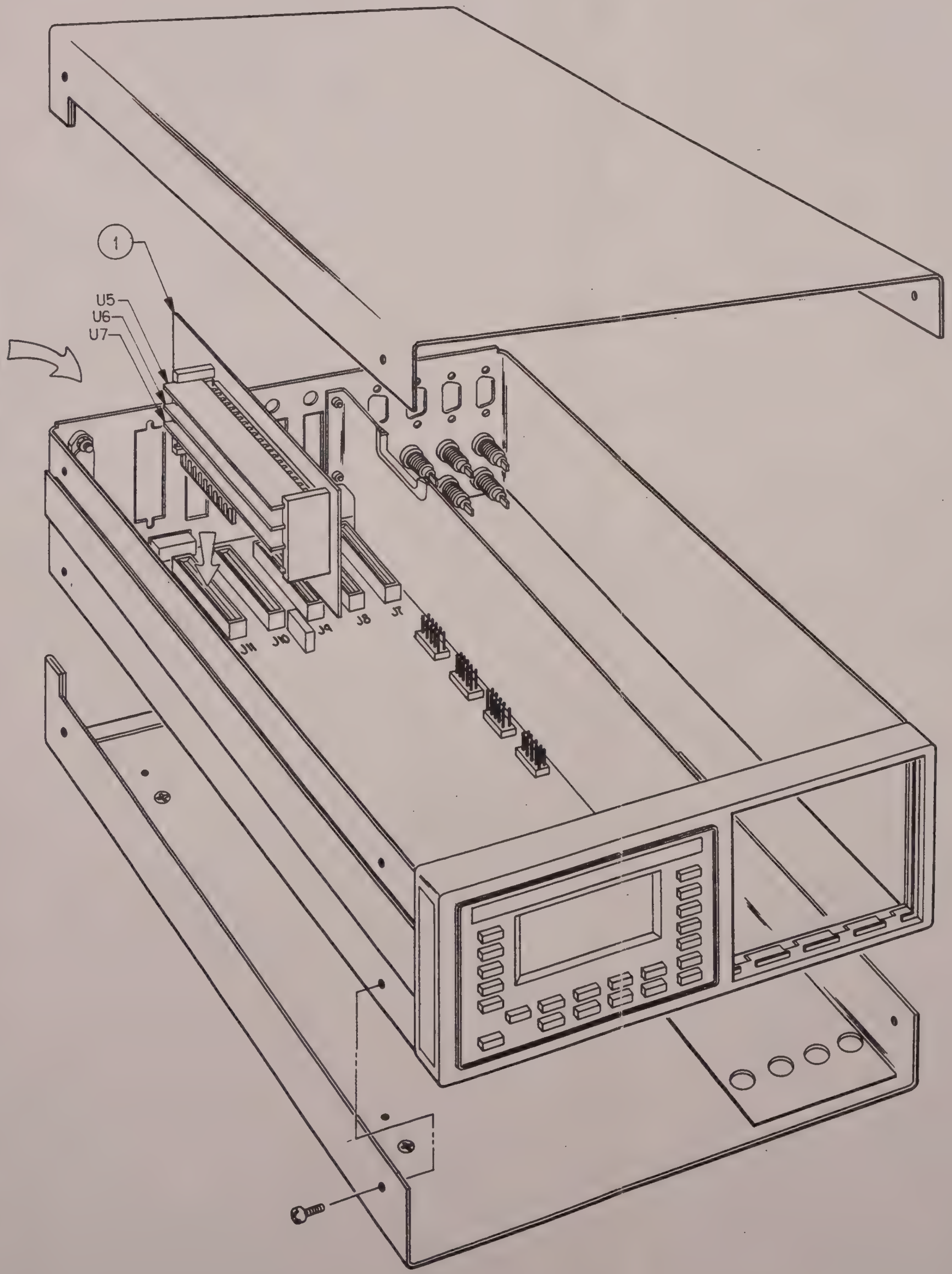
REV	ECN	BY	DATE	APP
A	FOR RELEASE			
B	7600		7/29/86	A.R.T.

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT-32	0004-00-0440	WVTK	0004-00-0440	1
1	PCA, RAM BD	32-1817	WVTK	1100-00-1817	1
U5 U6 U7	IC, 64KBYTE HYBRID MEMORY, LSI, 38-DECODER 32	SMS2200808	S-MOS	8000-22-0001	3

WAVETEK PARTS LIST	TITLE RAM EXPAN BD OPT 50-12-192K	ASSEMBLY NO. 1000-00-0470 PAGE 1	REV B


Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS-232-C
DCE or DTE Internally Selected
Hi
Lo
WARNING
Remove all inputs before opening.
WAVETEK
Model 51/52
S/N
Fuse
1A
3AG
Power
7-34 Vdc
6-30 Vac

SAMPLE REAR PANEL CONFIGURATION


1
U5
U6
U7
J11
J10
J9
J8
J7

3. RAM EXPANSION BOARD ASSEMBLY OPTION 50-12-192 MAY BE INSTALLED IN EITHER J7 (REAR PANEL OPTION 5), J8 (REAR PANEL OPTION 6), J9 (REAR PANEL OPTION 7), J10 (REAR PANEL OPTION 8), OR J11. SPECIFIC SLOT IS DEPENDENT UPON TOTAL INSTRUMENT CONFIGURATION. RAM ASSEMBLY PHYSICALLY TAKES TWO SLOTS; I.E. WHEN INSTALLED IN J7, NO OTHER OPTION MAY BE INSTALLED IN J8, AND WHEN INSTALLED IN J9, NO OTHER OPTION MAY BE INSTALLED IN J10, ETC.
2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0471

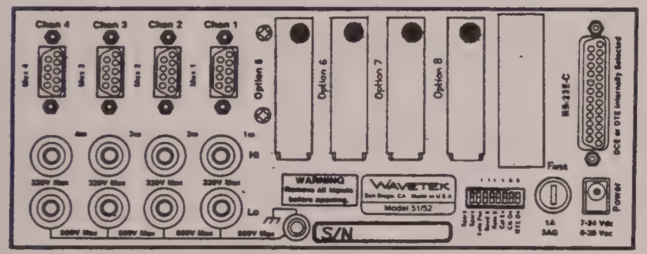
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3/13/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —‖—	PROJ ENGR	3/19/86	TITLE ASSEMBLY, RAM EXPANSION BOARD OPTION 50-12-192K
	RELEASE APPROV 3/19/86		
FINISH WAVETEK PROCESS —‖—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52 · DWG NO. 1000-00-0470 · REV B
	SCALE NONE		CODE IDENT 23338 · SHEET 1 OF 1

1000-00-0470 B

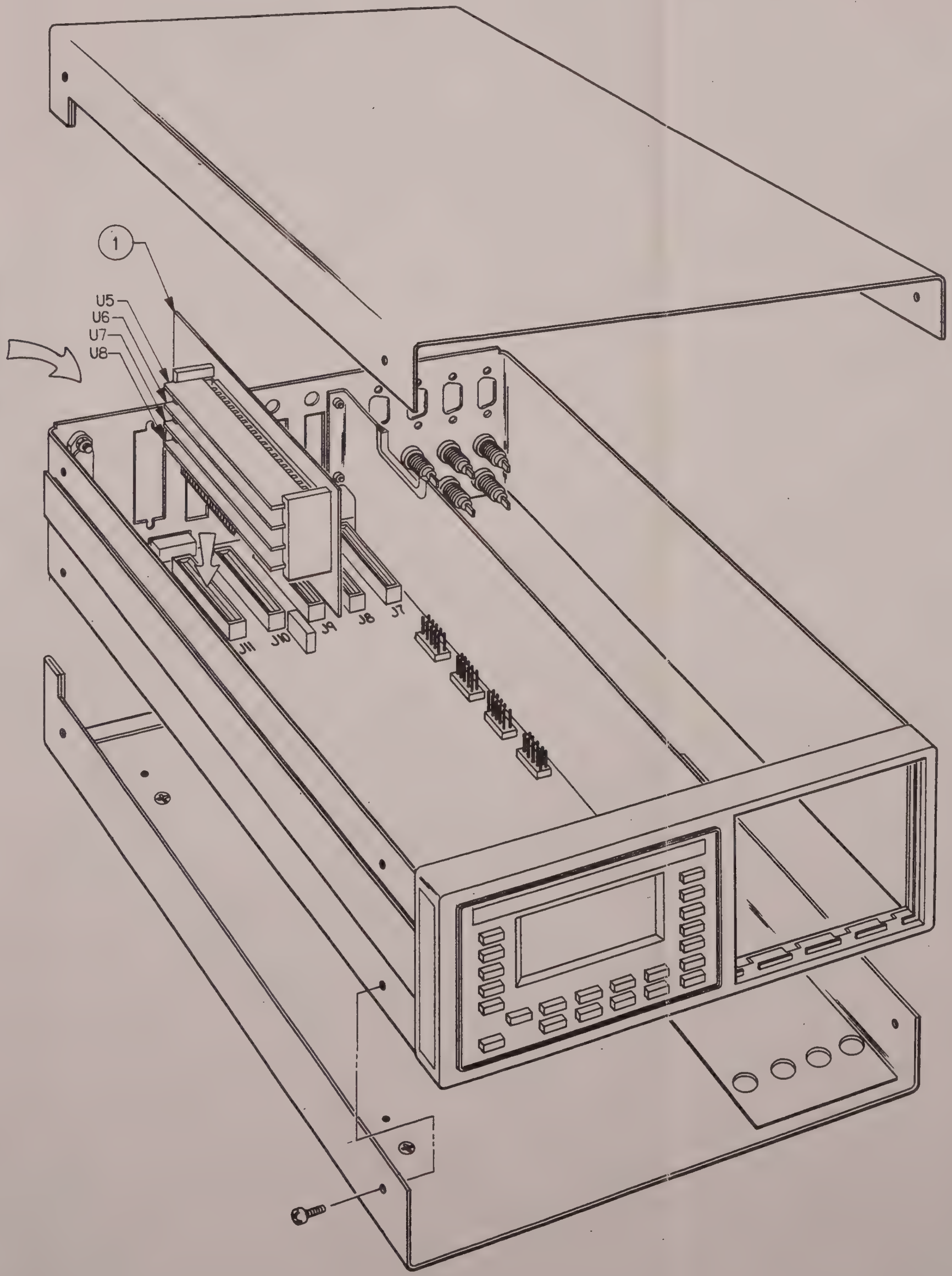
REV	ECN	BY	DATE	APP
A	FOR RELEASE	DT	3/19/86	DM
B	7600	DT	7/29/86	R.R.T.

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
1	PCA, RAM BD	52-1817	WVTK	1100-00-1817	1
U5 U6 U7 U8	IC, 64KBYTE HYBRID MEMORY, LSI, 38-DECODER 32	SHB2200808	S-MOS	8000-22-0001	4

WAVETEK
PARTS LIST
TITLE RAM EXPAN BD OPT 50-12-256K
ASSEMBLY NO. 1000-00-0471
REV B
PAGE 1


Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS-232-C
DCE or DTE Internally Selected
Hi
Lo
WARNING
WAVETEK
Model 51/52
S/N
Fuse
1A
3AG
Power
7-34 Vdc
6-25 Vdc

SAMPLE REAR PANEL CONFIGURATION


1
U5
U6
U7
U8
J11
J10
J9
J8
J7

3. RAM EXPANSION BOARD ASSEMBLY (OPTION 50-12-256)MAY BE INSTALLED IN EITHER J7 (REAR PANEL OPTION 5), J8 (REAR PANEL OPTION 6), J9 (REAR PANEL OPTION 7), J10 (REAR PANEL OPTION 8) OR J11. SPECIFIC SLOT IS DEPENDENT UPON TOTAL INSTRUMENT CONFIGURATION. RAM ASSEMBLY PHYSICALLY TAKES TWO SLOTS; I.E., WHEN INSTALLED IN J7, NO OTHER OPTION MAY BE INSTALLED IN J8 AND WHEN INSTALLED IN J9, NO OTHER OPTION MAY BE INSTALLED IN J10,ETC.

2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

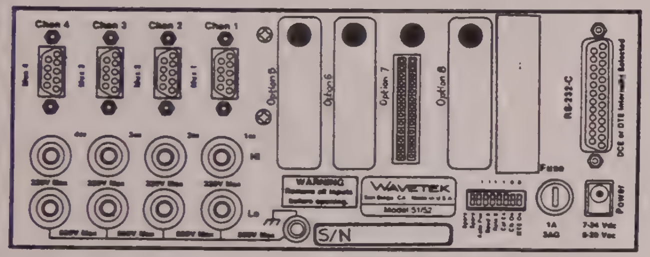
SEE SEPARATE PARTS LIST 1000-00-0471

REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN D. COOPER
DATE 3/13/86
PROJ ENGR DL Taylor 3/19/86
RELEASE APPROV DL Taylor 3/19/86
MATERIAL
FINISH WAVETEK PROCESS
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE ASSEMBLY, RAM EXPANSION BOARD OPTION 50-12-256K
MODEL NO. 51/52
DWG NO. 1000-00-0471
REV B
CODE IDENT 23338
SHEET 1 OF 1

1000-00-0471 B

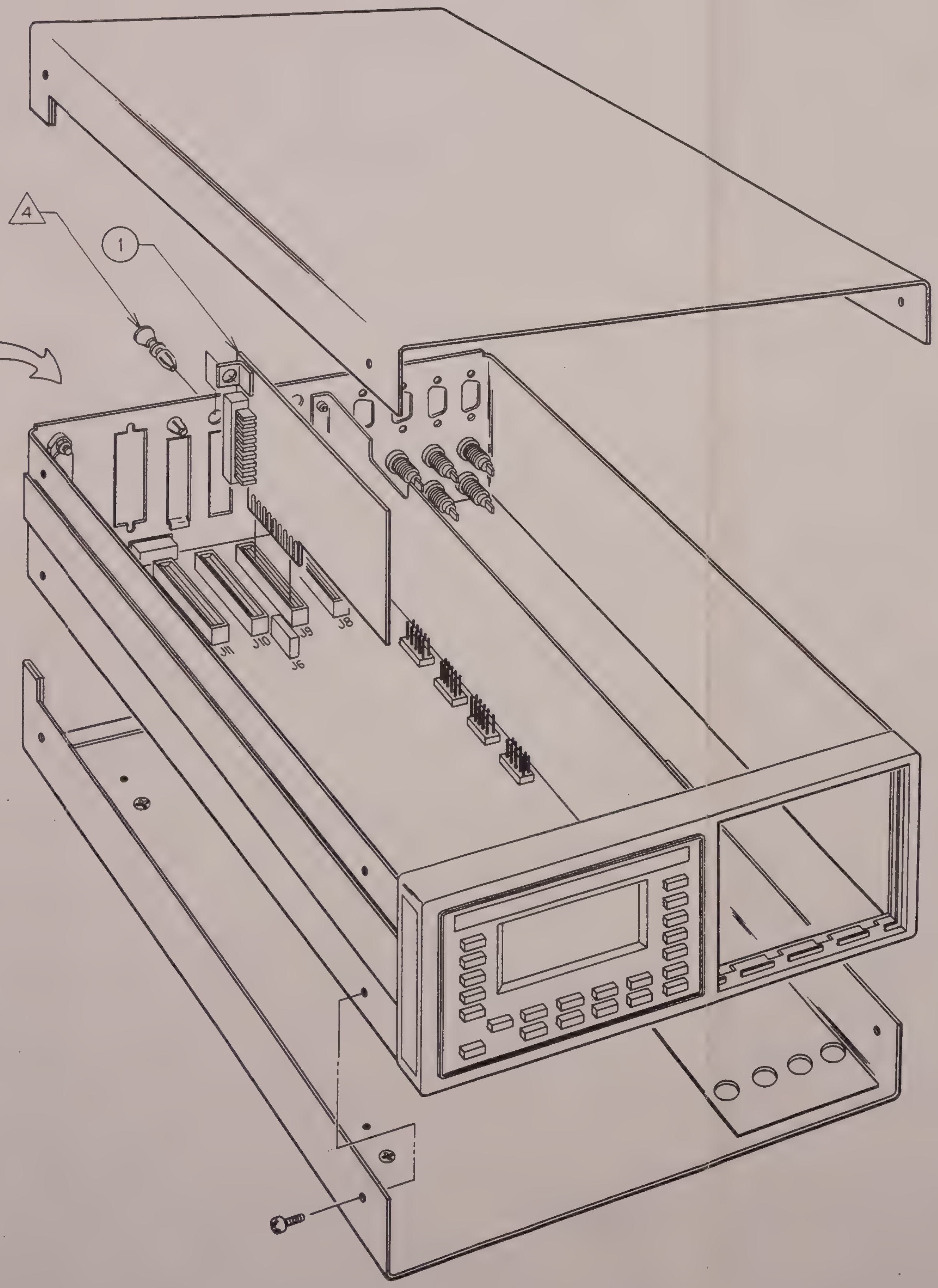
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A2708

REV	ECN	BY	DATE	APP
A	FOR RELEASE	[illegible]	3/24/86	ΛM
B	#7592	[illegible]	7/15/86	C.C.
C	# 7600	[illegible]	7/29/86	R.P.T.



SAMPLE REAR PANEL CONFIGURATION

(DIGITAL I/O INSTALLED IN J9 - REAR PANEL OPTION 7)



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
1	PCA, DIGITAL I/O BOARD	52-1814	WVTK	1100-00-1814	1
2	CONN, DUAL POLARIZED, 26 PIN .100X.100 CNTRS	746091-6	AMP	2100-02-0222	1

WAVETEK
PARTS LIST
TITLE
DIGITAL I/O AND ANALOG OUT OPT 50-14
ASSEMBLY NO. 1000-00-0472
REV C
PAGE 1

5. ITEM 2, MATING CONNECTOR, IS NOT SHOWN ON FACE OF DRAWING.

⚠4. DIGITAL I/O COVER (1400-02-158) WHICH IS SECURED WITH PLASTIC SNAP FASTENER ASSEMBLY (2800-60-0004 & 2800-60-0005) IS TO BE REMOVED PRIOR TO DIGITAL I/O BOARD INSTALLATION. BOARD ASSEMBLY TO BE SECURED WITH SAME PLASTIC SNAP FASTENER ASSEMBLY.

3. OPTION 50-14 DIGITAL I/O BOARD ASSEMBLY (1100-00-1814) MAY BE INSTALLED IN EITHER J7 (REAR PANEL OPTION 5), J8 (REAR PANEL OPTION 6), J9 (REAR PANEL OPTION 7) OR J10 (REAR PANEL OPTION 8). SPECIFIC SLOT LOCATION(S) IS DEPENDENT UPON TOTAL INSTRUMENT CONFIGURATION.

2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

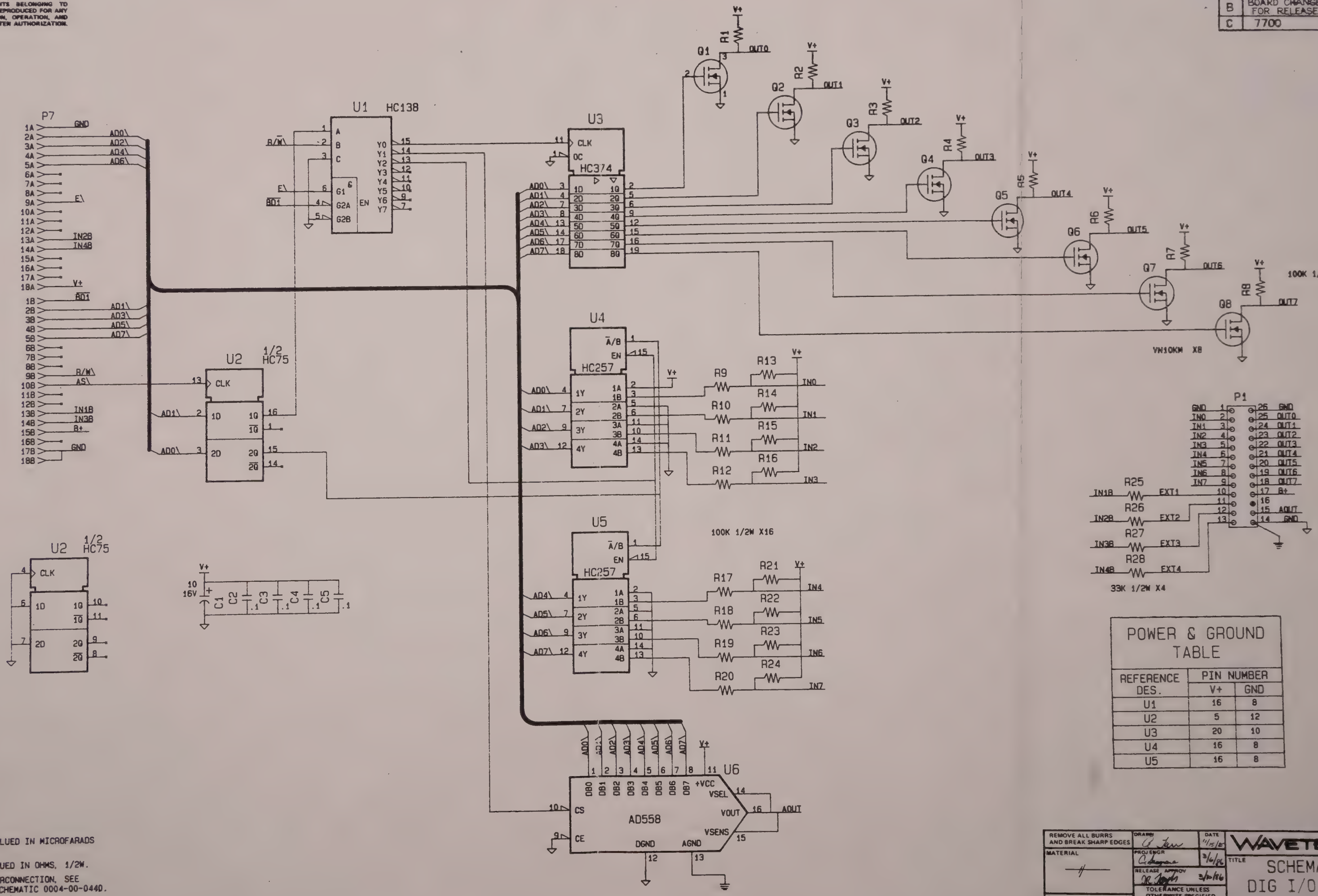
NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0472

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL —//—
FINISH WAVETEK PROCESS —//—
DRAWN A.TALMADGE DATE 3/20/86
PROJ ENGR N. E. Miller 3/24/86
RELEASE APPROV 3-25-86
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE ASSEMBLY, DIGITAL I/O AND ANALOG OUT OPTION (OPTION 50-14)
MODEL NO. 51/52
DWG NO. 1000-00-0472
REV C
CODE IDENT 23338
SHEET 1 OF 1

1000-00-0472 C

REV		BY		
A	BOARD CHANGES	AT		
B	BOARD CHANGES, FOR RELEASE			
C	7700	ACT		


P7
1A GND
2A AD0\
3A AD2\
4A AD4\
5A AD6\
9A E\
13A IN2B
14A IN4B
18A V+
1B BD1
2B AD1\
3B AD3\
4B AD5\
5B AD7\
9B R/W\
10B AS\
13B IN1B
14B IN3B
15B B+
17B GND
U1 HC138
A B C G1 G2A G2B EN
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
R/W\
E\
BD1
U2 1/2 HC75
CLK 1D 2D 1Q 2Q
U3 HC374
CLK OC
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
R1 R2 R3 R4 R5 R6 R7 R8
OUT0 OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7
100K 1/2W X8
VN10KM X8
U4 HC257
U5 HC257
Ā/B EN 1Y 2Y 3Y 4Y 1A 1B 2A 2B 3A 3B 4A 4B
R9 R10 R11 R12 R13 R14 R15 R16
IN0 IN1 IN2 IN3
R17 R18 R19 R20 R21 R22 R23 R24
IN4 IN5 IN6 IN7
100K 1/2W X16
U2 1/2 HC75
C1 10 16V
C2 .1
C3 .1
C4 .1
C5 .1
U6 AD558
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 +VCC
VSEL VOUT VSENS CS CE DGND AGND
AOUT
P1
GND IN0 IN1 IN2 IN3 IN4 IN5 IN6 IN7
26 GND 25 OUT0 24 OUT1 23 OUT2 22 OUT3 21 OUT4 20 OUT5 19 OUT6 18 OUT7 17 B+ 16 15 AOUT 14 GND
R25 R26 R27 R28
IN1B IN2B IN3B IN4B
EXT1 EXT2 EXT3 EXT4
33K 1/2W X4

POWER & GROUND TABLE

REFERENCE DES.	PIN NUMBER	
	V+	GND
U1	16	8
U2	5	12
U3	20	10
U4	16	8
U5	16	8

3. CAPACITORS VALUED IN MICROFARADS (uF).
2. RESISTORS VALUED IN OHMS, 1/2W.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN A. Fan DATE 11/15/85
PROJ ENGR 3/6/86
RELEASE APPROV 3/10/86
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE

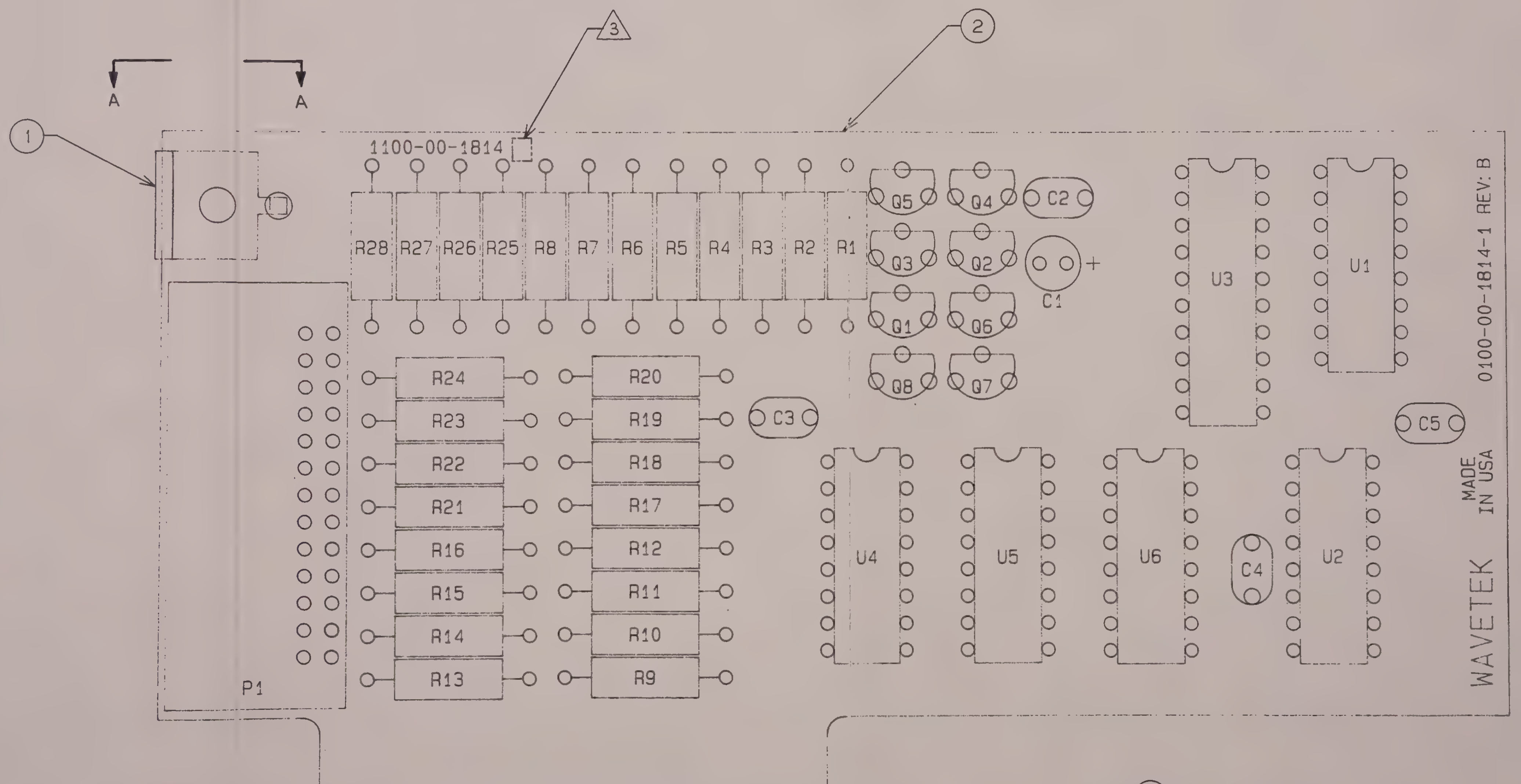
WAVETEK SAN DIEGO • CALIFORNIA

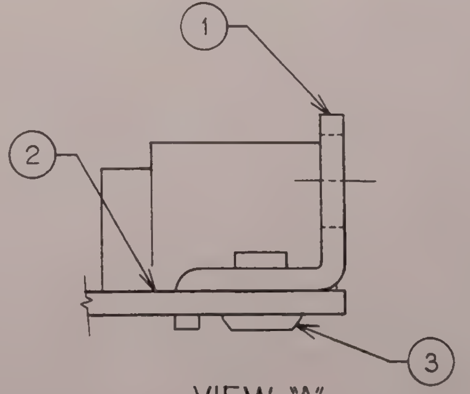
TITLE
SCHEMATIC,
DIG I/O OPTION

MODEL NO. 51/52
DWG NO. 0103-00-1814
REV C
CODE IDENT 23338
SHEET 1 OF 1

0103-00-1814 C

REV	ECN	BY	DATE	APP
A	BOARD CHANGES	AT	1/14/86	NM
B	LINE CLEARANCES FIXED, FOR RELEASE	AT	3/6/86	NM
C	#7700	AT	9/24/86	D R.T.
D	#7818	AT	12/19/86	A R.T.


A
A
1
3
2
1100-00-1814
R28
R27
R26
R25
R8
R7
R6
R5
R4
R3
R2
R1
Q5
Q4
C2
Q3
Q2
C1
+
Q1
Q6
Q8
Q7
U3
U1
0100-00-1814-1 REV: B
R24
R20
R23
R19
R22
R18
R21
R17
R16
R12
R15
R11
R14
R10
R13
R9
P1
C3
C5
U4
U5
U6
C4
U2
MADE IN USA
WAVETEK



VIEW "A"

3. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
2. SEE INSTRUMENT SCHEMATIC 0004-00-0440 FOR ASSEMBLY INTERCONNECTION.
1. SEE 0103-00-1814 FOR SCHEMATIC.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1100-00-1814.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. Tarr	DATE 1/14/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	PROJ ENGR N. S. Muller	1/14/86	TITLE PCA, DIGITAL 1/0
	RELEASE APPROV R. Taylor	3/6/86	
FINISH WAVETEK PROCESS —//—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 .XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO. 51, 52
	SCALE 4/1		DWG NO. 1100-00-1814
			REV D
			CODE IDENT 23338
			SHEET 1 OF 1

1100-00-1814 D

BISHOP GRAPHICS/ACCUPRESS REORDER NO A2708B

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PCA, DIGITAL I/O BOARD	0103-1814	WVTK	0103-00-1814	1
1	BRKT, RETAINING	52-1213	WVTK	1400-02-1213	1
C2 C3 C4 C5	CAP CER MON 1MF 50V Z5U +80/-20% RAD LD SP .2	SR215E104ZAA	AVX	1500-01-0420	4
C1	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	1
2	DRILL DRWG, PCA, DIGITAL I/O BOARD	1700-1814	WVTK	1700-00-1814	1
P1	CONNECTOR HEADER, 26 PIN, 0.1 SPACE DOUBLE	1-103167-0	AMP	2100-02-0201	1
3	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	1
R1 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R3 R4 R5 R6 R7 R8 R9	RESISTOR, METAL OXIDE, 1/2W, 100K, 5%	RSF1/2BJ100K	M-OHM	4705-25-1003	24
R25 R26 R27 R28	RESISTOR, METAL OXIDE, 1/2W, 5%, 33K	RSF1/2BJ33K	M-OHM	4705-25-3302	4
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8	TRANS	VN10KM	SILX	4902-00-0100	8
U6	DAC, 8-BIT, INTERNAL REF, 16 PIN DIP	AD558JN	ANDEV	7000-05-5801	1

WAVETEK PARTS LIST	TITLE PCA, DIGITAL I/O BOARD	ASSEMBLY NO. 1100-00-1814 PAGE 1	REV D

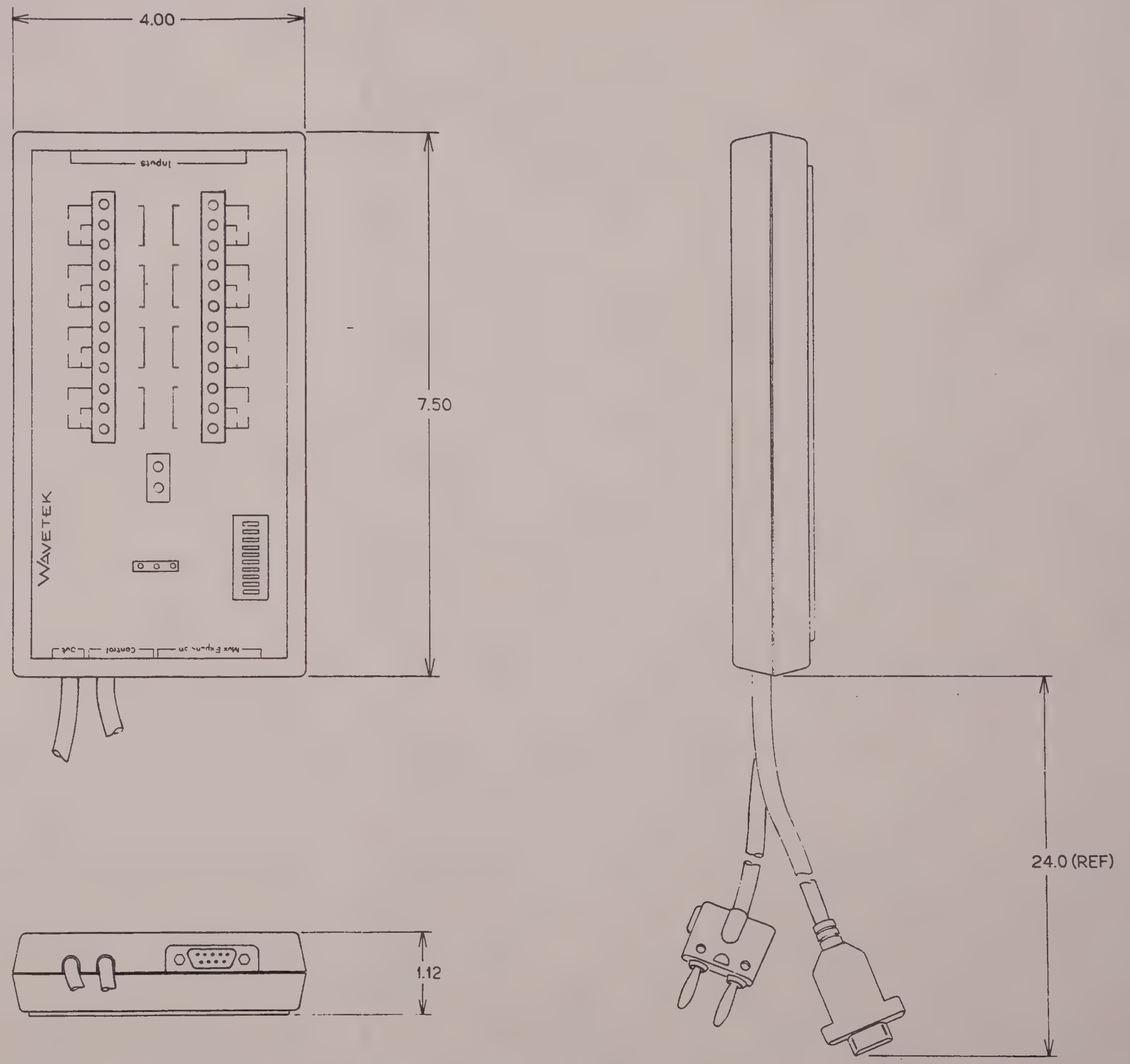
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U2	LATCH QUAD, TRANSPARENT, HCMOS, 16 PIN DIP	N74HC75N	SIG	8000-74-7501	1
U1	DECODER, 3-8 LINE, CMOS	MC74HC138N	MOT	8007-41-3840	1
U4 U5	MUX, QUAD 2-INPUT, TRI-STATE, HCMOS, 16 PIN	N74HC257N	SIG	8007-42-5701	2
U3	CMOS, D-F/F, TRI-S OCT	74HC374	TI	8007-43-7440	1

WAVETEK PARTS LIST	TITLE PCA, DIGITAL I/O BOARD	ASSEMBLY NO. 1100-00-1814 PAGE 2	REV D

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE PARTS LIST DIGITAL I/O
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-1814 · REV D
DO NOT SCALE DRAWING			SCALE Option 50-14 · SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE		7 1/86	NM


4.00
Inputs
WAVETEK
Out
Control
Mux Expansion
7.50
1.12
24.0 (REF)

2. UNIT WEIGHT: .4 KG (1.0 LB) NET

1. DIMENSIONS ARE IN INCHES.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN A.TALMADGE
DATE 6/12/86
PROJ ENGR
7/7/86
RELEASE APPROV
MATERIAL
FINISH WAVETEK PROCESS
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE FULL

WAVETEK SAN DIEGO • CALIFORNIA

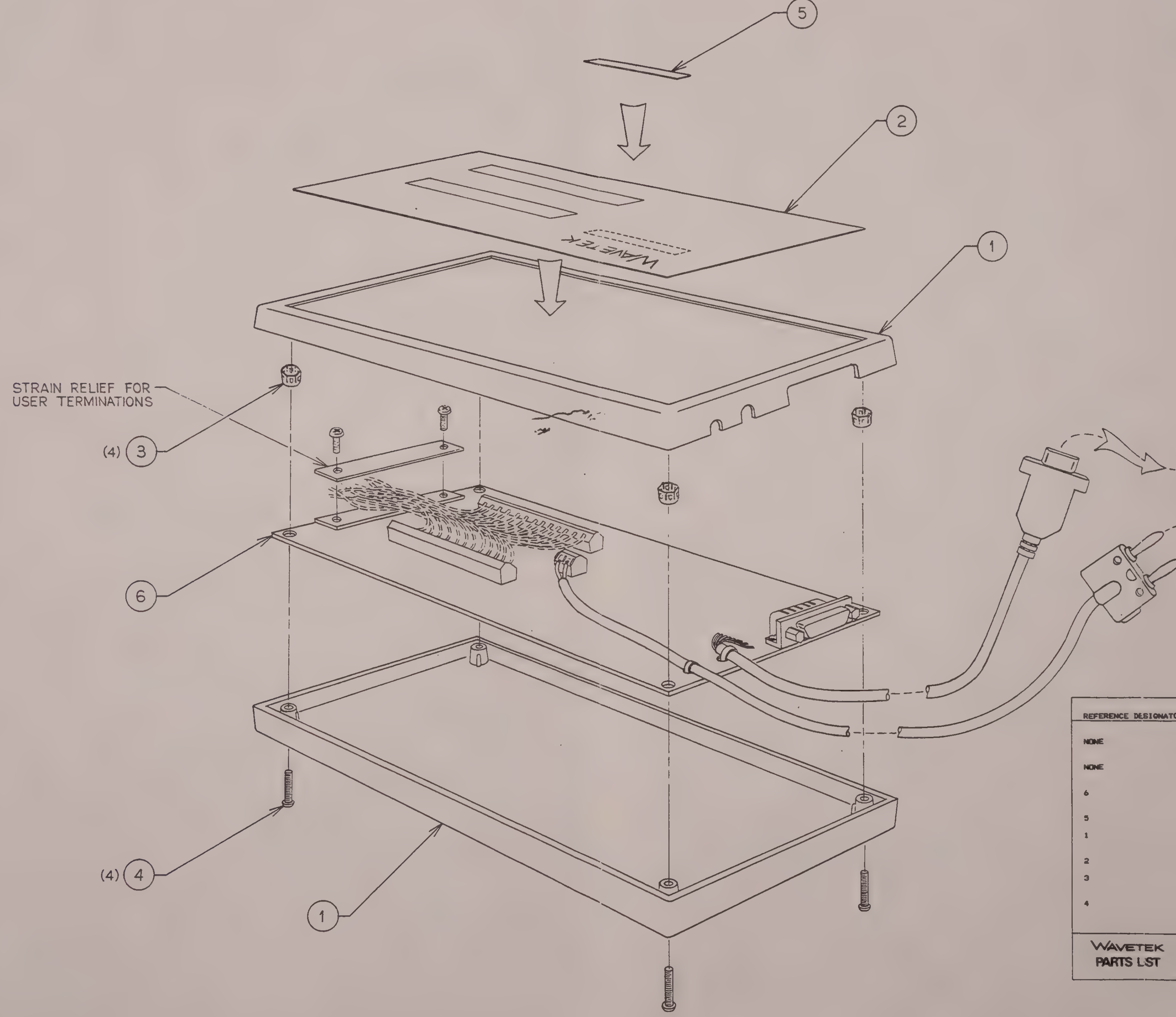
TITLE

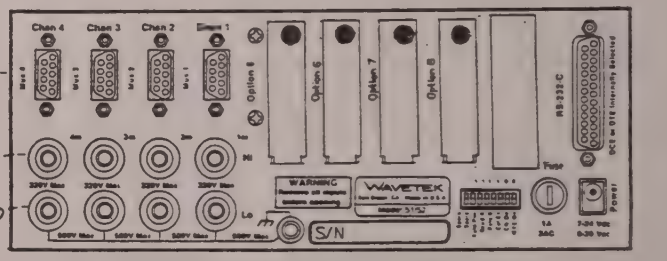
OUTLINE DRAWING
(8/16 CHANNEL MULTIPLEXER)

MODEL NO. 51/52
DWG NO 0002-00-0473
REV A
CODE IDENT 23338
SHEET 1 OF 1

0002-00-0473 A

REV	ECN	BY	DATE	APP
A	FOR RELEASE		7/2/86	


5
2
WAVETEK
1
STRAIN RELIEF FOR USER TERMINATIONS
(4) 3
6
(4) 4
1


Chan 4
Chan 3
Chan 2
1
Option 6
Option 7
Option 8
RS-232-C
Hi
Lo
WARNING
WAVETEK
Fuse
Power
S/N

MODEL 52 REAR PANEL
(VIEW FOR HOOKUP PICTORIAL ONLY)

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	OUTLINE DRAWING 8/16 CHANNEL MULTIPLEXER	0002-00-0473	WVTK	0002-00-0473	1
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
6	ASSY, 8/16 CHANNEL MUX BOARD	52-001-2656	WVTK	1100-00-2656	1
5	SERIAL TAG MODEL 602	602-6950	WVTK	1400-01-6950	1
1	ENCLOSURE 8/16 CHANNEL MULTIPLEXER	1400-02-2019	WVTK	1400-02-2019	1
2	LABEL, H.V. MUX	1400-02-2020	WVTK	1400-02-2020	1
3	ON-SERT FASTENER, 4-40	NR 440004	PAL	2800-09-0035	4
4	SCREW, PAN, CAD I, CROSS RECESS.	MS51957-17	COML	2800-38-4108	4

WAVETEK PARTS LIST	TITLE 8/16 CHANNEL HI-V MULTIPLEXER OPT 50-20	ASSEMBLY NO. 1000-00-0473 PAGE 1	REV A

SEE SEPARATE PARTS LIST 1000-00-0473

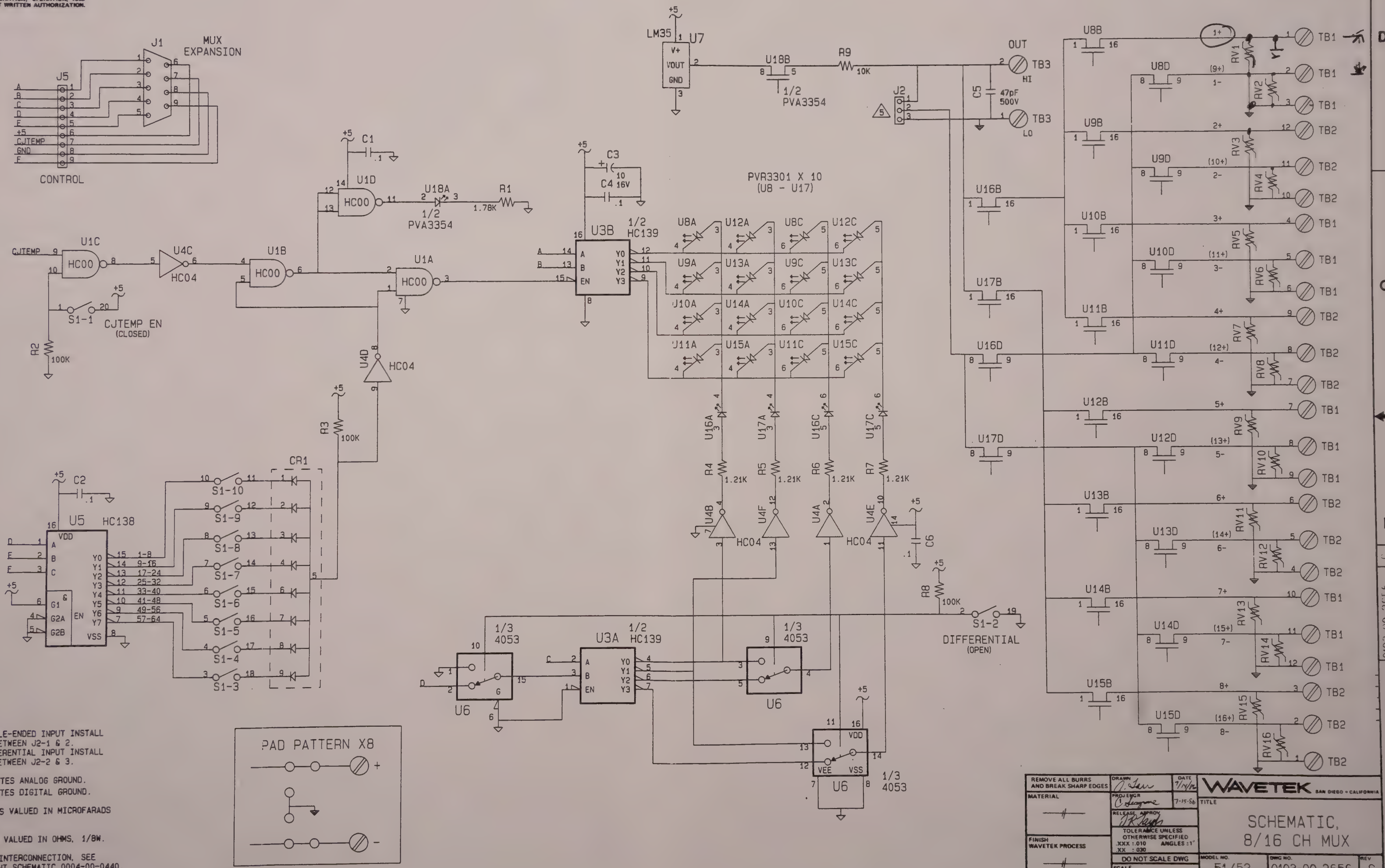
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.TALMADGE	DATE 6/4/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	7/7/86	TITLE ASSEMBLY, 8/16 CHANNEL MULTIPLEXER (OPTION 50-20)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO 51/52 | DWG NO 1000-00-0473 | REV A
	SCALE NONE		CODE IDENT 23338 | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. AJ7086

REV	ECN	BY	DATE	APP
C	FOR RELEASE	JT	7/7/86	TJM


J1
MUX EXPANSION
J5
A
B
C
D
E
+5
CJTEMP
GND
F
CONTROL
LM35
U7
V+
VOUT
GND
U18B
1/2
PVA3354
R9
10K
OUT
TB3
HI
LO
J2
5
C5
47pF
500V
C1
.1
U1D
HC00
U18A
1/2
PVA3354
R1
1.78K
C3
C4 16V
10
U3B
1/2
HC139
PVR3301 X 10
(U8 - U17)
U1C
HC00
U4C
HC04
U1B
U1A
S1-1
CJTEMP EN
(CLOSED)
R2
100K
U4D
R3
100K
CR1
C2
U5
HC138
VDD
G1
G2A
G2B
EN
VSS
1-8
9-16
17-24
25-32
33-40
41-48
49-56
57-64
S1-10
S1-9
S1-8
S1-7
S1-6
S1-5
S1-4
S1-3
U8A
U12A
U8C
U12C
U9A
U13A
U9C
U13C
U10A
U14A
U10C
U14C
U11A
U15A
U11C
U15C
U16A
U17A
U16C
U17C
R4
R5
R6
R7
1.21K
U4B
U4F
U4A
U4E
C6
R8
100K
S1-2
DIFFERENTIAL
(OPEN)
1/3
4053
U6
U3A
1/2
HC139
VEE
VSS
U8B
U8D
U9B
U9D
U10B
U10D
U11B
U11D
U12B
U12D
U13B
U13D
U14B
U14D
U15B
U15D
U16B
U17B
U16D
U17D
RV1
RV2
RV3
RV4
RV5
RV6
RV7
RV8
RV9
RV10
RV11
RV12
RV13
RV14
RV15
RV16
TB1
TB2
1+
(9+)
1-
2+
(10+)
2-
3+
(11+)
3-
4+
(12+)
4-
5+
(13+)
5-
6+
(14+)
6-
7+
(15+)
7-
8+
(16+)
8-
PAD PATTERN X8
+
-

5. FOR SINGLE-ENDED INPUT INSTALL JUMPER BETWEEN J2-1 & 2. FOR DIFFERENTIAL INPUT INSTALL JUMPER BETWEEN J2-2 & 3.

4. ⏚ INDICATES ANALOG GROUND.
⏚ INDICATES DIGITAL GROUND.

3. CAPACITORS VALUED IN MICROFARADS (uF).

2. RESISTORS VALUED IN OHMS, 1/8W.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN J. Tan DATE 7/14/86
PROJ ENGR C. Leggmee 7-15-86
RELEASE APPROV TK Taylor

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

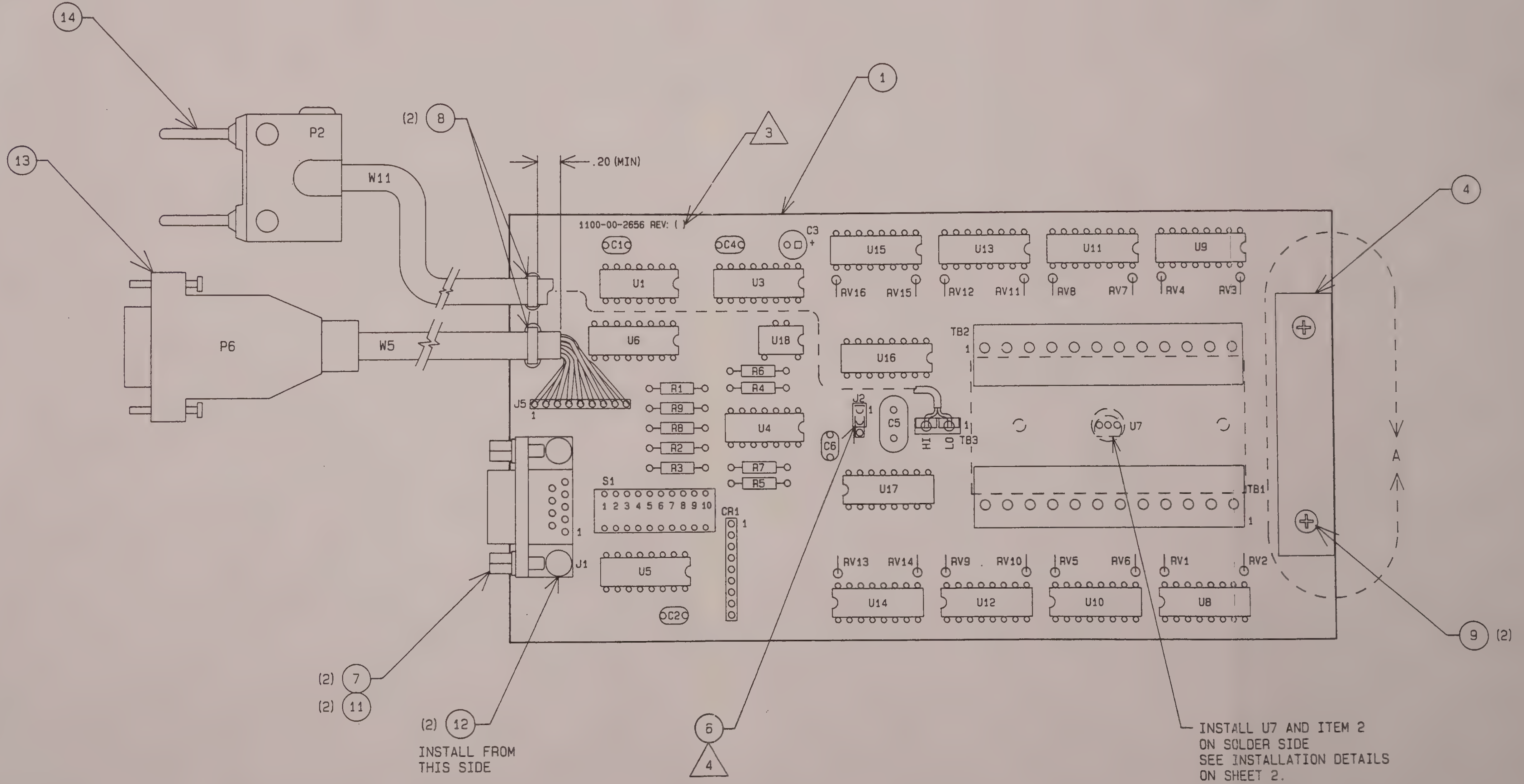
SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
8/16 CH MUX

MODEL NO. 51/52
DWG NO. 0103-00-2656
REV C
CODE IDENT 23338
SHEET 1 OF 1

REV	ECN	BY	DATE	APP
B	FOR RELEASE	A.T.	7/14/86	N.M.
C	#7635	AT	8/23/86	NM


14
P2
(2) 8
13
W11
3
.20 (MIN)
1
4
1100-00-2656 REV: ( )
C1
C4
C3
U15
U13
U11
U9
RV16
RV15
RV12
RV11
RV8
RV7
RV4
RV3
U1
U3
P6
W5
U6
U18
U16
TB2
1
J5
1
R1
R9
R8
R2
R3
R6
R4
R7
R5
U4
J2
C5
C6
HI
LO
TB3
U7
A
TB1
S1
1 2 3 4 5 6 7 8 9 10
CR1
J1
U5
C2
RV13
RV14
RV9
RV10
RV5
RV6
RV1
RV2
U14
U12
U10
U8
9 (2)
(2) 7
(2) 11
(2) 12
6
4

INSTALL FROM
THIS SIDE

INSTALL U7 AND ITEM 2
ON SOLDER SIDE
SEE INSTALLATION DETAILS
ON SHEET 2.

J5 WIRE CONNECTIONS	
PIN NO.	WIRE COLOR
1	BROWN
2	RED
3	ORANGE
4	YELLOW
5	GREEN
6	BLUE
7	VIOLET
8	GRAY
9	BLACK

TB3 WIRE CONNECTIONS		
PIN NO.	WIRE COLOR	DESIGNATION
1	BLACK	LO
2	RED	HI

5. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
4. FOR SINGLE-ENDED INPUT INSTALL JUMPER BETWEEN J2-1 & 2. FOR DIFFERENTIAL INPUT INSTALL JUMPER BETWEEN J2-2 & 3.
3. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.
1. SEE 0103-00-2656 FOR SCHEMATIC.

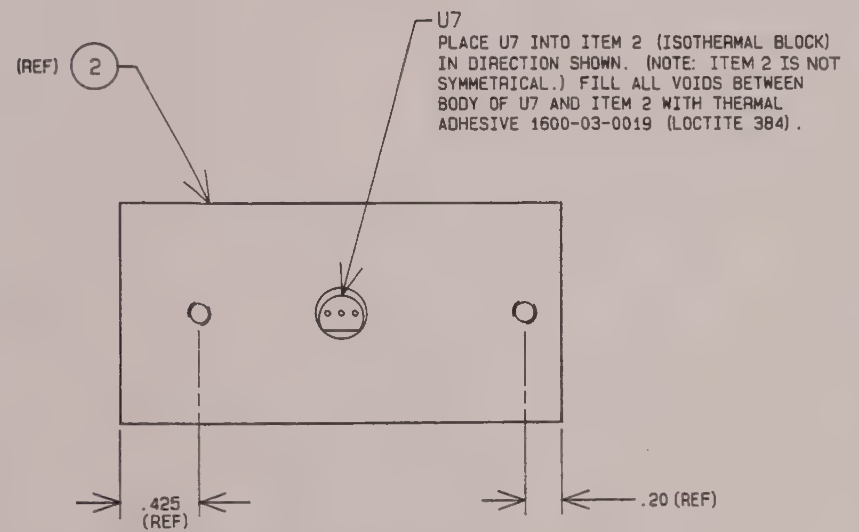
NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1100-00-2656

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A TALMADGE	DATE 7/14/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR C SEAGRAVE	7/15/86	TITLE PCA, 8/16 CH MUX BOARD
	RELEASE APPROV DR TAYLOR		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 .XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO. 51/52 · DWG NO. 1100-00-2656 · REV C
	SCALE NONE		CODE IDENT 23338 · SHEET 1 OF 2

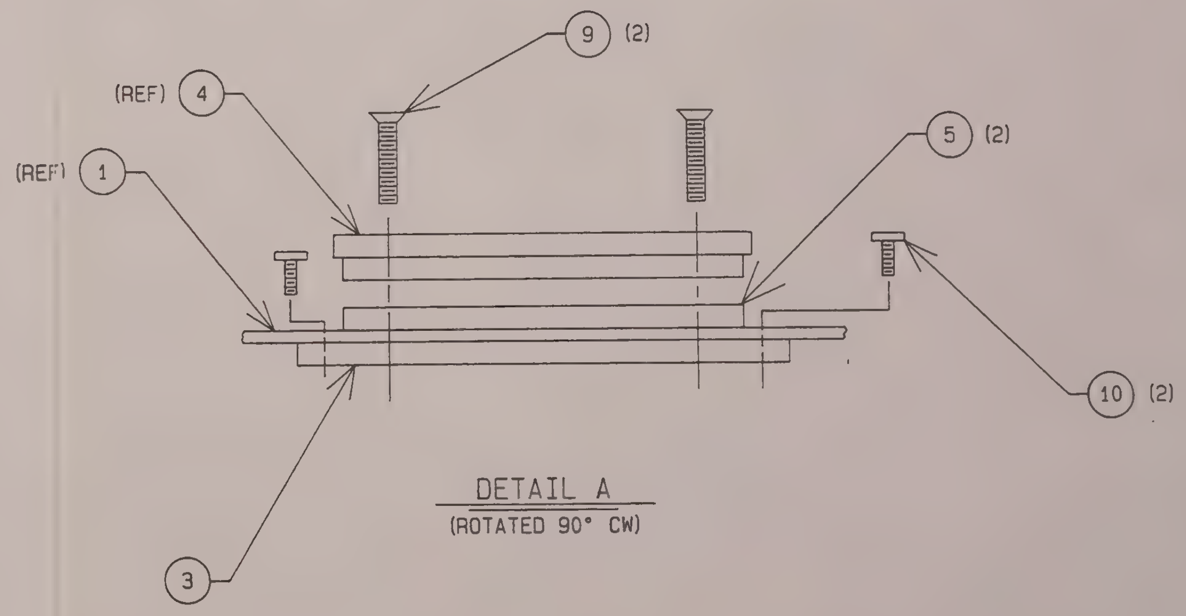
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A2708

REV	ECN	BY	DATE	APP

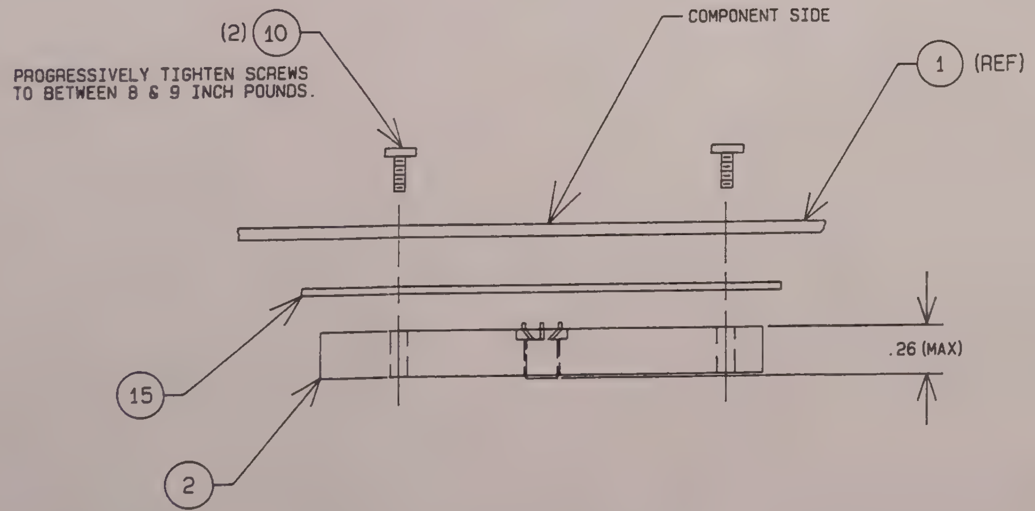


U7
PLACE U7 INTO ITEM 2 (ISOTHERMAL BLOCK) IN DIRECTION SHOWN. (NOTE: ITEM 2 IS NOT SYMMETRICAL.) FILL ALL VOIDS BETWEEN BODY OF U7 AND ITEM 2 WITH THERMAL ADHESIVE 1600-03-0019 (LOCTITE 384).

U7 INSTALLATION



DETAIL A
(ROTATED 90° CW)



PROGRESSIVELY TIGHTEN SCREWS TO BETWEEN 8 & 9 INCH POUNDS.

INSTALLATION OF ITEMS 2 & 15

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN A.TALMADGE DATE 7/14/86
PROJ ENGR 7-15-86
RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG
SCALE 2/1

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PCA,
8/16 CH MUX
BOARD

MODEL NO. 51/52
DWG NO. 1100-00-2656
REV C
CODE IDENT 23338
SHEET 2 OF 2

1100-00-2656 C

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, 8/16 CHANNEL MUX BOARD	0103-00-2656	WVTK	0103-00-2656	1
2	ISOTHERMAL BLOCK	52-1053	WVTK	1400-02-1053	1
3	BAR CLAMP, LOWER	52-1063	WVTK	1400-02-1063	1
4	BAR CLAMP, UPPER	52-1073	WVTK	1400-02-1073	1
5	RETAINER, CABLE CLAMP	1400-02-2040	WVTK	1400-02-2040	2
15	INSULATOR, ISOTHERMAL BLOCK	1400-02-2130	WVTK	1400-02-2130	1
C1 C2 C4 C6	CAP CER MON 1MF 50V Z5U +80/-20% RAD LD SP .2	SR215E104ZAA	AVX	1500-01-0420	4
C5	CAP, MICA, 47PF, 500V	DM15-470J	ARCO	1500-14-7000	1
C3	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	1
1	DRILL DRWG, PCA, MUX 50-20	1700-00-2656	WVTK	1700-00-2656	1
J2	CONN, HEADER, 3 PIN	929834-01-03	APTRN	2100-02-0196	1
J1	CONNECTOR, RT ANGLE PC MOUNT, 9 PIN	745394-2	AMP	2100-02-0200	1
6	JUMPER, FEMALE, 2 POSITION, 0.1 SPACE	929950-00	APTRN	2100-02-0213	1

WAVETEK PARTS LIST
TITLE ASSY, 8/16 CHANNEL MUX BOARD
ASSEMBLY NO. 1100-00-2656
REV C
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
7	SCREWLOCK, CONNECTOR, FEMALE, SHORT	205818-2	AMP	2100-07-0007	2
TB1 TB2	TERMINAL STRIP 12 PIN PC MOUNT	25.135.1253	ELECT	2100-09-0019	2
TB3	TERMINAL STRIP 2 PIN, PC MOUNT	25.135.0253	ELECT	2100-09-0020	1
8	TY-WRAP	TY-523M	TB	2800-00-0006	2
9	MACHINE SCREW, 82 DEG, F.H., PHLPS, 4-40X5/8,	4-40X5/8 PHLPS M/S	CMRCL	2800-19-4110	2
10	SCREW, SELF LOCKING, PAN CROSS RECESS	4-40 X 1/4	CMRCL	2800-23-4104	4
11	WASHER, SPLIT LOCK, 4	#4SRLW	CMRCL	2800-42-4000	2
12	PLASTIC RIVET	231-080551-05-0101	FASTX	2800-60-0008	2
U18	RELAY, PHOTO VOLTAIC, SP, 130mA	PVA3354	IR	4500-00-0032	1
U10 U11 U12 U13 U14 U15 U16 U17 U8 U9	RELAY, PHOTO VOLTAIC, BOSFET, 16 PIN DIP	PVR3301	IR	4500-01-0001	10
R9	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	1
R2 R3 R8	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	3

WAVETEK PARTS LIST
TITLE ASSY, 8/16 CHANNEL MUX BOARD
ASSEMBLY NO. 1100-00-2656
REV C
PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R4 R5 R6 R7	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	4
R1	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	1
CR1	DIODE, SIP, ULTRA HIGH SPEED SWITCHING	DAP801	ROHM	4805-02-0801	1
RV1 RV10 RV11 RV12 RV13 RV14 RV15 RV16 RV2 RV3 RV4 RV5 RV6 RV7 RV8 RV9	VARISTOR, METAL OXIDE	V390MA3A	GE	4899-00-0049	16
S1	SWITCH, DIP, SPST ROCKER	76SB10	GRHL	5199-00-0009	1
W5	CABLE, CONTROL	6001-50-0021	WVTK	6001-50-0021	1
W11	OUTPUT CABLE ASSY	6009-90-0039	WVTK	6009-90-0039	1
U7	IC, CENTIGRADE TEMP SENSOR	LM35DZ	NAT	7000-00-3500	1
U6	IC, TRIPLE 2 CHANNEL MUX\DEMUX	CD4053BCN	NSC	8000-40-5300	1
U1	IC, QUAD 2 INPUT NAND GATE, 14 PIN DIP	MC74HC00N	MOT	8000-74-0011	1
U4	CMOS, ENVERTER, HEX	MM74HC04	NSC	8000-74-0440	1
U5	DECODER, 3-8 LINE, CMOS	MC74HC138N	MOT	8007-41-3840	1

WAVETEK PARTS LIST
TITLE ASSY, 8/16 CHANNEL MUX BOARD
ASSEMBLY NO. 1100-00-2656
REV C
PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U3	IC, DUAL 1 OF 4 DECODER/DEMUX, 16 PIN DIP	MC74HC139N	MOT	8007-41-3911	1

WAVETEK PARTS LIST
TITLE ASSY, 8/16 CHANNEL MUX BOARD
ASSEMBLY NO. 1100-00-2656
REV C
PAGE 4

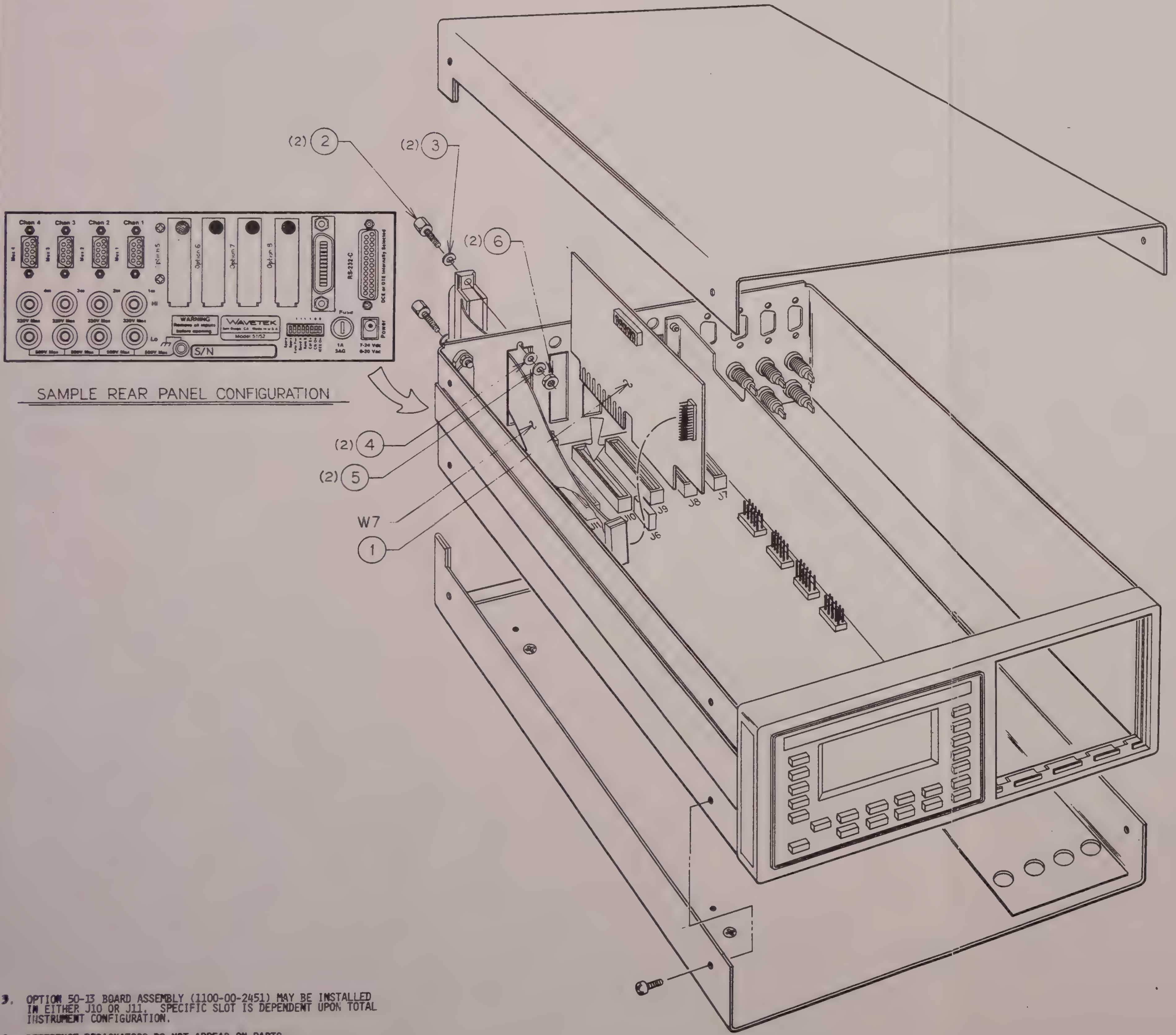
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE PARTS LIST ASSY, 8/16 CHANNEL MUX BOARD
SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-2656
REV C
SCALE
MODEL
SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP
A	FOR RELEASE	t.	3/24/86	


Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS-232-C
DCE or DTE Internally Selected
Hi
Lo
WARNING
WAVETEK
Model 51/52
S/N
Fuse
1A
3AG
Power
7-24 Vdc
6-20 Vac
(2) 2
(2) 3
(2) 6
(2) 4
(2) 5
W7
1
J6
J7
J8
J9
J10
J11

SAMPLE REAR PANEL CONFIGURATION

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
1	ASSY, GPIB OPT BOARD	52-2451	WVTK	1100-00-2451	1
2	JACK SCREW	859-0530	WVTK	1400-01-0530	2
6	NUT, HEX, CAD PLATE 6-32	MS35649-264	COML	2800-14-6100	2
4	WASHER, FLAT, #6 BIN 495	#6FLAT WASHER	CMRCL	2800-26-6001	2
5	WASHER, SPLIT LOCK #6 6	#6SRLW	CMRCL	2800-42-6000	2
3	LOCKWASHER, #8 SPLIT RING BIN 540	#8SRLW	CMRCL	2800-42-8000	2
W7	RIBBON CABLE ASSEMBLY, 24 PIN, 6.75"	6002-00-0044	WVTK	6002-00-0044	1

WAVETEK
PARTS LIST
TITLE
IEEE-488 BOARD OPT 50-13
ASSEMBLY NO. 1000-00-0476
REV B
PAGE 1

3. OPTION 50-13 BOARD ASSEMBLY (1100-00-2451) MAY BE INSTALLED IN EITHER J10 OR J11. SPECIFIC SLOT IS DEPENDENT UPON TOTAL INSTRUMENT CONFIGURATION.

2. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

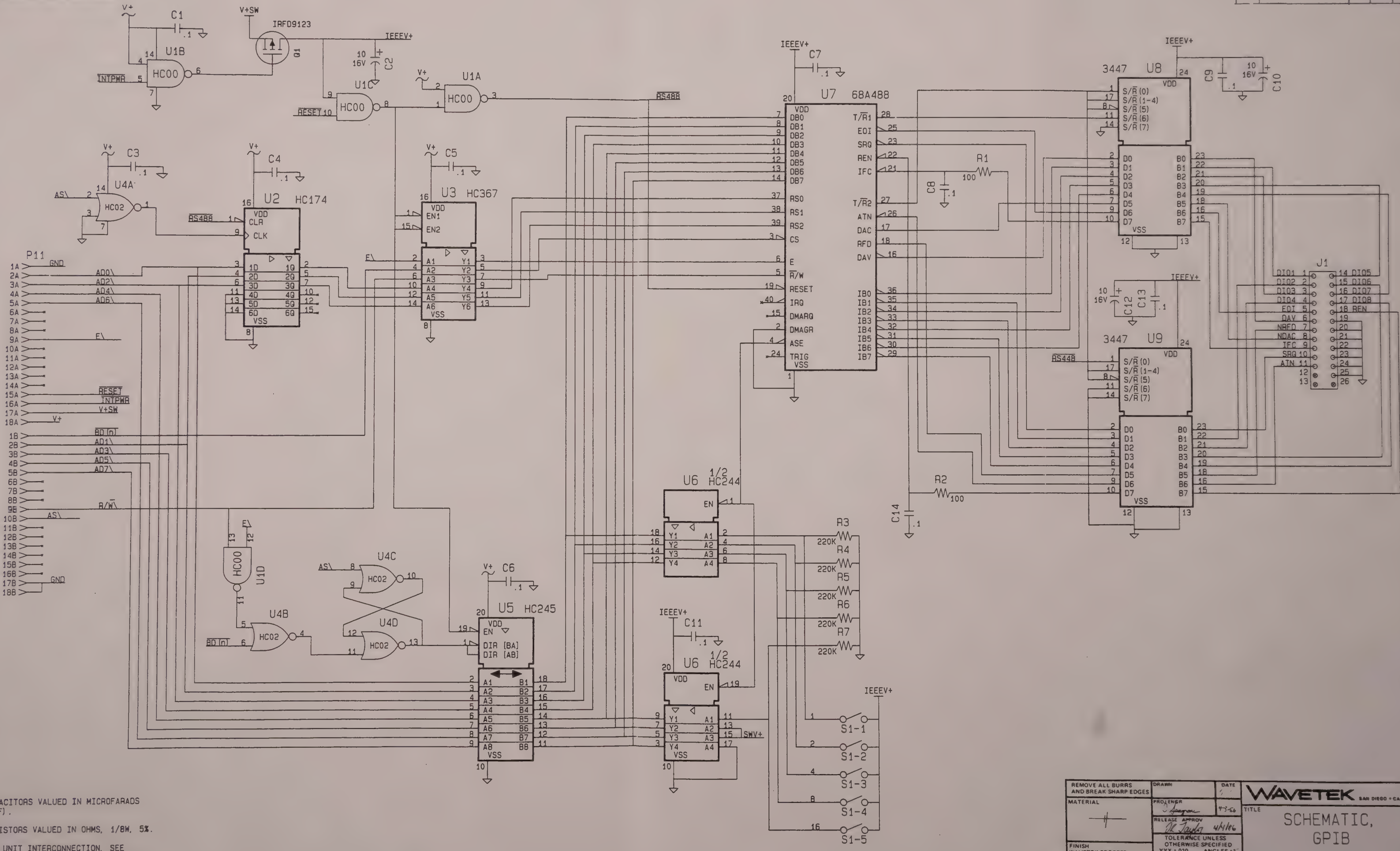
NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0476

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3/24/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL -ǁ-	PROJ ENGR N. F. Miller	3/24/86	TITLE ASSEMBLY, IEEE-488 BOARD OPTION (OPTION 50-13)
	RELEASE APPROV JC Taylor 4/4/86		
FINISH WAVETEK PROCESS -ǁ-	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52 · DWG NO. 1000-00-0476 · REV A
	SCALE NONE		CODE IDENT 23338 · SHEET 1 OF 1

1000-00-0476 A

REV	ECN	BY	DATE	APP
B	FOR RELEASE	AT	4/1/86	ΥM
C	#7751	OJ	10/28/86	A.R.T.


V+
C1
.1
V+SW
IRFD9123
Q1
IEEEV+
10
16V
C2
U1B
HC00
INTPWR
U1C
RESET
U1A
RS488
C3
U4A
HC02
AS\
C4
U2
HC174
VDD
CLR
CLK
C5
U3
HC367
EN1
EN2
E\
P11
GND
AD0\
AD2\
AD4\
AD6\
V+SW
BD(n)
AD1\
AD3\
AD5\
AD7\
R/W
U1D
U4B
U4C
U4D
C6
U5
HC245
DIR (BA)
DIR (AB)
C7
U7
68A488
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
RS0
RS1
RS2
CS
E
R/W
RESET
IRQ
DMARQ
DMAGR
ASE
TRIG
VSS
T/R1
EOI
SRQ
REN
IFC
T/R2
ATN
DAC
RFD
DAV
IB0
IB1
IB2
IB3
IB4
IB5
IB6
IB7
R1
100
C8
C14
R2
100
U6
1/2
HC244
EN
C11
SWV+
R3
R4
R5
R6
R7
220K
S1-1
S1-2
S1-3
S1-4
S1-5
3447
U8
C9
C10
S/R(0)
S/R(1-4)
S/R(5)
S/R(6)
S/R(7)
U9
RS448
C12
C13
J1
DIO1
DIO2
DIO3
DIO4
EOI
DAV
NRFD
NDAC
IFC
SRQ
ATN
DIO5
DIO6
DIO7
DIO8
REN

3. CAPACITORS VALUED IN MICROFARADS (uF).

2. RESISTORS VALUED IN OHMS, 1/8W, 5%.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN

PROJ ENGR 4-3-86

RELEASE APPROV Jk Taylor 4/4/86

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
GPIB

MODEL NO 51/52

DWG NO. 0103-00-2451

REV C

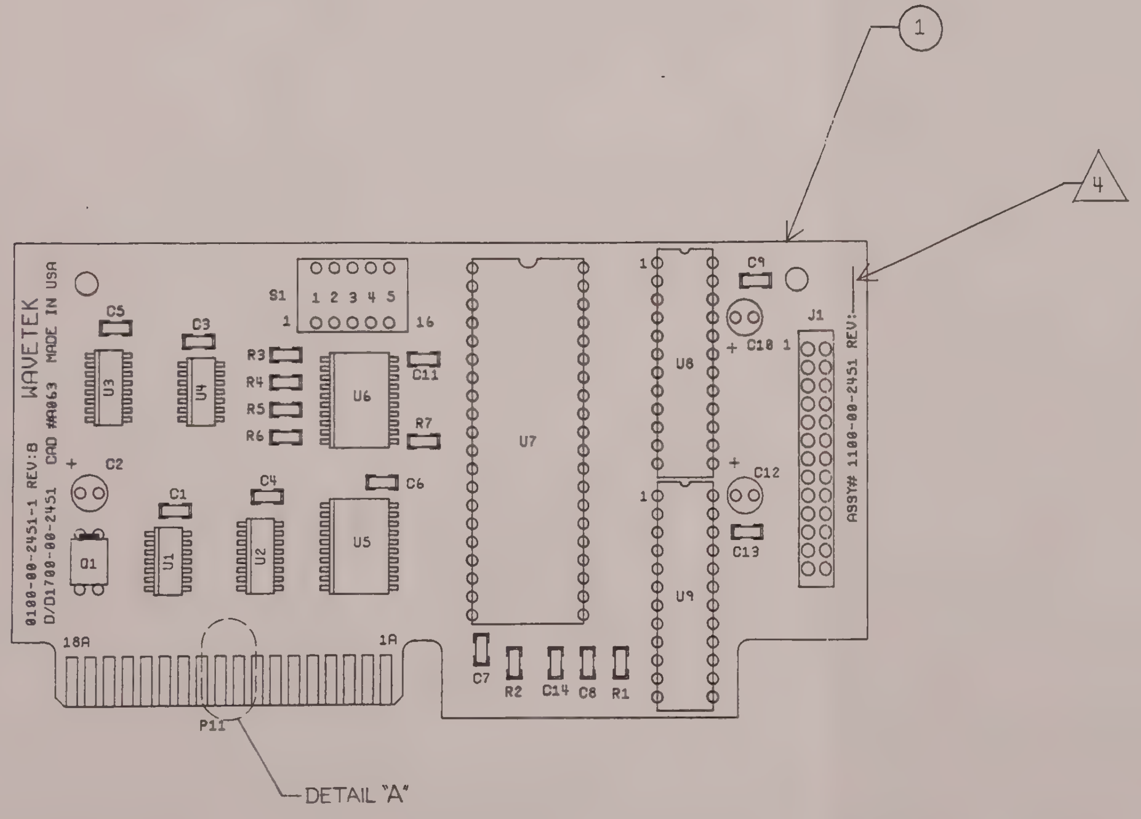
CODE IDENT 23338

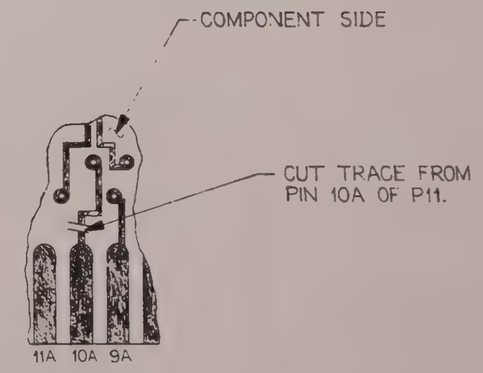
SHEET 1 OF 1

0103-00-2451 C

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

REV	ECN	BY	DATE	APP
B	FOR RELEASE	B.R	1/17/86	MB1
C	7115	AT.	10/31/96	R F.T.


1
4
WAVETEK
MADE IN USA
CAD #A063
D/D1700-00-2451
0100-00-2451-1 REV:B
ASSY# 1100-00-2451 REV:
S1
1 2 3 4 5
1
16
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
R1
R2
R3
R4
R5
R6
R7
U1
U2
U3
U4
U5
U6
U7
U8
U9
Q1
J1
18A
1A
P11
DETAIL "A"


COMPONENT SIDE
CUT TRACE FROM PIN 10A OF P11.
11A
10A
9A

DETAIL "A"
(SCALE: NONE)

4. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
3. SEE INSTRUMENT SCHEMATIC 0004-00-0040 FOR ASSEMBLY INTERCONNECTION.
2. SEE 0103-00-2451 FOR SCHEMATIC.
1. SEE PARTS LIST 1100-00-2451.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE 1/17/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	PROJ ENGR C.	4-4-86	TITLE PCA, GPIB OPTION
	RELEASE APPROV	4/4/86	
FINISH WAVETEK PROCESS —//—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO 51/52
	SCALE 2/1		DWG NO 1100-00-2451
			REV C
			CODE IDENT 23338
			SHEET 1 OF 1

1100-00-2451 C

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27089

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	DRAWING - GPIB OPT. BOARD			0103-00-2451	1
C10 C12 C2	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	3
C1 C11 C13 C14 C3 C4 C5 C6 C7 C8 C9	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	11
I	DRILL DRWG, GPIB OPT BD	1700-00-2451	WVTK	1700-00-2451	1
J1	CONN, HEADER 26 PIN/2 ROW	929836-01-13	A/P	2100-02-0156	1
R1 R2	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 100 OHM	9C12063A1000JLR	MEPCO	4703-20-1015	2
R3 R4 R5 R6 R7	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 220K OHM	9C12063A2203JLR	MEPCO	4703-20-2245	5
Q1	TRANSISTOR	IRFD9123	IR	4902-09-1230	1
S1	SWITCH PC	500-105	DUNCN	5199-00-0001	1
U8 U9	TTL, BUS XCVR, BIDIR, D	MC3447P3	MOT	8000-34-4700	2
U1	NAND, QUAD 2INP POS	74HC00D	SIG	8000-74-0041	1
U4	GATE, NOR QUAD 2 INPUT POS HCMOS SMD	74HC02D	SIG	8000-74-0241	1

WAVETEK PARTS LIST	TITLE ASSY, GPIB OPT BOARD	ASSEMBLY NO. 1100-00-2451 PAGE 1	REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U7	IEEE 488 INTERFACE ADAPTER	MC68A488P	MOT	8006-84-8801	1
U2	SMD, HEX D-FLIP FLOP, RESET, HCMOS	74HC174D	SIG	8007-41-7441	1
U6	BUF/LN DRIVER, OCTAL, TRISTATE, HCMOS, SMD	N74HC244D	SIG	8007-42-4441	1
U5	SMD, OCTAL BUSS TRANCEIVER, TRISTATE HCMOS	74HC245D	SIG	8007-42-4541	1
U3	SMD, HEX BUFFER/LINE DRIVER, TRI-STATE, HCMOS	74HC367D	SIG	8007-43-6741	1

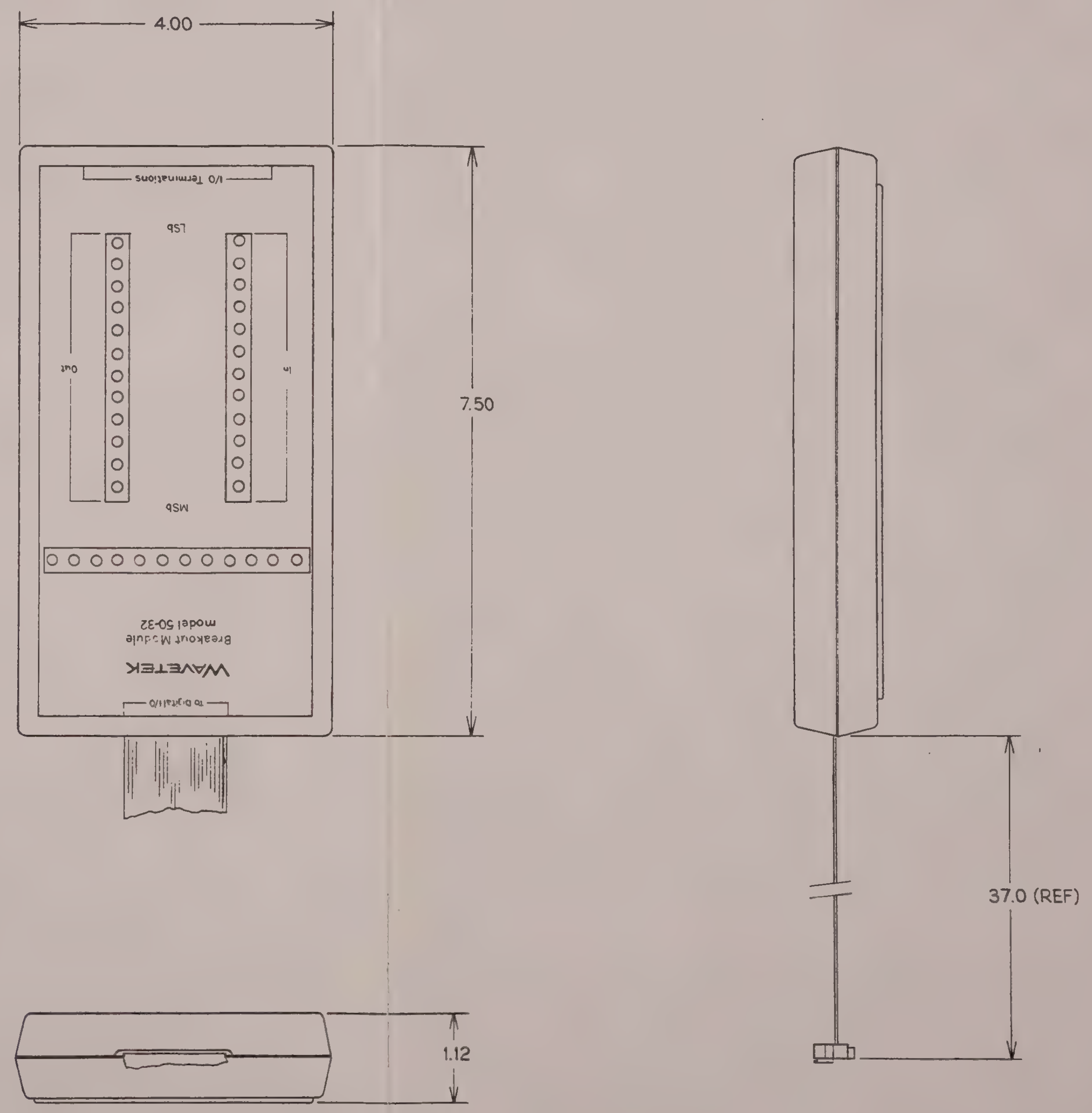
WAVETEK PARTS LIST	TITLE ASSY, GPIB OPT BOARD	ASSEMBLY NO. 1100-00-2451 PAGE 2	REV C

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA			
MATERIAL	CHECKED		TITLE PARTS LIST ASSY, GPIB OPT BOARD			
	PROJ. ENGR.					
	RELEASE APPROV.					
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D	FSCM NO. 23338	DWG. NO. 1100-00-2451	REV C
DO NOT SCALE DRAWING			SCALE OPTION 50-13		SHEET 1 OF 1	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP
A	FOR RELEASE	AT	6/30/86	NM


4.00
I/O Terminations
LSb
Out
In
MSb
model 50-32
Breakout Module
WAVETEK
to Digital I/O
7.50
37.0 (REF)
1.12

0002-00-0468 A

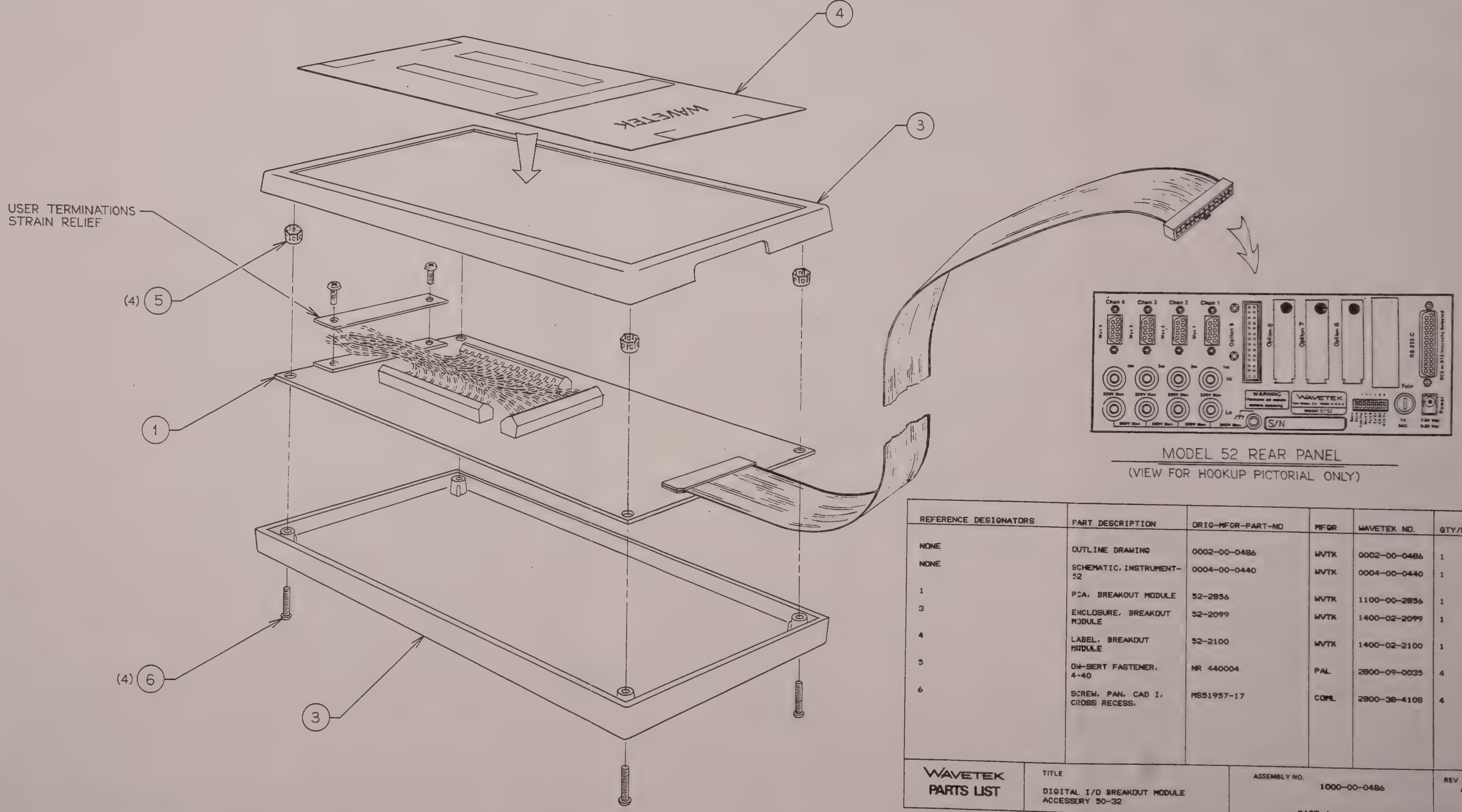
2. UNIT WEIGHT: 1.4 KG (.6 LB) NET.

1. DIMENSIONS ARE IN INCHES.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN AMY TALMADGE	DATE 6/21/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	PROJ ENGR N. E. Melk	7/1/86	TITLE OUTLINE DRAWING- BREAKOUT MODULE
	RELEASE APPROV 8/20/86		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
FINISH WAVETEK PROCESS —//—	DO NOT SCALE DWG		MODEL NO. 51/52 | DWG NO. 0002-00-0486 | REV A
	SCALE FULL		CODE IDENT 23338 | SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE	AT	7/7/86	NM


4
3
USER TERMINATIONS STRAIN RELIEF
(4) 5
1
(4) 6
3
WAVETEK
Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS 232-C
Hi
Lo
WARNING
WAVETEK
Fuse
Power
S/N

MODEL 52 REAR PANEL
(VIEW FOR HOOKUP PICTORIAL ONLY)

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	OUTLINE DRAWING	0002-00-0486	WVTK	0002-00-0486	1
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
1	PCA, BREAKOUT MODULE	52-2856	WVTK	1100-00-2856	1
3	ENCLOSURE, BREAKOUT MODULE	52-2099	WVTK	1400-02-2099	1
4	LABEL, BREAKOUT MODULE	52-2100	WVTK	1400-02-2100	1
5	ON-SERT FASTENER, 4-40	NR 440004	PAL	2800-09-0035	4
6	SCREW, PAN, CAD I, CROSS RECESS,	MS51957-17	COML	2800-38-4108	4

WAVETEK PARTS LIST	TITLE DIGITAL I/O BREAKOUT MODULE ACCESSORY 50-32	ASSEMBLY NO. 1000-00-0486 PAGE 1	REV A

SEE SEPARATE PARTS LIST 1000-00-0486

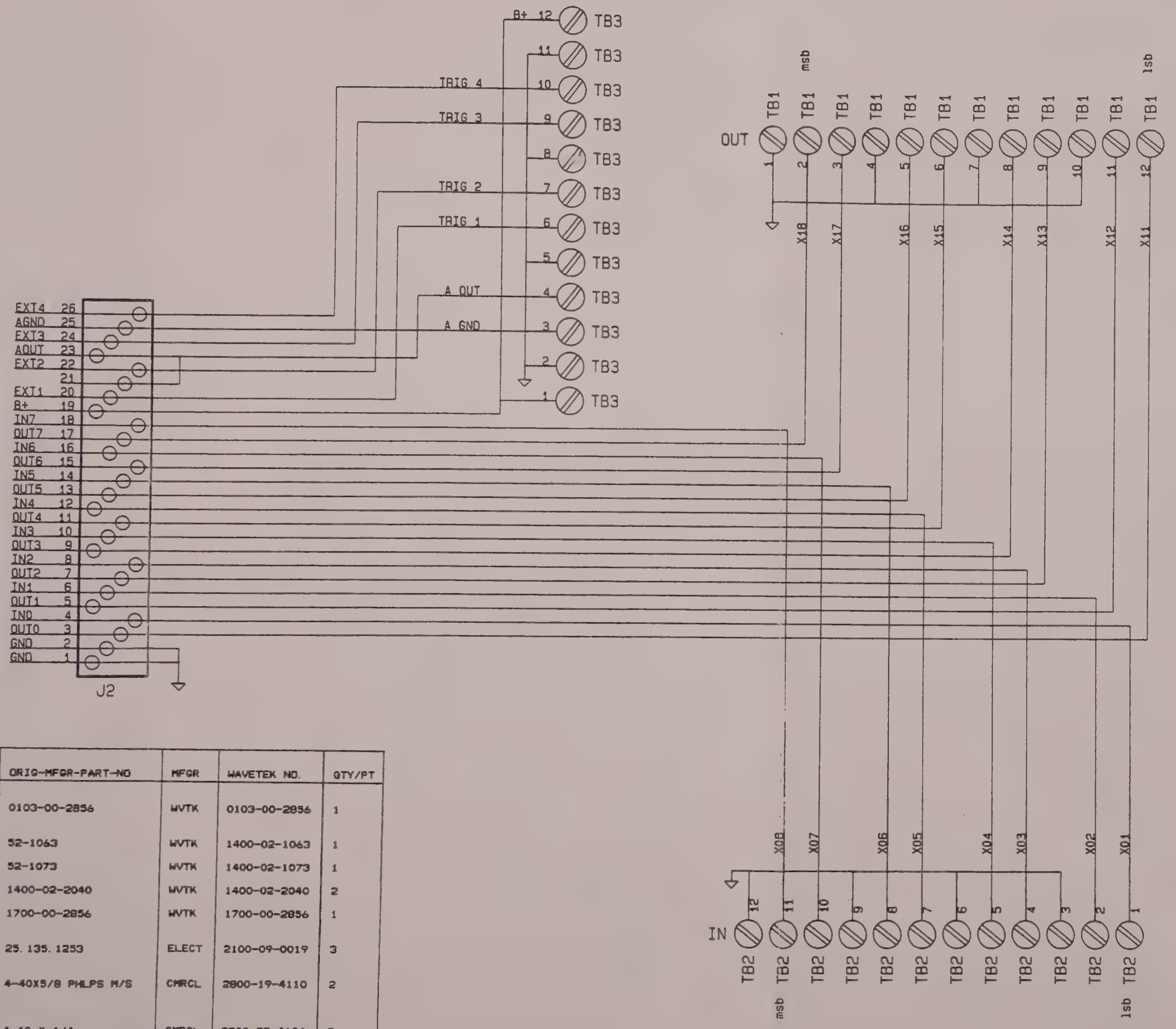
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.TALMADGE	DATE 6/4/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —/—	PROJ ENGR N. S. Mullen	7/7/86	TITLE ASSEMBLY, BREAKOUT MODULE (ACCESSORY 50-32)
	RELEASE APPROV 8/20/86		
FINISH WAVETEK PROCESS —/—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 51/52
	SCALE NONE		DWG NO. 1000-00-0486
			REV A
			CODE IDENT 23338
			SHEET 1 OF 1

1000-00-0486 A

REV	ECN	BY	DATE	APP
B	FOR RELEASE	A.T.	7/28/86	TM


B+
TRIG 4
TRIG 3
TRIG 2
TRIG 1
A OUT
A GND
TB3
12
11
10
9
8
7
6
5
4
3
2
1
EXT4 26
AGND 25
EXT3 24
AOUT 23
EXT2 22
21
EXT1 20
B+ 19
IN7 18
OUT7 17
IN6 16
OUT6 15
IN5 14
OUT5 13
IN4 12
OUT4 11
IN3 10
OUT3 9
IN2 8
OUT2 7
IN1 6
OUT1 5
IN0 4
OUT0 3
GND 2
GND 1
J2
OUT
TB1
msb
lsb
X18
X17
X16
X15
X14
X13
X12
X11
X08
X07
X06
X05
X04
X03
X02
X01
IN
TB2
msb
lsb

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, BREAKOUT MODULE BD	0103-00-2856	WVTK	0103-00-2856	1
1	BAR CLAMP, LOWER	52-1063	WVTK	1400-02-1063	1
2	BAR CLAMP, UPPER	52-1073	WVTK	1400-02-1073	1
3	RETAINER, CABLE CLAMP	1400-02-2040	WVTK	1400-02-2040	2
4	DRILL DRAWING BREAKOUT MODULE BD	1700-00-2856	WVTK	1700-00-2856	1
5	TERMINAL STRIP 12 PIN PC MOUNT	25. 135. 1253	ELECT	2100-09-0019	3
6	MACHINE SCREW, 82 DEG, F.H., PHLPS, 4-40X5/8,	4-40X5/8 PHLPS M/S	CMRCL	2800-19-4110	2
7	SCREW, SELF LOCKING, PAN CROSS RECESS	4-40 X 1/4	CMRCL	2800-23-4104	2
8	ASSY, RIBBON CABLE 38 INCH 26 PIN	6002-00-0045	WVTK	6002-00-0045	1

WAVETEK PARTS LIST	TITLE PCA, BREAKOUT MODULE	ASSEMBLY NO. 1100-00-2856 PAGE 1	REV A

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL
—/—

FINISH
WAVETEK PROCESS
—/—

DRAWN A. Tan DATE 7/30/86

PROJ ENGR 8-19-86

RELEASE APPROV 8/20/86

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
DIGITAL I/O
BREAKOUT BOARD

MODEL NO. 51/52

DWG NO. 0103-00-2856

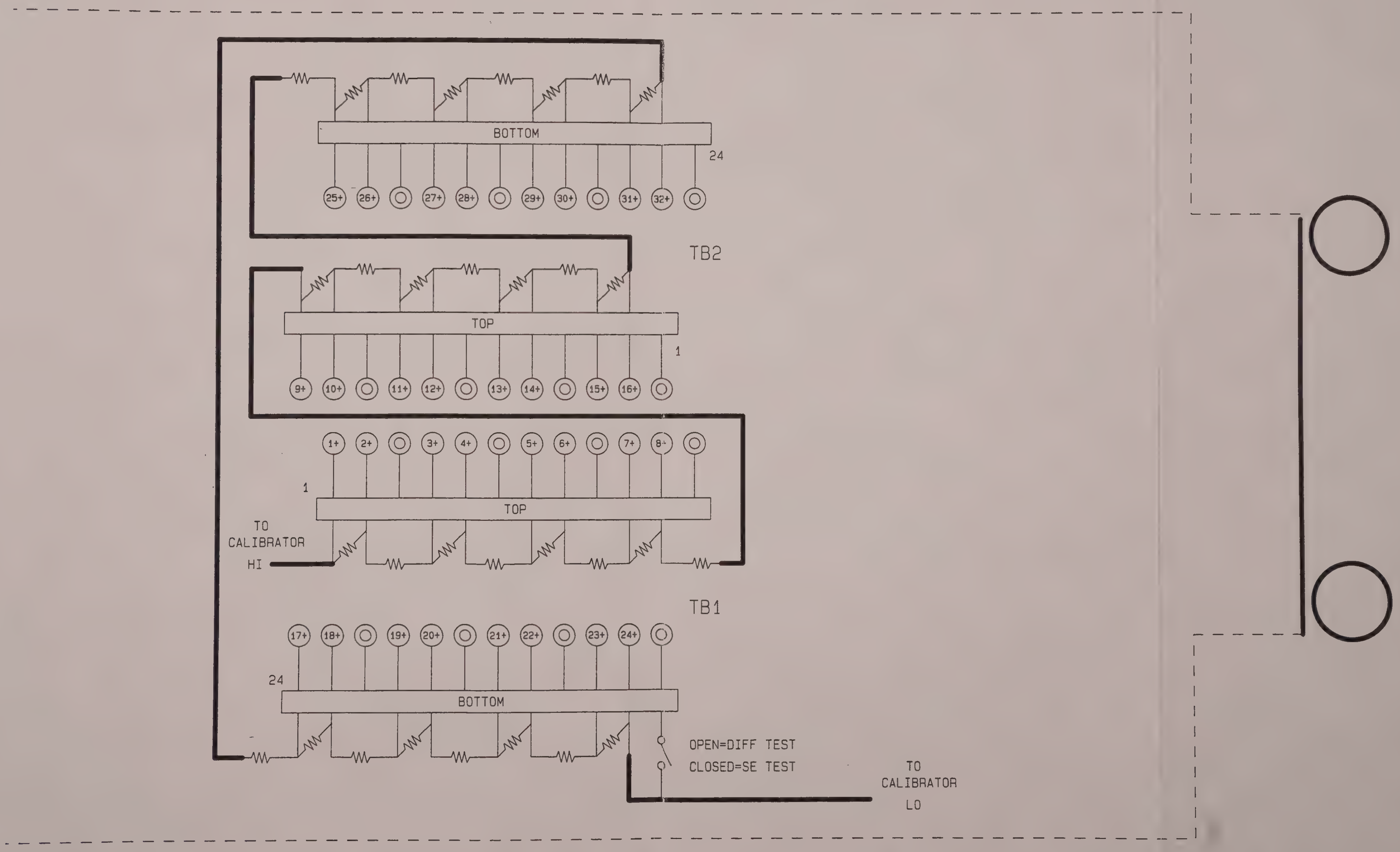
REV B

CODE IDENT 23338

SHEET 1 OF 1

0103-00-2856 B

REV	ECN	BY	DATE	APP
A	RELEASE PER ECO NO. 9103	WAE	8-31-87	


BOTTOM
24
25+
26+
27+
28+
29+
30+
31+
32+
TB2
TOP
1
9+
10+
11+
12+
13+
14+
15+
16+
1+
2+
3+
4+
5+
6+
7+
8+
1
TOP
TO CALIBRATOR HI
TB1
17+
18+
19+
20+
21+
22+
23+
24+
24
BOTTOM
OPEN=DIFF TEST
CLOSED=SE TEST
TO CALIBRATOR LO

NOTE: UNLESS OTHERWISE SPECIFIED

A
0004-00-0498

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
—
FINISH
WAVETEK PROCESS
—
DRAWN
DATE 9/1/87
PROJ ENGR C. Kauffman 9-1-87
RELEASE APPROV D.R. Taylor 9/1/87
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC,
16/32 TEST FIXTURE
MODEL NO. 53
DWG NO. 0004-00-0498
REV A
CODE IDENT 23338
SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A2708

ADHESIVE HANDLING PRECAUTIONS

1. BONDS SKIN IN SECONDS. IN CASE OF BODY CONTACT, FLUSH WITH WATER. TO SEPARATE SKIN, SOAK IN HOT SOAPY WATER. USE WITH A PEELING ACTION TO SEPARATE SKIN.
2. EYE IRRITANT. USE WITH ADEQUATE VENTILATION AND USE EYE PROTECTION. IN CASE OF EYE CONTACT, BATHE THE EYE WITH LARGE QUANTITIES OF WATER. (GET MEDICAL ATTENTION).

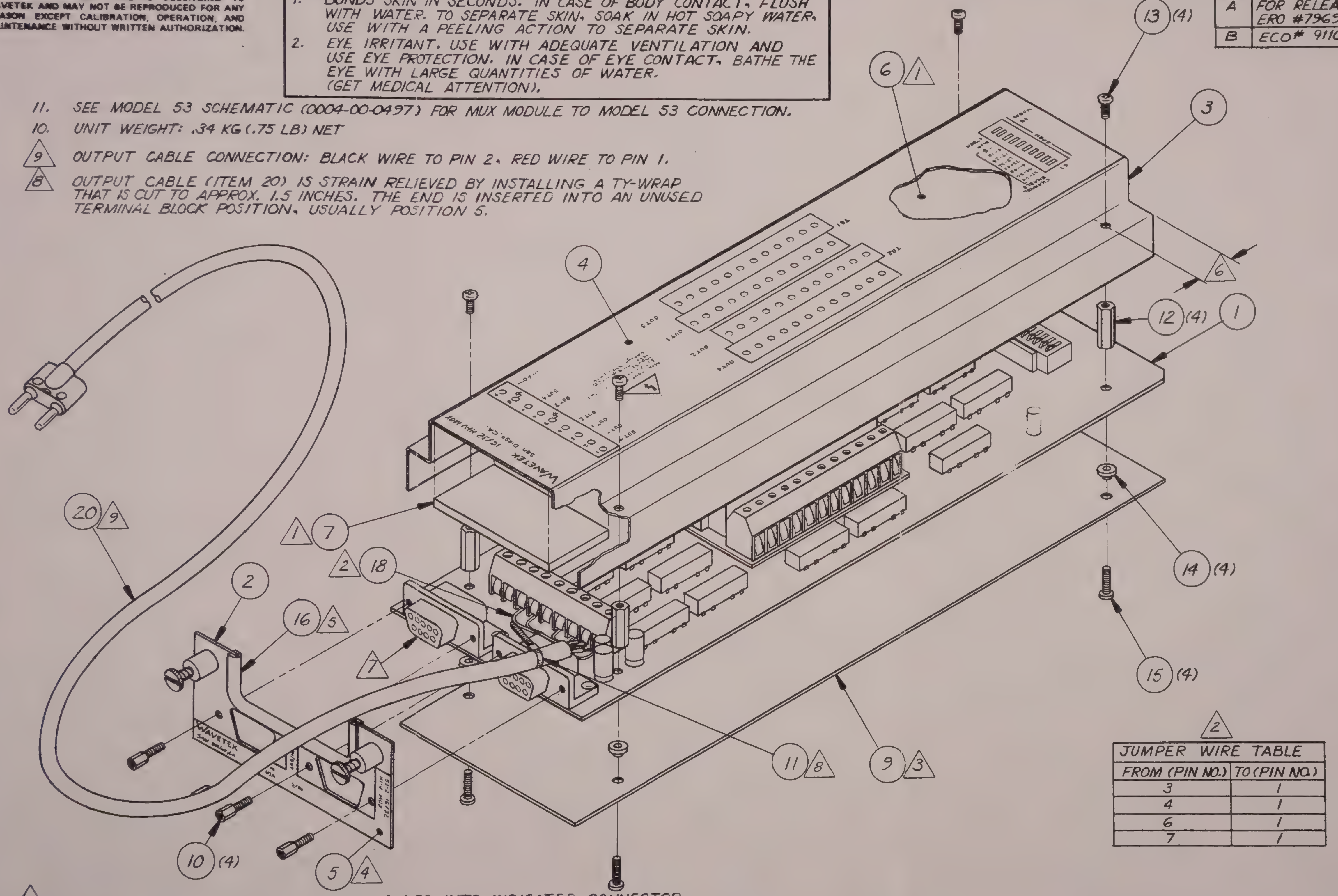
REV	ECN	BY	DATE	APP
A	FOR RELEASE ERO #7969	mag	2-17-87	NM
B	ECO# 9110	J.C. 9-29-87	9/29/87	A.R.T.

11. SEE MODEL 53 SCHEMATIC (0004-00-0497) FOR MUX MODULE TO MODEL 53 CONNECTION.

10. UNIT WEIGHT: .34 KG (.75 LB) NET

△9 OUTPUT CABLE CONNECTION: BLACK WIRE TO PIN 2, RED WIRE TO PIN 1.

△8 OUTPUT CABLE (ITEM 20) IS STRAIN RELIEVED BY INSTALLING A TY-WRAP THAT IS CUT TO APPROX. 1.5 INCHES. THE END IS INSERTED INTO AN UNUSED TERMINAL BLOCK POSITION, USUALLY POSITION 5.



△2

JUMPER WIRE TABLE	
FROM (PIN NO.)	TO (PIN NO.)
3	1
4	1
6	1
7	1

△7 CONTROL CABLE (ITEM 19) (NOT SHOWN) PLUGS INTO INDICATED CONNECTOR.

△6 SHORT END TO MOUNTING HOLE PATTERN OF COMPONENT SHIELD (ITEM 3) IS TO BE OPPOSITE OF OUTPUT CABLE (ITEM 20).

△5 MOUNT RUBBER EXTRUSION (ITEM 16) TO ITEM 2 USING ADHESIVE (ITEM 8).

△4 TYPE SERIAL NUMBER ON LABEL (ITEM 5) BEFORE INSTALLATION.

△3 COPPER SIDE OF CIRCUIT SHIELD (ITEM 9) FACES OUTWARD.

△2 JUMPER WIRE (ITEM 18) IS TO BE CUT INTO (4) 1.5 INCH LENGTHS WITH EACH END STRIPPED .25 INCH AND TINNED. CONNECT THE WIRES ACCORDING TO TABLE.

△1 INSTALL COMPONENT SHIELD INSULATOR (ITEM 6) UNDERNEATH COMPONENT SHIELD (ITEM 3) BEFORE INSTALLING NEOPRENE SPONGE TAPE (ITEM 7).

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0498

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. GROVES	DATE 2-17-87	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR C. Seagrave	3-6-87	TITLE ASSY – 16/32 MUX MODULE	
	RELEASE APPROV N. S. Nuth 3/16/87			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030			
	DO NOT SCALE DWG		MODEL NO. 53	DWG NO. 1000-00-0498 REV B
	SCALE FULL		CODE IDENT 23338	SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	CUSTOMER SPECIFICATION 53-2	0003-00-0498	WVTK	0003-00-0498	1
NONE	SCHEMATIC, 16/32 TEST FIXTURE	0004-00-0498	WVTK	0004-00-0498	1
1	PCA, 16/32 MUX	1100-00-2886	WVTK	1100-00-2886	1
2	PANEL, MODULE REAR	1400-02-2433	WVTK	1400-02-2433	1
3	SHIELD, COMPONENT	1400-02-2463	WVTK	1400-02-2463	1
4	DECAL, SHIELD, 16/32	1400-02-3070	WVTK	1400-02-3070	1
5	LABEL, S/N, 53-2 MODULE, 16/32	1400-02-3090	WVTK	1400-02-3090	1
6	INSULATOR, COMPONENT SHIELD	1400-02-3110	WVTK	1400-02-3110	1
7	CLOSED CELL NEOPRENE SPONGE TAPE, 1/8X1 WIDE	4508	SCTCH	1600-02-0014	1.88
8	ADHESIVE (CYANOACRYLATE)	85	HENKL	1600-03-0014	1
9	SHIELD, CIRCUIT	1700-00-2936	WVTK	1700-00-2936	1
10	SCREWLOCK, CONNECTOR, FEMALE, SHORT	205818-2	AMP	2100-07-0007	4
11	TY-WRAP	TY-523M	TB	2800-00-0006	1

WAVETEK
PARTS LIST
TITLE
MODEL 53-2, 16/32 MUX MODULE
ASSEMBLY NO.
1000-00-0498
REV
B
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
12	STANDOFF .625H, .250 HEX, 4-40	8835	SMITH	2800-02-0033	4
13	SCREW, SELF LOCKING, PAN CROSS RECESS	4-40 X 1/4	CMRCL	2800-23-4104	4
14	WASHER, SHOULDER, .250 OD X .116 ID	5607-153	SEBTM	2800-27-0009	4
15	SCREW, SELF-LOCK, PH, 4-40 X 3/8	4-40 X 3/8 PH, SL	CMRCL	2800-56-9106	4
16	EXTRU, RUBBER, U CHNL, 1/16 INSIDE, 1/8 OUTSIDE	924	LESIG	3200-06-0079	3
17				3300-01-0021	1
18	WIRE, HU, 24GA	H0103011 (WHT)	JUDD	6000-42-4009	.5
19	CABLE, CONTROL 53	6002-00-0046	WVTK	6002-00-0046	1
20	OUTPUT CABLE ASSY	6009-90-0039	WVTK	6009-90-0039	1

WAVETEK
PARTS LIST
TITLE
MODEL 53-2, 16/32 MUX MODULE
ASSEMBLY NO.
1000-00-0498
REV
B
PAGE 2

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

DRAWN	DATE
CHECKED	
PROJ. ENGR.	
RELEASE APPROV.	

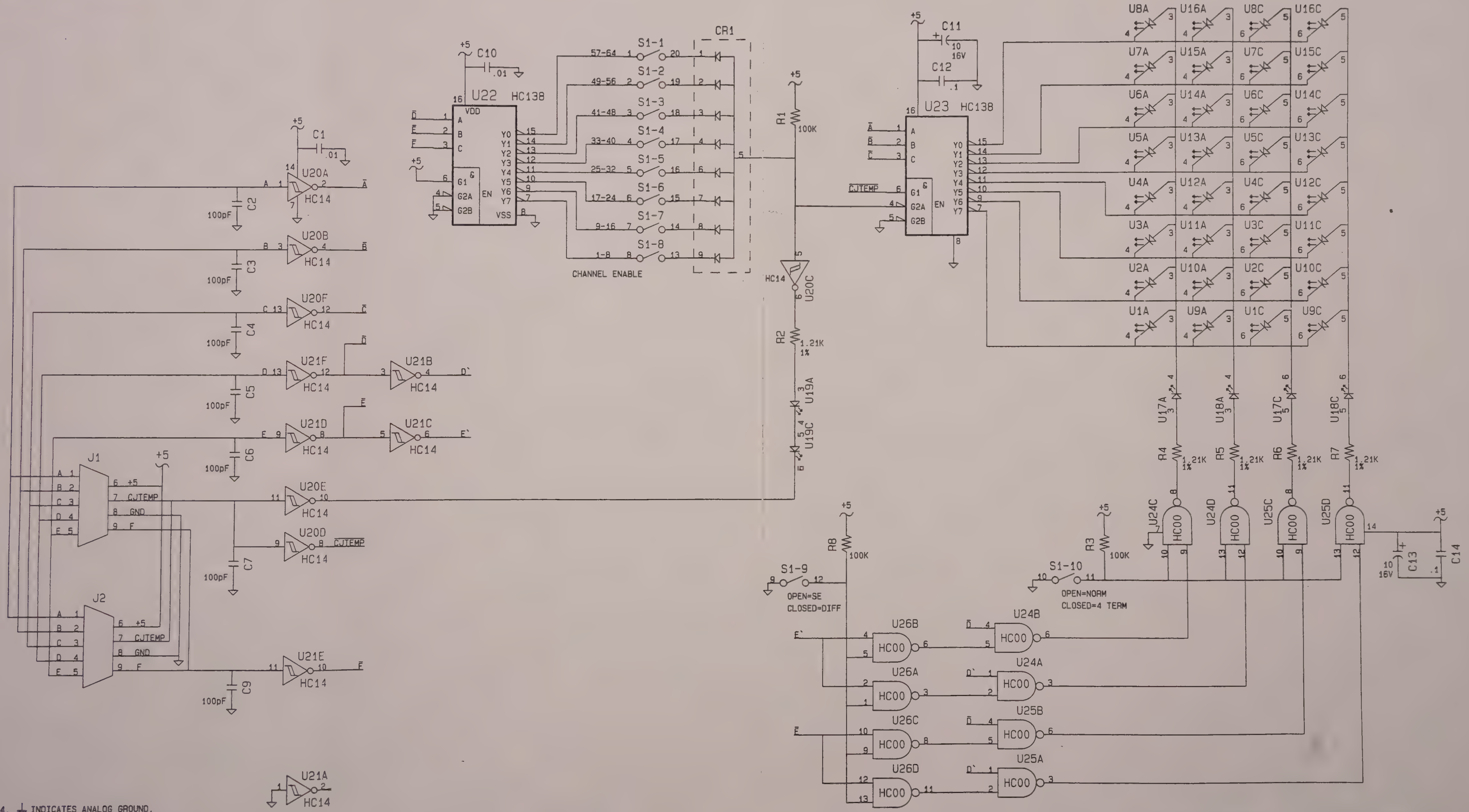
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
MODEL 53-2,
16/32 MUX MODULE

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1000-00-0498	B

SCALE
MODEL 53-2
SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE PER ERO # 7066			


C10 .01
U22 HC138
S1-1 57-64
S1-2 49-56
S1-3 41-48
S1-4 33-40
S1-5 25-32
S1-6 17-24
S1-7 9-16
S1-8 1-8
CHANNEL ENABLE
CR1
R1 100K
HC14 U20C
R2 1.21K 1%
U19A
U19C
C11 10 16V
C12 .1
U23 HC138
CJTEMP
U8A U16A U8C U16C
U7A U15A U7C U15C
U6A U14A U6C U14C
U5A U13A U5C U13C
U4A U12A U4C U12C
U3A U11A U3C U11C
U2A U10A U2C U10C
U1A U9A U1C U9C
U17A U18A U17C U18C
R4 1.21K 1%
R5 1.21K 1%
R6 1.21K 1%
R7 1.21K 1%
U24C U24D U25C U25D HC00
C13 10 16V
C14 .1
C1 .01
U20A HC14
C2 100pF
U20B HC14
C3 100pF
U20F HC14
C4 100pF
U21F HC14
U21B HC14
C5 100pF
U21D HC14
U21C HC14
C6 100pF
J1
+5
CJTEMP
GND
U20E HC14
U20D HC14
C7 100pF
J2
U21E HC14
C9 100pF
U21A HC14
R8 100K
S1-9
OPEN=SE
CLOSED=DIFF
R3 100K
S1-10
OPEN=NORM
CLOSED=4 TERM
U26B U24B
U26A U24A
U26C U25B
U26D U25A
HC00

4. ↓ INDICATES ANALOG GROUND.
   ⏚ INDICATES DIGITAL GROUND.

3. CAPACITORS VALUED IN MICROFARADS (uF).

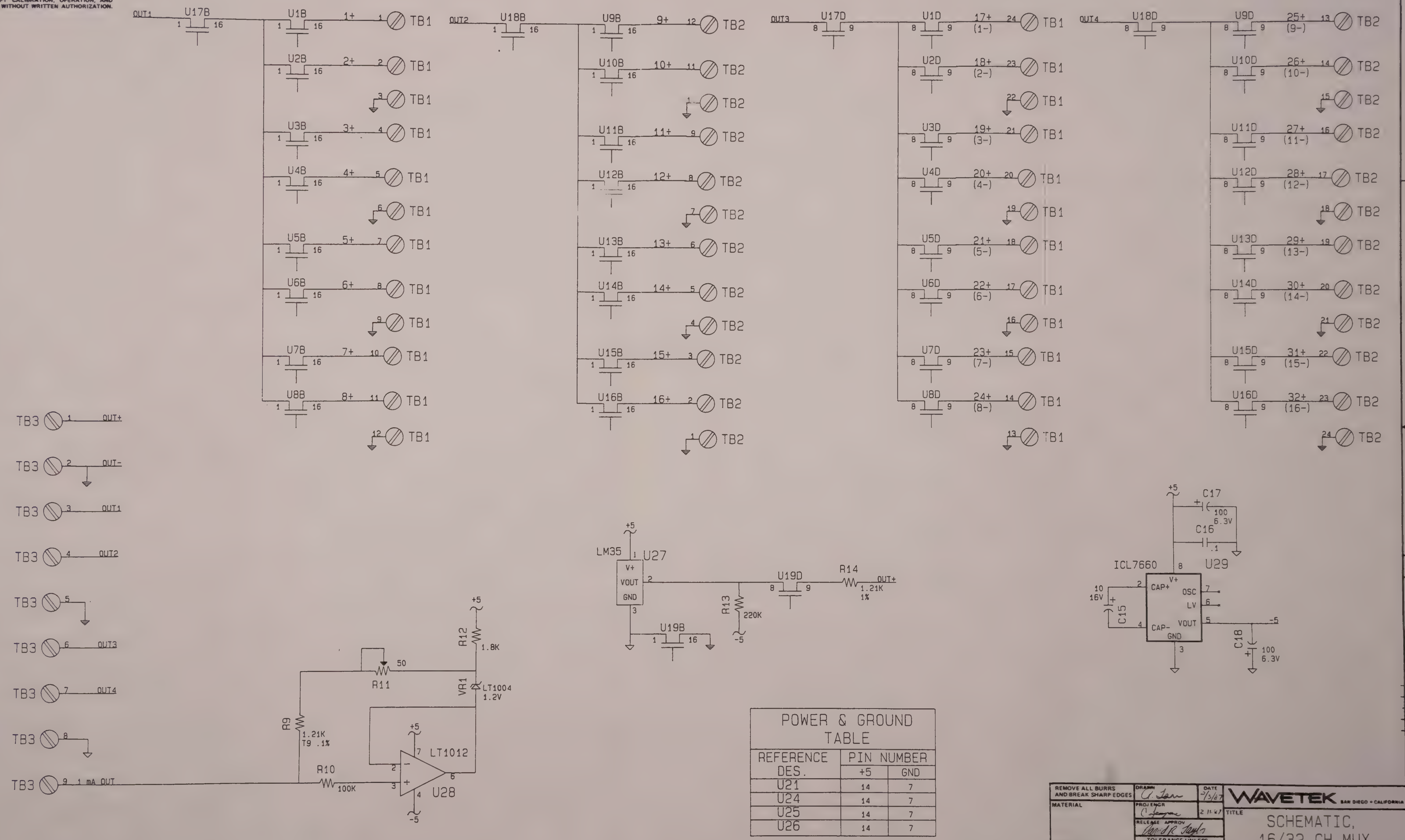
2. RESISTORS VALUED IN OHMS, 1/8W.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0497.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TARR	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR C Seagrave	2-19-87	TITLE SCHEMATIC, 16/32 CH MUX
	RELEASE APPROV JK Taylor		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 53 / DWG NO. 0103-00-2886 / REV A
	SCALE NONE		CODE IDENT 23338 / SHEET 1 OF 2

REV	ECN	BY	DATE	APP


OUT1
U17B
U1B 1+ 1 TB1
U2B 2+ 2 TB1
3 TB1
U3B 3+ 4 TB1
U4B 4+ 5 TB1
6 TB1
U5B 5+ 7 TB1
U6B 6+ 8 TB1
9 TB1
U7B 7+ 10 TB1
U8B 8+ 11 TB1
12 TB1
OUT2
U18B
U9B 9+ 12 TB2
U10B 10+ 11 TB2
1 TB2
U11B 11+ 9 TB2
U12B 12+ 8 TB2
7 TB2
U13B 13+ 6 TB2
U14B 14+ 5 TB2
4 TB2
U15B 15+ 3 TB2
U16B 16+ 2 TB2
1 TB2
OUT3
U17D
U1D 17+ (1-) 24 TB1
U2D 18+ (2-) 23 TB1
22 TB1
U3D 19+ (3-) 21 TB1
U4D 20+ (4-) 20 TB1
19 TB1
U5D 21+ (5-) 18 TB1
U6D 22+ (6-) 17 TB1
16 TB1
U7D 23+ (7-) 15 TB1
U8D 24+ (8-) 14 TB1
13 TB1
OUT4
U18D
U9D 25+ (9-) 13 TB2
U10D 26+ (10-) 14 TB2
15 TB2
U11D 27+ (11-) 16 TB2
U12D 28+ (12-) 17 TB2
18 TB2
U13D 29+ (13-) 19 TB2
U14D 30+ (14-) 20 TB2
21 TB2
U15D 31+ (15-) 22 TB2
U16D 32+ (16-) 23 TB2
24 TB2
TB3 1 OUT+
TB3 2 OUT-
TB3 3 OUT1
TB3 4 OUT2
TB3 5
TB3 6 OUT3
TB3 7 OUT4
TB3 8
TB3 9 1 mA OUT
+5
R12 1.8K
50
R11
VR1 LT1004 1.2V
R9 1.21K T9 .1%
R10 100K
LT1012
U28
+5
-5
+5
LM35 U27
V+
VOUT
GND
U19D
R14 1.21K 1%
OUT+
R13 220K
-5
U19B
+5
C17 100 6.3V
C16 .1
ICL7660 U29
CAP+
V+
OSC
LV
CAP-
VOUT
GND
10 16V C15
-5
C18 100 6.3V

POWER & GROUND TABLE

REFERENCE DES.	PIN NUMBER	
	+5	GND
U21	14	7
U24	14	7
U25	14	7
U26	14	7

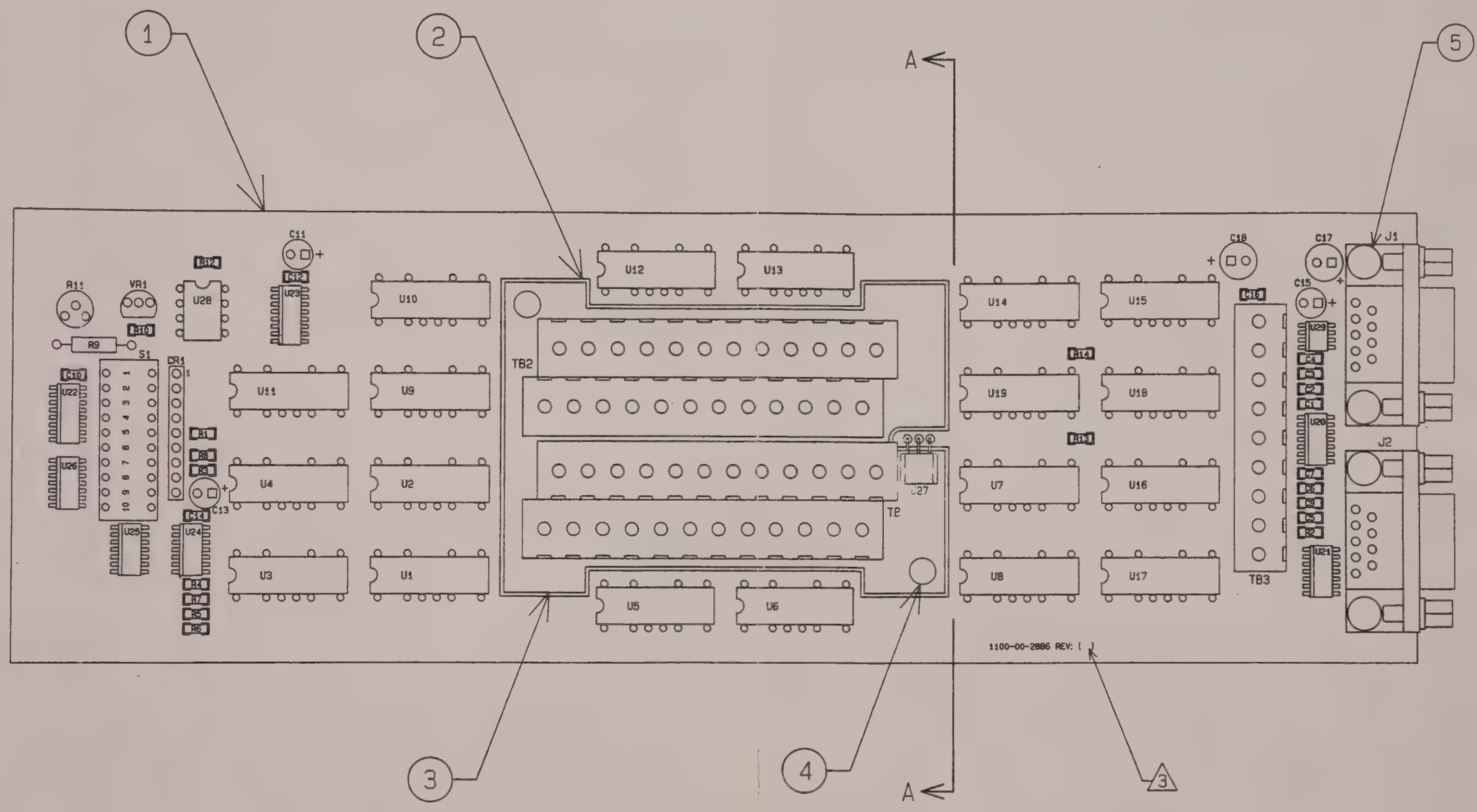
NOTE UNLESS OTHERWISE SPECIFIED

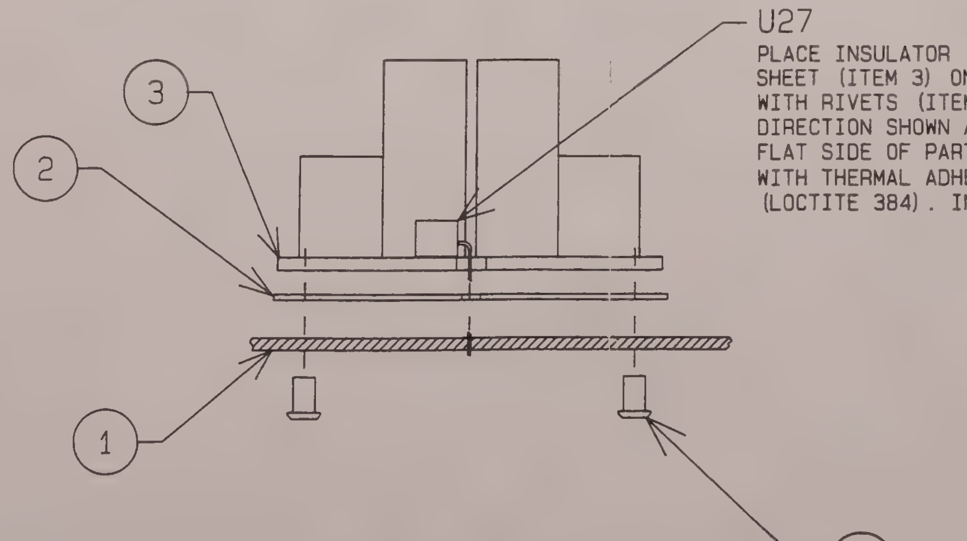
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN C. Tan DATE 2/3/87
PROJ ENGR 2 11 87
RELEASE APPROV David R Taylor
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE SCHEMATIC, 16/32 CH MUX
MODEL NO. 53
DWG NO. 0103-00-2886
REV A
CODE IDENT 23338
SHEET 2 OF 2

0103-00-2886 A

BISHOP GRAPHICS/ACCUPRESS REORDER NO A27086

REV	ECN	BY	DATE	APP
A	FOR RELEASE PER ERO #7966	JT	2/10/87	
B	·ECO # 9065	A.C. 8-26-87	8/26/87	ART
C	ECO # 9066	A.C. 9-8-87	9-9-87	ART


1
2
A
5
C11
C18
C17
J1
R11
VR1
R12
U28
C12
U23
U10
U12
U13
U14
U15
C16
C15
R10
R9
S1
CR1
C10
U22
TB2
U11
U9
U19
U16
U29
C4
C3
C2
C1
U20
J2
U26
R1
R8
R3
C13
U4
U2
U27
U7
U16
C7
C6
C9
C5
C8
C14
U25
U24
TP
U21
U3
U1
U8
U17
TB3
R4
R7
R5
R6
U5
U6
1100-00-2886 REV: ( )
3
4
A
3



PLACE INSULATOR (ITEM 2) AND ISOTHERMAL SHEET (ITEM 3) ON PC BOARD AND FASTEN WITH RIVETS (ITEM 4). INSTALL U27 IN DIRECTION SHOWN AND FOLD DOWN TOWARD FLAT SIDE OF PART. ATTACH U27 TO ITEM 3 WITH THERMAL ADHESIVE 1600-00-0019 (LOCTITE 384). INSTALL TB1 AND TB2.

SECTION A-A

(ROTATED 90° CW)
(EXPLODED FOR CLARITY)

5. TRIM COMPONENT LEADS TO A MAXIMUM HEIGHT OF .060 FROM BOARD SURFACE.
4. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
△3 MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0947.
1. SEE 0103-00-2886 FOR SCHEMATIC.

NOTE: UNLESS OTHERWISE SPECIFIED

1100-00-2886 C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T. / A.L.T.	DATE 2/10/87	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	PROJ ENGR	2-11-87	TITLE PCA, 16/32 MUX
	RELEASE APPROV		
FINISH WAVETEK PROCESS —//—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 53 · DWG NO. 1100-00-2886 · REV C
	SCALE 2/1		CODE IDENT 23338 · SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	GTY/PT
NONE	SCHEMATIC, 16/32 CHANNEL MUX	0103-00-2886	WVTK	0103-00-2886	1
3	SHEET, ISOTHERMAL, 16/32 MUX	1400-02-2513	WVTK	1400-02-2513	1
2	INSULATOR, ISOTHERMAL SHEET, 16/32 MUX	1400-02-2520	WVTK	1400-02-2520	1
C11 C13 C15	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	3
C17 C18	CAP, ELECT, 100UF, 6.3V	NRWA101M6.3	NIC	1500-31-0100	2
C1 C10	SMD, CAP, CER, 25U, 50V, .01UF	C1206C103M5RAC	KEMET	1500-80-0008	2
C2 C3 C4 C5 C6 C7 C9	SMD, CAP, CER, 2%, 50V, NPO 100PF	C1206C101J2GAC	KEMET	1500-81-0101	7
C12 C14 C16	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	3
1	16/32 CHANNEL MUX BD	1700-00-2886	WVTK	1700-00-2886	1
J1 J2	CONNECTOR, RT ANGLE PC MOUNT, 9 PIN	745394-2	AMP	2100-02-0200	2
TB3	TERMINAL STRIP, 9 PIN, PC MOUNT	20.872.009	WECO	2100-09-0024	1
TB1 TB2	TERMINAL STRIP, 24 PIN, TIERED	21.872.912	WECO	2100-09-0027	2

WAVETEK PARTS LIST
TITLE PCA, 16/32 MUX
ASSEMBLY NO. 1100-00-2886
REV C
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	GTY/PT
	[illegible]				
U27	IC, CENTIGRADE TEMP SENSOR	LM35DZ	NAT	7000-00-3500	1
VR1	MICROPOWER VOLT REF, 1.2V, +-MV INITIAL ACC	LT1004CZ-1.2	LINTE	7000-10-0400	1
U28	IC, PICOAMP INPUT MIC VOLT OFFSET LOW NOISE	LT1012CN8	LINTE	7000-10-1200	1
U29	SMD, DC TO DC CONVERTER, CMOS, 300MW	ICL7660CBA	INTSL	7000-76-6041	1
U24 U25 U26	NAND, QUAD 2INP POS	74HC00D	SIG	8000-74-0041	3
U20 U21	SMD, HEX SCHMITT TRIGGER/INVERTER, HCMOS	74HC14D	SIG	8000-74-1441	2
U22 U23	SMD, 1 OF 8 DECODER/DEMUX, HCMOS	74HC138D	SIG	8007-41-3841	2

WAVETEK PARTS LIST
TITLE PCA, 16/32 MUX
ASSEMBLY NO. 1100-00-2886
REV C
PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	GTY/PT
4	RIVET, ALUM 1/8X1/4L .126-.187	1125-0408	AVDEL	2800-12-0043	2
5	PLASTIC RIVET	231-080551-05-0101	FASTX	2800-60-0008	4
U1 U10 U11 U12 U13 U14 U15 U16 U17 U18 U19 U2 U3 U4 U5 U6 U7 U8 U9	RELAY, PHOTO VOLTAIC, BOSFET, 16 PIN DIP	PVR3301	IR	4500-01-0001	19
R11	POT, TRIM, 50	3329H-1-500	BOURN	4600-05-0001	1
R1 R10 R3 R8	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 100K OHM	MCR18EZH104JW5%	ROHM	4703-20-1045	4
R12	RES, SMD GP 1/8 LONG 200PPM 5% 1.8K OHM	MCR18EZH182JW5%	ROHM	4703-20-1825	1
R13	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 220K OHM	9C12063A2203JLR	MEPCO	4703-20-2245	1
R14 R2 R4 R5 R6 R7	RES, SMD 1/8 LONG 100PPM 1% 1.21K OHM	0108-00-2765	REF SPE	4703-21-2111	6
R9	RES, MF, 1/8W, .1%, T-9, 1.21K	CMF-551211BT-9	DALE	4799-00-0143	1
CR1	DIODE, SIP, ULTRA HIGH SPEED SWITCHING	DAP801	ROHM	4805-02-0801	1
S1	SWITCH, DIP, SPST	76SB10	GRHL	5199-00-0009	1

WAVETEK PARTS LIST
TITLE PCA, 16/32 MUX
ASSEMBLY NO. 1100-00-2886
REV C
PAGE 2

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
PCA 16/32 MUX
SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-2886
REV C
SCALE OPTION 53-2
SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C1 C10	CAP, SMD CER 25U 50V .01UF	C1206C103M5RAC	KEMET	1500-80-0008	2
C2 C3 C4 C5 C6 C7 C9	CAP, SMD CER 5% 50V NPO 100PF	C1206C101J20AC	KEMET	1500-81-0101	7
C12 C14 C16	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	3
NONE	16/32 CHANNEL MUX BD	1700-00-2886	WVTK	1700-00-2886	1
R1 R10 R3 R8	RES, SMD GP 1/8 LONG 200PPM 5% 100K OHM	MCR18EZH104JW5%	ROHM	4703-20-1045	4
R12	RES, SMD GP 1/8 LONG 200PPM 5% 1.8K OHM	MCR18EZH182JW5%	ROHM	4703-20-1825	1
R13	RES, SMD GP 1/8 LONG 200PPM 5% 220K OHM	9C12063A2203JLR	MEPCO	4703-20-2245	1
R14 R2 R4 R5 R6 R7	RES, SMD 1/8 LONG 100PPM 1% 1.21K OHM	0108-00-2765	REF SPE	4703-21-2111	6
U29	CONVERTER, DC TO DC, CMOS, 300MW, SMD	ICL7660CBA	INTSL	7000-76-6041	1
U24 U25 U26	GATE, NAND, QUAD, 2INP POS, SMD	74HC00D	SIG	8000-74-0041	3
U20 U21	HEX SCHMITT TRIGGER/INVERTER, HCMOS, SMD	74HC14D	SIG	8000-74-1441	2

WAVETEK PARTS LIST	TITLE ASSY, PCA 16/32 MUX (SMD)	ASSEMBLY NO. 1208-00-2953 PAGE 1	REV A

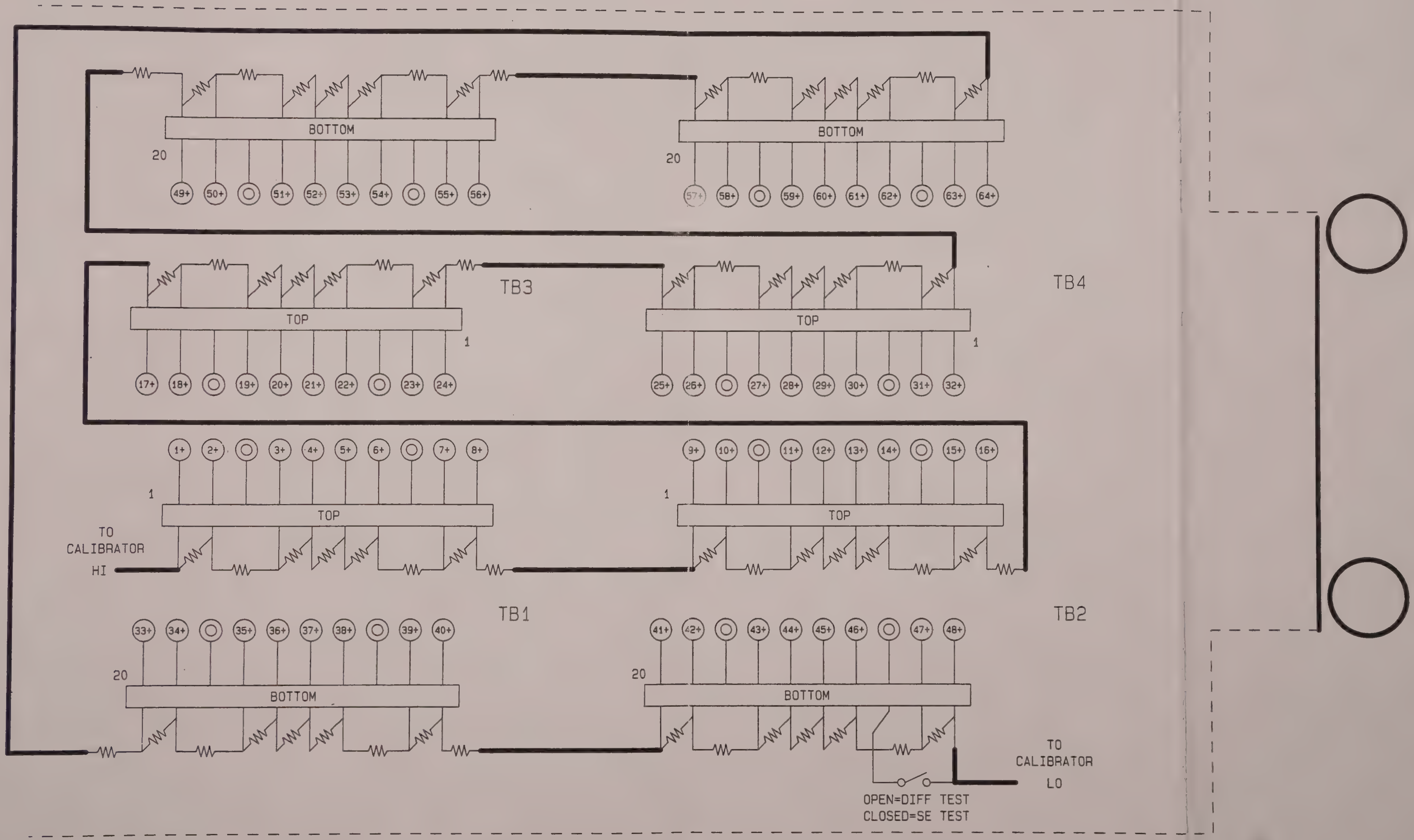
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U22 U23	DECODER/DEMUX, 1 OF 8, HCMOS, SMD	74HC138D	SIG	8007-41-3841	2

WAVETEK PARTS LIST	TITLE ASSY, PCA 16/32 MUX (SMD)	ASSEMBLY NO. 1208-00-2953 PAGE 2	REV A

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE PARTS LIST ASSY, PCA 16/32 MUX (SMD)
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1208-00-2953 · REV A
DO NOT SCALE DRAWING			SCALE · MODEL 53 · SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	RELEASE PER EPO NO. 9103	MAG	8-31-87	


BOTTOM
20
49+
50+
51+
52+
53+
54+
55+
56+
BOTTOM
20
57+
58+
59+
60+
61+
62+
63+
64+
TB3
TOP
1
17+
18+
19+
20+
21+
22+
23+
24+
TB4
TOP
1
25+
26+
27+
28+
29+
30+
31+
32+
1+
2+
3+
4+
5+
6+
7+
8+
1
TOP
9+
10+
11+
12+
13+
14+
15+
16+
1
TOP
TO
CALIBRATOR
HI
TB1
TB2
33+
34+
35+
36+
37+
38+
39+
40+
20
BOTTOM
41+
42+
43+
44+
45+
46+
47+
48+
20
BOTTOM
TO
CALIBRATOR
LO
OPEN=DIFF TEST
CLOSED=SE TEST

0004-00-0499
A

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL
—//—

FINISH
WAVETEK PROCESS
—//—

DRAWN
DATE 9/1/87

PROJ ENGR C. [illegible] 9-1-87

RELEASE APPROV [illegible] 9/1/87

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ± .010 ANGLES ±1°
.XX ± .030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
32/64 TEST FIXTURE

MODEL NO. 53
DWG NO. 0004-00-0499
REV A
CODE IDENT 23338
SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS RECORDER NO A27096

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

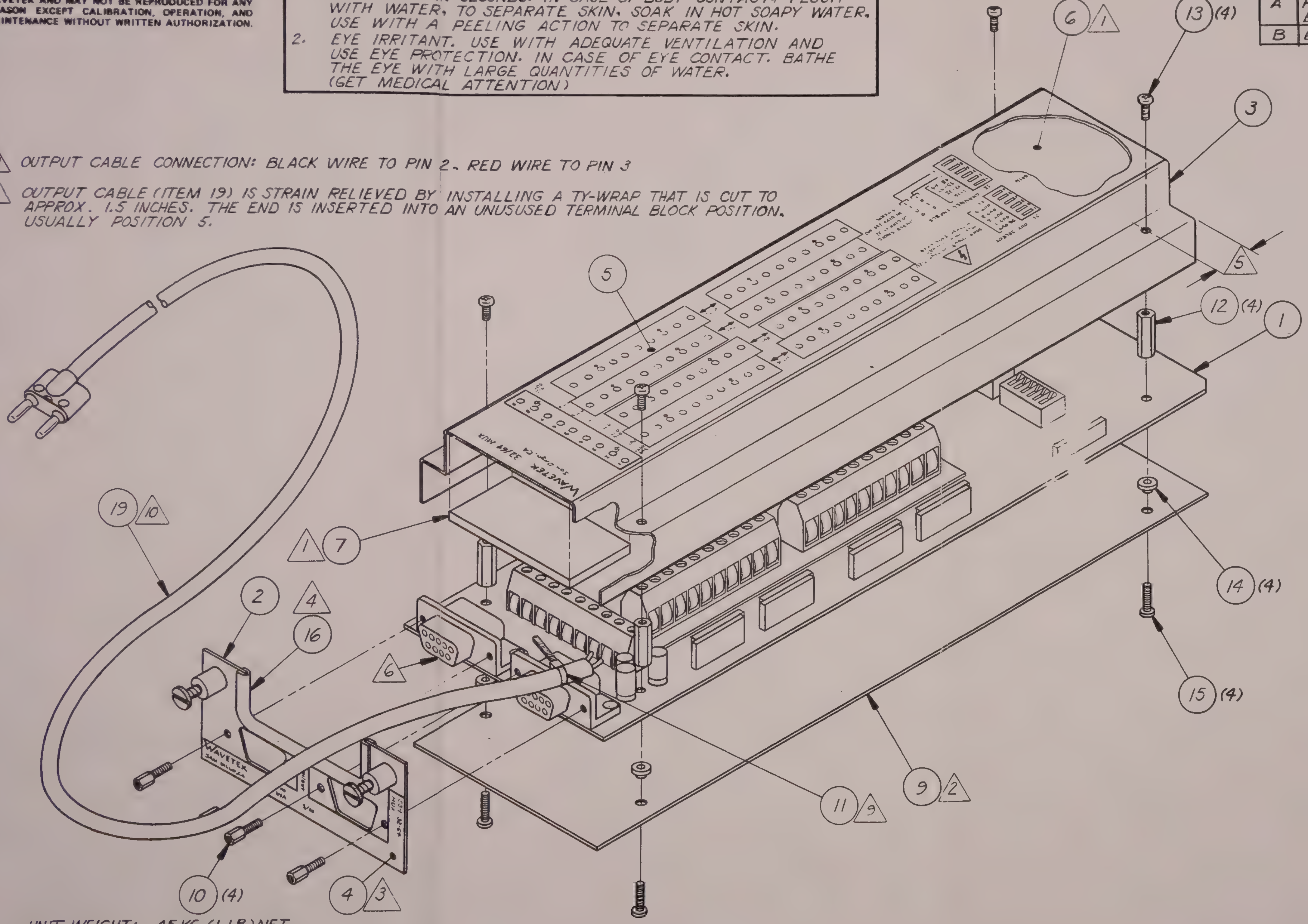
ADHESIVE HANDLING PRECAUTIONS

1. BONDS SKIN IN SECONDS. IN CASE OF BODY CONTACT, FLUSH WITH WATER, TO SEPARATE SKIN, SOAK IN HOT SOAPY WATER. USE WITH A PEELING ACTION TO SEPARATE SKIN.
2. EYE IRRITANT. USE WITH ADEQUATE VENTILATION AND USE EYE PROTECTION. IN CASE OF EYE CONTACT. BATHE THE EYE WITH LARGE QUANTITIES OF WATER. (GET MEDICAL ATTENTION)

REV	ECN	BY	DATE	APP
A	FOR RELEASE ERO #7969	mag	2-17-87	nm
B	ECO # 9111	A. C. 9-29-87	9/28/87	A.R.T.

△10 OUTPUT CABLE CONNECTION: BLACK WIRE TO PIN 2, RED WIRE TO PIN 3

△9 OUTPUT CABLE (ITEM 19) IS STRAIN RELIEVED BY INSTALLING A TY-WRAP THAT IS CUT TO APPROX. 1.5 INCHES. THE END IS INSERTED INTO AN UNUSUSED TERMINAL BLOCK POSITION, USUALLY POSITION 5.



8. UNIT WEIGHT: .45 KG (1 LB) NET
7. SEE MODEL 53 SCHEMATIC (0004-00-0497) FOR MUX MODULE TO MODEL 53 CONNECTION.

△6 CONTROL CABLE (ITEM 18) (NOT SHOWN) PLUGS INTO INDICATED CONNECTOR.

△5 SHORT END TO MOUNTING HOLE PATTERN OF COMPONENT SHIELD (ITEM 3) IS TO BE OPPOSITE OF OUTPUT CABLE (ITEM 19).

△4 MOUNT RUBBER EXTRUSION (ITEM 16) TO ITEM 2 USING ADHESIVE (ITEM 8).

△3 TYPE SERIAL NUMBER ON LABEL (ITEM 4) BEFORE INSTALLATION.

△2 COPPER SIDE OF CIRCUIT SHIELD (ITEM 9) FACES OUTWARD.

△1 INSTALL COMPONENT SHIELD INSULATOR (ITEM 6) UNDERNEATH COMPONENT SHIELD (ITEM 3) BEFORE INSTALLING NEOPRENE SPONGE TAPE (ITEM 7).

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0499

REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN M. GROVES
DATE 2-17-87
WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL
PROJ ENGR C. Seagrave 3-6-87
RELEASE APPROV N. E. Mell 3/16/87
TITLE ASSY-32/64 MUX MODULE
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
FINISH WAVETEK PROCESS
DO NOT SCALE DWG
SCALE FULL
MODEL NO. 53
DWG NO. 1000-00-0499
REV B
CODE IDENT 23338
SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	CUSTOMER SPECIFICATION 53-1	0003-00-0499	WVTK	0003-00-0499	1
NONE	SCHEMATIC, 32/64 TEST FIXTURE	0004-00-0499	WVTK	0004-00-0499	1
1	PCA, 32/64 MUX	1100-00-2877	WVTK	1100-00-2877	1
2	PANEL, MODULE REAR	1400-02-2433	WVTK	1400-02-2433	1
3	SHIELD, COMPONENT	1400-02-2463	WVTK	1400-02-2463	1
4	LABEL, S/N, 53-1 MODULE, 32/64	1400-02-3080	WVTK	1400-02-3080	1
5	DECAL, SHIELD, 32/64	1400-02-3100	WVTK	1400-02-3100	1
6	INSULATOR, COMPONENT SHIELD	1400-02-3110	WVTK	1400-02-3110	1
7	CLOSED CELL NEOPRENE SPONGE TAPE, 1/8X1 WIDE	4508	SCTCH	1600-02-0014	1.88
8	ADHESIVE (CYANOACRYLATE)	85	HENKL	1600-03-0014	1
9	SHIELD, CIRCUIT	1700-00-2936	WVTK	1700-00-2936	1
10	SCREWLOCK, CONNECTOR, FEMALE, SHORT	205818-2	AMP	2100-07-0007	4
11	TY-WRAP	TY-523M	TB	2800-00-0006	1

WAVETEK PARTS LIST
TITLE ASSY, 32/64 MUX MODULE
ASSEMBLY NO. 1000-00-0499
REV B
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
12	STANDOFF .625H, .250 HEX, 4-40	8835	SMITH	2800-02-0033	4
13	SCREW, SELF LOCKING, PAN CROSS RECESS	4-40 X 1/4	CMRCL	2800-23-4104	4
14	WASHER, SHOULDER, .250 OD X .116 ID	3607-153	SESTM	2800-27-0009	4
15	SCREW, SELF-LOCK, PH, 4-40 X 3/8	4-40 X 3/8 PH, SL	CMRCL	2800-56-9106	4
16	EXTRU, RUBBER, U CHNL, 1/16 INSIDE, 1/8 OUTSIDE	724	LEBIG	3200-06-0079	3
17				3300-01-0021	1
18	CABLE, CONTROL 53	6002-00-0046	WVTK	6002-00-0046	1
19	OUTPUT CABLE ASSY	6009-90-0039	WVTK	6009-90-0039	1

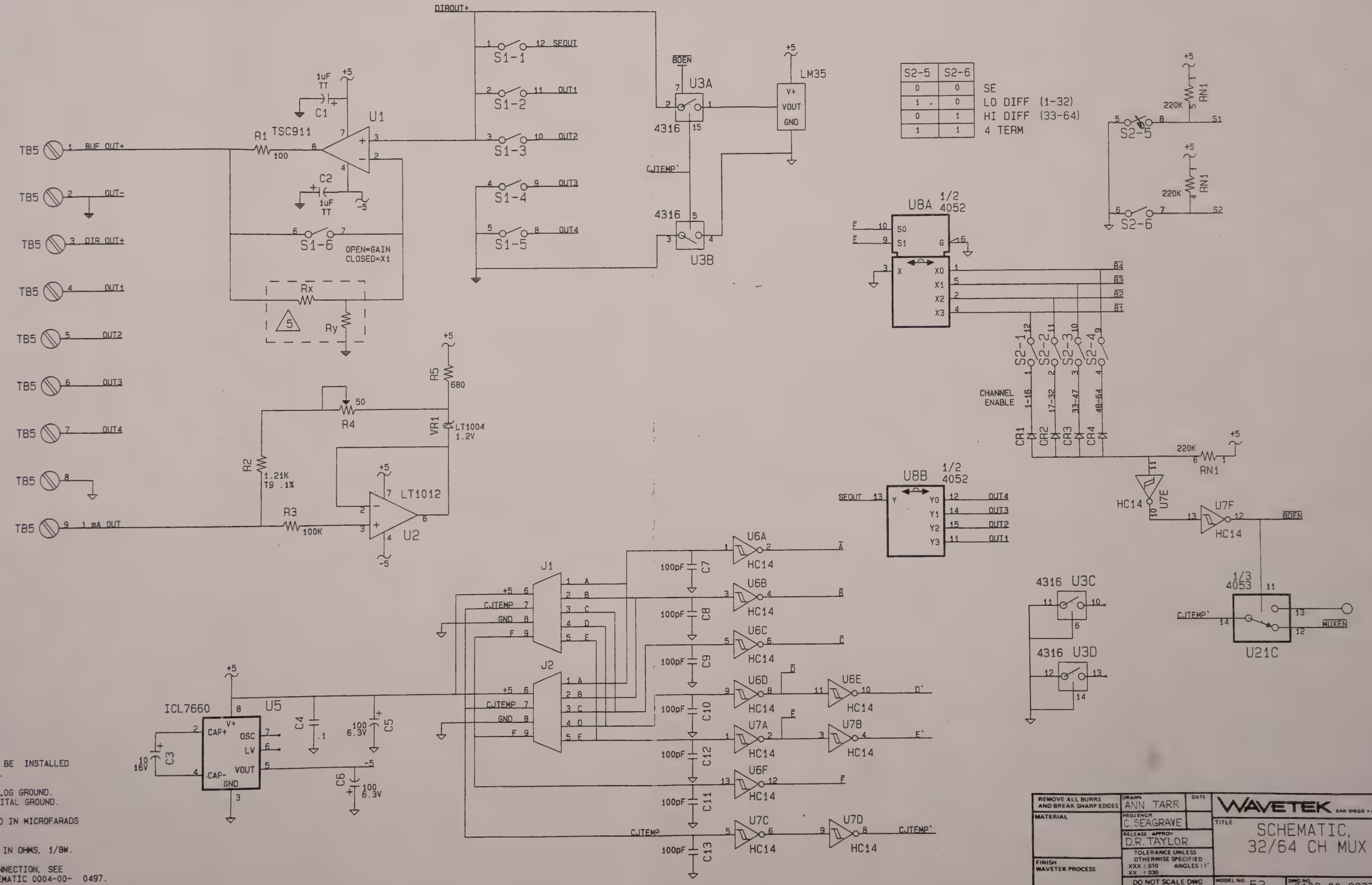
WAVETEK PARTS LIST
TITLE ASSY, 32/64 MUX MODULE
ASSEMBLY NO. 1000-00-0499
REV B
PAGE 2

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
ASSY, 32/64 MUX
MODULE
SIZE D
FSCM NO. 23338
DWG. NO. 1000-00-0499
REV B
SCALE OPTION 53-1
SHEET 1 OF 1

REV	ECN	BY	DATE	APP
B	FOR RELEASE PER ERO 13..	/ -		
C	ECO #3002	A	[illegible]	A.E.T


DIROUT+
TB5 1 BUF OUT+
TB5 2 OUT-
TB5 3 DIR OUT+
TB5 4 OUT1
TB5 5 OUT2
TB5 6 OUT3
TB5 7 OUT4
TB5 8
TB5 9 1 mA OUT
R1 100
TSC911
U1
1uF TT C1
+5
C2 1uF TT
-5
S1-1 SEOUT
S1-2 OUT1
S1-3 OUT2
S1-4 OUT3
S1-5 OUT4
S1-6 OPEN=GAIN CLOSED=X1
Rx
Ry
5
BDEN
U3A 4316
U3B 4316
CJTEMP`
LM35 V+ VOUT GND
R5 680
VR1 LT1004 1.2V
R4 50
R2 1.21K T9 .1%
R3 100K
LT1012 U2
U8A 1/2 4052 S0 S1 X X0 X1 X2 X3
B4 B3 B2 B1
S2-1 S2-2 S2-3 S2-4
CHANNEL ENABLE 1-16 17-32 33-47 48-64
CR1 CR2 CR3 CR4
RN1 220K
S2-5 S1
S2-6 S2
U7E HC14
U7F HC14
BDEN
U8B 1/2 4052 SEOUT Y Y0 Y1 Y2 Y3 OUT4 OUT3 OUT2 OUT1
4316 U3C
4316 U3D
1/3 4053 U21C CJTEMP` MUXEN
J1 +5 CJTEMP GND F A B C D E
J2 +5 CJTEMP GND F A B C D E
100pF C7 C8 C9 C10 C12 C11 C13
U6A U6B U6C U6D U6E U6F U7A U7B U7C U7D HC14
A B C D D` E E` F CJTEMP CJTEMP`
ICL7660 U5 V+ OSC LV CAP+ CAP- VOUT GND
C3 10 16V
C4 .1
C5 100 6.3V
C6 100 6.3V

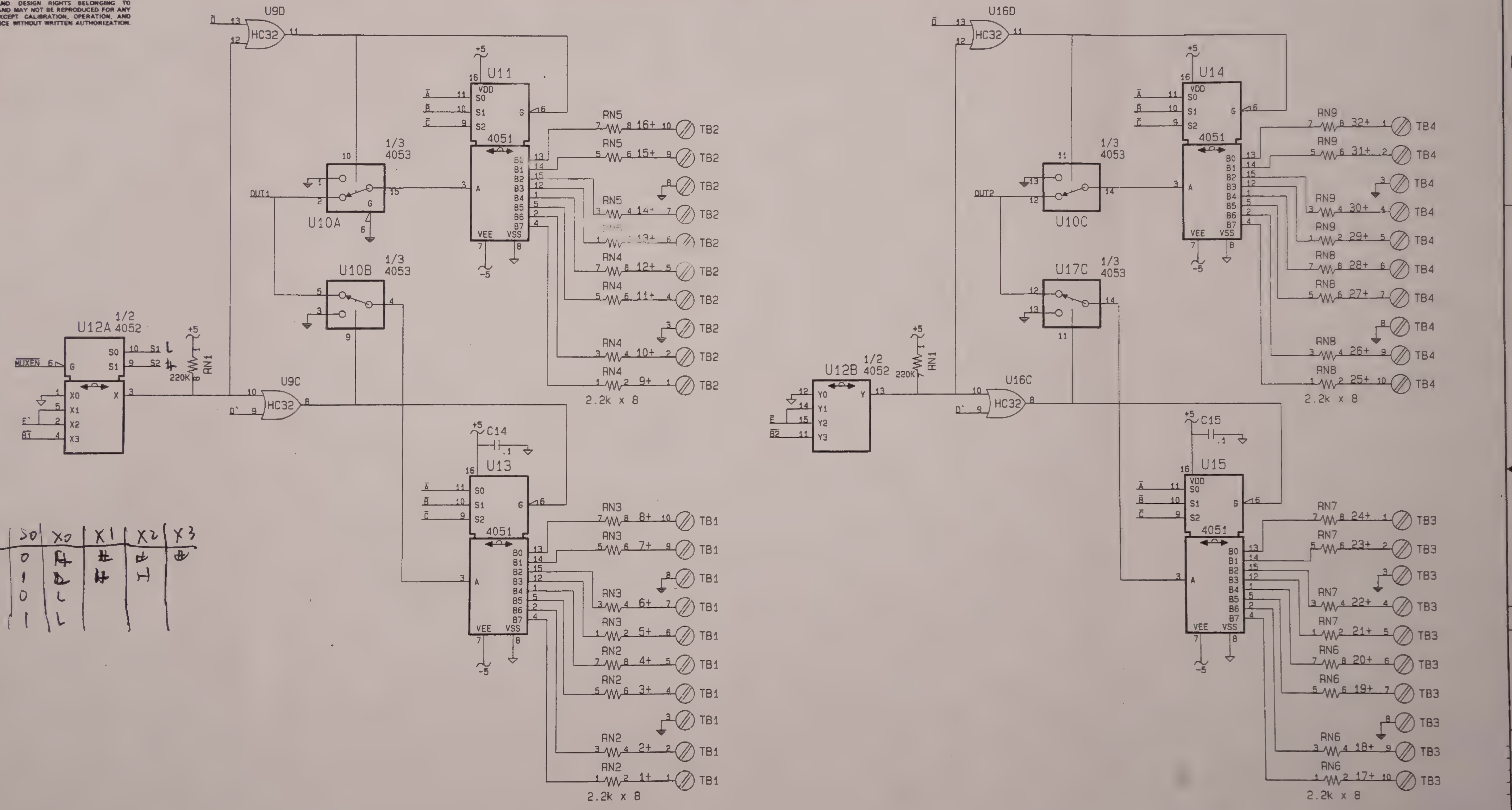
S2-5	S2-6	
0	0	SE
1	0	LO DIFF (1-32)
0	1	HI DIFF (33-64)
1	1	4 TERM

5. RESISTOR NET MAY BE INSTALLED FOR GAIN = Rx/Ry.
4. ⏚ INDICATES ANALOG GROUND.
   ⏚ INDICATES DIGITAL GROUND.
3. CAPACITORS VALUED IN MICROFARADS (uF).
2. RESISTORS VALUED IN OHMS, 1/8W.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00- 0497.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ANN TARR	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR C. SEAGRAVE		TITLE SCHEMATIC, 32/64 CH MUX
	RELEASE APPROV D.R. TAYLOR		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 53	DWG NO. 0103-00-2877 REV C
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 3

0103-00-2877 C


U9D
HC32
D̄
U11
4051
U10A
1/3 4053
U10B
1/3 4053
OUT1
U12A
1/2 4052
MUXEN
S0
S1
X0
X1
X2
X3
E`
B̄1
220K
RN1
+5
U9C
HC32
D`
U13
4051
C14
.1
-5
VDD
VEE
VSS
Ā
B̄
C̄
B0
B1
B2
B3
B4
B5
B6
B7
RN5
RN4
RN3
RN2
16+
15+
14+
13+
12+
11+
10+
9+
8+
7+
6+
5+
4+
3+
2+
1+
TB2
TB1
2.2k x 8
U16D
HC32
U14
4051
U10C
1/3 4053
U17C
1/3 4053
OUT2
U12B
1/2 4052
Y0
Y1
Y2
Y3
Ē
B̄2
U16C
HC32
U15
4051
C15
RN9
RN8
RN7
RN6
32+
31+
30+
29+
28+
27+
26+
25+
24+
23+
22+
21+
20+
19+
18+
17+
TB4
TB3
2.2k x 8

S1	S0	X0	X1	X2	X3
0	0	H	H	[illegible]	[illegible]
0	1	L	H	H	
1	0	L			
1	1	L			

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN Ann Iärr
DATE
PROJ ENGR C. Eajrave
RELEASE APPROV P.K. Taylik

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX : 010 ANGLES : 1°
XX : 030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

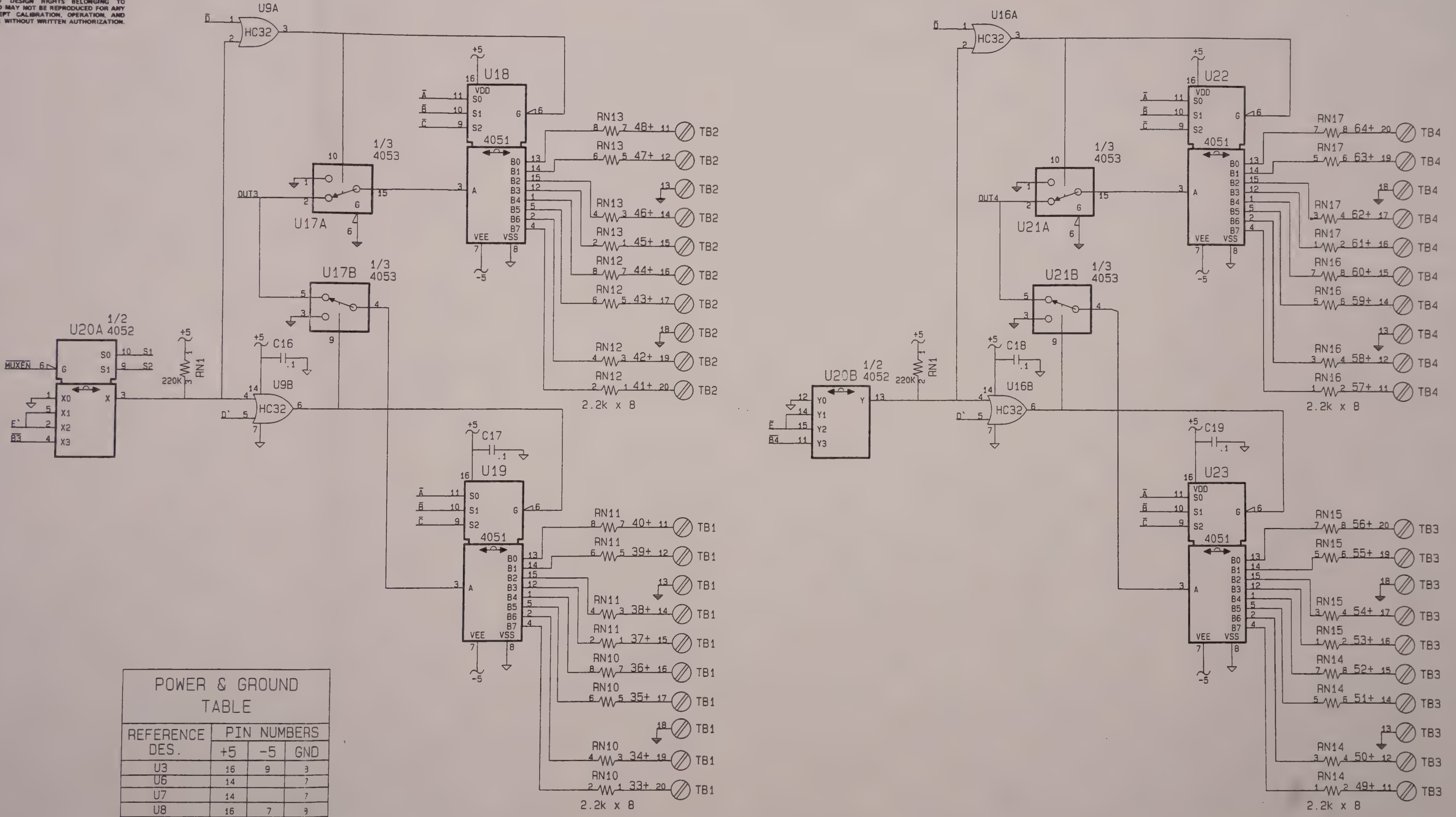
TITLE SCHEMATIC, 32/64 CH MUX

MODEL NO. 53
DWG NO 0103-00-2877
REV C
CODE IDENT 23338
SHEET 2 OF 3

REV | ECN | BY | DATE | APP

0103-00-2877 C

REV	ECN	BY	DATE	APP


U9A
HC32
D̄
U18
4051
VDD
S0
S1
S2
G
VEE
VSS
A
B0
B1
B2
B3
B4
B5
B6
B7
+5
-5
Ā
B̄
C̄
1/3
4053
OUT3
U17A
U17B
U20A
1/2
4052
MUXEN
X0
X1
X2
X3
X
E`
B3
RN1
220K
C16
.1
U9B
D`
U19
C17
RN13
RN12
RN11
RN10
2.2k x 8
48+
47+
46+
45+
44+
43+
42+
41+
40+
39+
38+
37+
36+
35+
34+
33+
TB1
TB2
U16A
U22
OUT4
U21A
U21B
U20B
Y0
Y1
Y2
Y3
Y
Ē
B4
C18
U16B
U23
C19
RN17
RN16
RN15
RN14
64+
63+
62+
61+
60+
59+
58+
57+
56+
55+
54+
53+
52+
51+
50+
49+
TB3
TB4

POWER & GROUND TABLE			
REFERENCE DES.	PIN NUMBERS		
	+5	-5	GND
U3	16	9	3
U6	14		7
U7	14		7
U8	16	7	9
U10	16	7	3
U12	16	7	3
U17	16	7	8
U20	16	7	3
U21	16	7	8

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN AnnTarr
DATE
PROJ ENGR C.Seagrave
RELEASE APPROV D.R.Taylor
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE

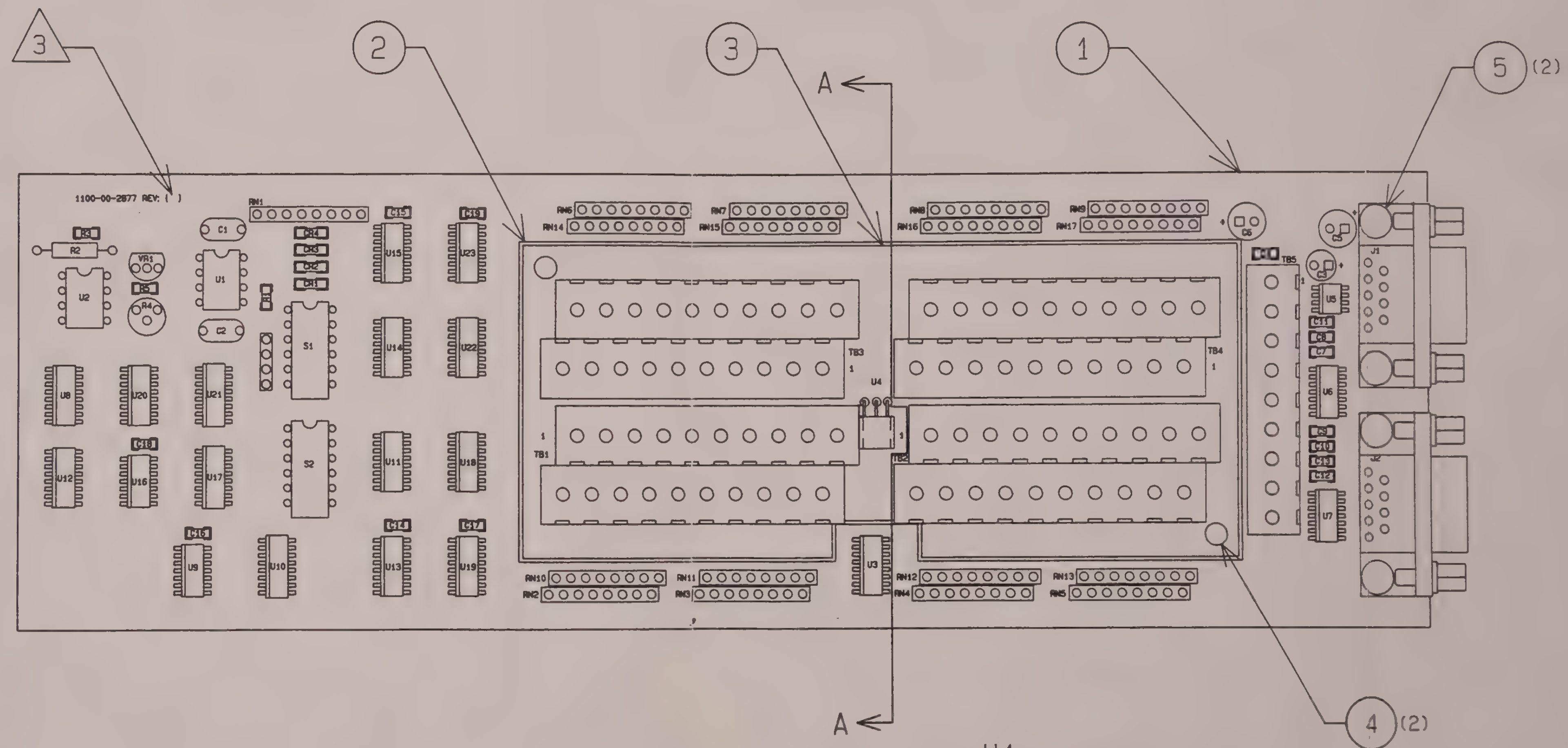
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
32/64 CH MUX

MODEL NO. 53
DWG NO 0103-00-2877
REV C
CODE IDENT 23338
SHEET 3 OF 3

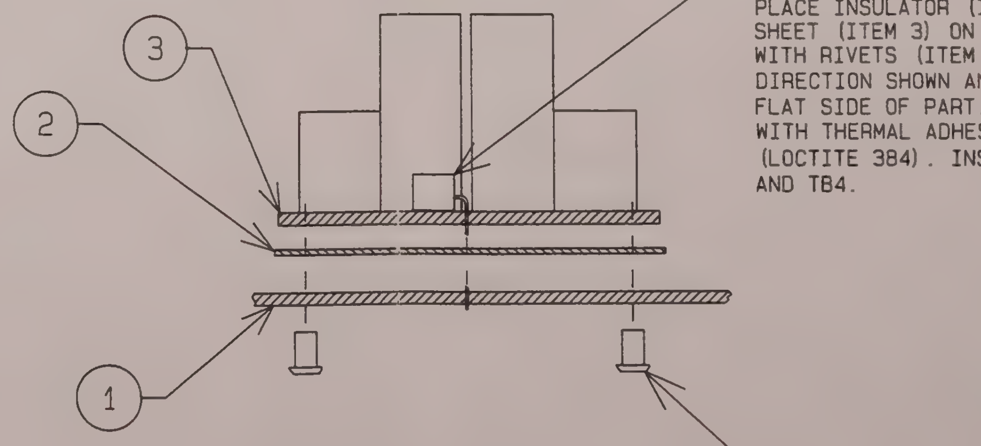
0103-00-2877 C

REV	ECN	BY	DATE	APP
A	FOR RELEASE PER ERO # 7966		2/11/87	
B	ECO # 9002	T.C.	8/3/87	Q.R.T
C	ECO # 9004		8/26/87	Q.R.T.



3
2
3
1
5 (2)
A
A
4 (2)
1100-00-2877 REV: ( )
R3
R2
VR1
R5
R4
U2
C1
U1
C2
RN1
CR4
CR3
CR2
CR1
R1
S1
S2
U8
U20
U21
U12
C18
U16
U17
C16
U9
U10
C15
U15
C19
U23
U14
U22
U11
U18
C14
U13
C17
U19
RN6
RN14
RN7
RN15
RN8
RN16
RN9
RN17
TB3
TB1
TB4
TB2
U4
U3
RN10
RN2
RN11
RN3
RN12
RN4
RN13
RN5
C6
C5
C4
TB5
U5
C11
C8
C7
U6
C9
C10
C13
C12
U7
J1
J2

U4
PLACE INSULATOR (ITEM 2) AND ISOTHERMAL SHEET (ITEM 3) ON PC BOARD AND FASTEN WITH RIVETS (ITEM 4). INSTALL U4 IN DIRECTION SHOWN AND FOLD DOWN TOWARD FLAT SIDE OF PART. ATTACH U4 TO ITEM3 WITH THERMAL ADHESIVE 1600-00-0019 (LOCTITE 384). INSTALL TB1, TB2, TB3 AND TB4.



SECTION A-A
(ROTATED 90° CW)
(EXPLODED FOR CLARITY)

5. TRIM COMPONENT LEADS TO A MAXIMUM HEIGHT OF .060 FROM BOARD SURFACE.
4. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
3. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0947.
1. SEE 0103-00-2886 FOR SCHEMATIC.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1100-00-2877

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T./A.L.T.	DATE 2/11/87	WAVETEK SAN DIEGO • CALIFORNIA		
MATERIAL	PROJ ENGR	2-17-87	TITLE PCA, 32/64 MUX		
	RELEASE APPROV				
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 .XX ±.030 ANGLES ±1°				
	DO NOT SCALE DWG		MODEL NO. 53	DWG NO. 1100-00-2877	REV C
	SCALE 2/1		CODE IDENT 23338	SHEET 1 OF 1	

1100-00-2877 C

BISHOP GRAPHICS/ACCUPRESS

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, 32/64 MUX BOARD	0103-00-2877	WVTK	0103-00-2877	1
3	SHEET, ISOTHERMAL	1400-02-2473	WVTK	1400-02-2473	1
2	INSULATOR, ISOTHERMAL SHEET	1400-02-2480	WVTK	1400-02-2480	1
C3	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	1
C5 C6	CAP, ELECT, 100UF, 6.3V	NRWA101M6.3	NIC	1500-31-0100	2
C1 C2	CAP, TANT, 1MF, 35V	196D105X0035HA1	SPRAG	1500-71-0512	2
'C12 C10 C11 C13 C7 C8 C9	SMD, CAP, CER, 2%, 50V, NPO 100PF	C1206C101J2GAC	KEMET	1500-81-0101	7
C14 C15 C16 C17 C18 C19 C4	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	7
1	32/64 MUX BOARD	1700-00-2877	WVTK	1700-00-2877	1
J1 J2	CONNECTOR, RT ANGLE PC MOUNT, 9 PIN	745394-2	AMP	2100-02-0200	2
TB5	TERMINAL STRIP, 9 PIN, PC MOUNT	20.872.009	WECO	2100-09-0024	1
TB1 TB2 TB3 TB4	TERMINAL STRIP, 20 PIN, TIERED, PC MOUNT	21.872.910	WECO	2100-09-0025	4
4	RIVET, ALUM 1/8X1/4L	1125-0408	AVDEL	2800-12-0043	2

WAVETEK
PARTS LIST
TITLE PCA, 32/64 MUX
ASSEMBLY NO. 1100-00-2877
REV C
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	ROCKERS				
U4	IC, CENTIGRADE TEMP SENSOR	LM35DZ	NAT	7000-00-3500	1
~~U1~~	IC, OP AMP, AUTO-ZERO, MONOLITHIC	TSC911ACPA	TELE	7000-09-1100	1
VR1	MICROPOWER VOLT REF, 1.2V, +-MV INITIAL ACC	LT1004CZ-1.2	LINTE	7000-10-0400	1
~~U2~~	IC, PICOAMP INPUT MIC VOLT OFFSET LOW NOISE	LT1012CN8	LINTE	7000-10-1200	1
U12 U20 U8	MUL/DEMUL, DUAL 4 CHANNEL ANALOG, SMD	HEF4052BTD	SIG	7000-40-5200	3
U10 U17 U21	SO, TRIPLE 2 CHANNEL ANALOG MUL/DEMUL	HEF4053BTD	SIG	7000-40-5301	3
U5	SMD, DC TO DC CONVERTER, CMOS, 300MW	ICL7660CBA	INTSL	7000-76-6041	1
U11 U13 U14 U15 U18 U19 U22 U23	MUX/DEMUX 8-CHANNEL ANALOG CMOS SMD	HEF4051BTD	SIG	8000-40-5141	8
U6 U7	SMD, HEX SCHMITT TRIGGER/INVERTER, HCMOS	74HC14D	SIG	8000-74-1441	2
U16 U9	SMD, QUAD 2-INPUT OR GATE, HCMOS	74HC32D	SIG	8000-74-3241	2

WAVETEK
PARTS LIST
TITLE PCA, 32/64 MUX
ASSEMBLY NO. 1100-00-2877
REV C
PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	.126-.187				
5	PLASTIC RIVET	231-080151-05-0101	FASTX	2800-60-0008	4
R4	POT, TRIM, 50	3329H-1-500	BOURN	4600-05-0001	1
R1	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 100 OHM	9C12063A1000JLR	MEPCO	4703-20-1015	1
R3	SMD, GP RESISTOR, 1/8 LONG, 200PPM, 5%, 100K OHM	MCR18EZH104JM5%	ROHM	4703-20-1045	1
R5	RES, SMD GP 1/8 LONG 200PPM 5% 680 OHM	0108-00-2765	REF SPE	4703-20-6815	1
RN1	RES, NETWORK, 8 PIN SIP, ONE PIN COMMON 220K	4308R-101-224	BOURN	4770-00-0055	1
RN10 RN11 RN12 RN13 RN14 RN15 RN16 RN17 RN2 RN3 RN4 RN5 RN6 RN7 RN8 RN9	RES NETWORK, 4 ISOLATED, 2.2K, THICK FILM, .350	MSP08C032220	DALE	4770-00-0056	16
R2	RES, MF, 1/8W, .1%, T-9, 1.21K	CMF-551211BT-9	DALE	4799-00-0143	1
CR1 CR2 CR3 CR4	SMD, DIODE, LEADLESS EQUIVALENT IN4148, 500MW	RLS4148	ROHM	4807-01-4148	4
S1 S2	SWITCH, DIP, SPST, 6	76SB06	GRHL	5100-00-0010	2

WAVETEK
PARTS LIST
TITLE PCA, 32/64 MUX
ASSEMBLY NO. 1100-00-2877
REV C
PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U3	IC, SMD, QUAD BILATERAL SWITCHES	74HC4316D	SIG	8007-44-3161	1

WAVETEK
PARTS LIST
TITLE PCA, 32/64 MUX
ASSEMBLY NO. 1100-00-2877
REV C
PAGE 4

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
PCA, 32/64 MUX
SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-2877
REV C
SCALE OPTION 53-2
SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C10 C11 C12 C13 C7 C8 C9	CAP, SMD CER 5% 50V NPO 100PF	C1206C101J2GAC	KEMET	1500-81-0101	7
C14 C15 C16 C17 C18 C19 C4	CAP, SMD CER +80-20% Z5U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	7
NONE	32/64 MUX BOARD	1700-00-2877	WVTK	1700-00-2877	1
R1	RES, SMD GP 1/8 LONG 200PPM 5% 100 OHM	9C12063A1000JLR	MEPCO	4703-20-1015	1
R3	RES, SMD GP 1/8 LONG 200PPM 5% 100K OHM	MCR18EZH104JW5%	ROHM	4703-20-1045	1
R5	RES, SMD GP 1/8 LONG 200PPM 5% 680 OHM	0108-00-2765	REF SPE	4703-20-6815	1
CR1 CR2 CR3 CR4	DIODE, LEADLESS EQUIVALENT IN4148, 500MW, SMD	RLS4148	ROHM	4807-01-4148	4
U12 U20 U8	MUL/DEMUL, DUAL 4 CHANNEL ANALOG, SMD	HEF4052BTD	SIG	7000-40-5200	3
U10 U17 U21	MUL/DEMUL, TRIPLE 2-CH ANALOG, SO	HEF4053BTD	SIG	7000-40-5301	3
U5	CONVERTER, DC TO DC, CMOS, 300MW, SMD	ICL7660CBA	INTSL	7000-76-6041	1
U11 U13 U14 U15 U18 U19 U22 U23	MUX/DEMUX 8-CHANNEL ANALOG CMOS SMD	HEF4051BTD	SIG	8000-40-5141	8

WAVETEK
PARTS LIST
TITLE
ASSY, PCA 32/64 MUX (SMD)
ASSEMBLY NO.
1208-00-2954
REV
A
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U6 U7	HEX SCHMITT TRIGGER/INVERTER, HCMOS, SMD	74HC14D	SIG	8000-74-1441	2
U16 U9	GATE, OR, QUAD 2-INPUT, HCMOS, SMD	74HC32D	SIG	8000-74-3241	2
U3	SWITCHES, QUAD BILATERAL, SMD	74HC4316D	SIG	8007-44-3161	1

WAVETEK
PARTS LIST
TITLE
ASSY, PCA 32/64 MUX (SMD)
ASSEMBLY NO.
1208-00-2954
REV
A
PAGE 2

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
ASSY, PCA 32/64 MUX (SMD)
SIZE D
FSCM NO. 23338
DWG. NO. 1208-00-2954
REV A
SCALE
MODEL 53
SHEET 1 OF 1

APPENDIX A.

AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII)

BITS[2] b7 b6 b5					000	MSG[1]	001	MSG	010	MSG	011	MSG	100	MSG	101	MSG	110	MSG	111	MSG
b4	b3	b2	b1	column → row ↓	0		1		2		3		4		5		6		7	
0	0	0	0	0	NUL		DLE		SP	MLA ASSIGNED TO DEVICE	0	MLA ASSIGNED TO DEVICE	@	MTA ASSIGNED TO DEVICE	P	MTA ASSIGNED TO DEVICE	\	MEANING DEFINED BY PCG CODE	p	MEANING DEFINED BY PCG CODE
0	0	0	1	1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0	0	1	0	2	STX		DC2		"		2		B		R		b		r	
0	0	1	1	3	ETX		DC3		#		3		C		S		c		s	
0	1	0	0	4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0	1	0	1	5	ENQ	PPC[3]	NAK	PPU	%		5		E		U		e		u	
0	1	1	0	6	ACK		SYN		&		6		F		V		f		v	
0	1	1	1	7	BEL		ETB		'		7		G		W		g		w	
1	0	0	0	8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1	0	0	1	9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1	0	1	0	10	LF		SUB		•				J		Z		j		z	
1	0	1	1	11	VT		ESC		+		.		K		[		k		{	
1	1	0	0	12	FF		FS		,		<		L		\		l		¦	
1	1	0	1	13	CR		GS		-		=		M		]		m		|	
1	1	1	0	14	SO		RS		•		>		N		^		n		~	
1	1	1	1	15	SI		US		/		?	UNL	O		___	UNT	o		DEL	

ADDRESSED COMMAND GROUP (ACG)

UNIVERSAL COMMAND GROUP (UCG)

[4] LISTEN ADDRESS GROUP (LAG)

TALK ADDRESS GROUP (TAG)

PRIMARY COMMAND GROUP (PCG)

SECONDARY COMMAND GROUP (SCG)

---

[1] MSG = INTERFACE MESSAGE

[2] b1 = DIO1 . . . b7 = DIO7

[3] REQUIRES SECONDARY COMMAND

[4] DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	=	DCL	Device clear	Universal Command Group
DC1	=	LLO	Local lockout	
NAK	=	PPU	Parallel poll unconfigure	
EM	=	SPD	Serial poll disable	
CAN	=	SPE	Serial poll enable	
SOH	=	GTL	Go to local	Addressed Command Group
EOT	=	SDC	Selected device clear	
ENQ	=	PPC	Parallel poll configure	
BS	=	GET	Group execute trigger	
HT	=	TCT	Take control	

APPENDIX B.
RECOMMENDED SPARE PARTS

The Wavetek part number for any component is given in the parts list for the appropriate board in the drawing package, section 7.

Generic Part Number	Designator	Function
Motherboard		
1A, 3AG		Chassis fuse
63B03	U1	MPU (microprocessor)
SRM2064M	U4, U7	8K RAMs (replace as a pair)
27C512	U5	ROM
	U5T	Test ROM (Call Factory)
ST5152	U27	Gate Array
HC241	U10	Tristate buffer
HC244	U11	Tristate buffer
MAX232EPE	U6	Level Translator
RFP6P08	Q2	Switcher FET
IRFD9123	Q3	MOSFET
4093	U13D	Quad Schmitt Nand
HC138	U24	3 to 8 decoder
HC245	U25	Bidirectional bus driver
Measurement Modules		
1A, 3AG	F1	J3 Fuse
6N136	U22	Optoisolator
6N136	U23	Optoisolator
2730	U24	Optoisolator
PWR103-2	U25	Power Module for 50-1
PWR103-1	U25	Power Module for 50-2
ICL7660	U26	Voltage inverter
DS2E-SL2 – DC6V	K1-K5	Relay
Battery Pack		50-11 rechargeable battery
1A, 3AG		Fuse
GPIP board		
IRFD9123	Q1	Power switching FET
MC3447P3	U8, U9	GPIB Transceiver
Digital I/O Board		
VN10KM		Output FET
100K, 1/2W		Protection resistor, flameproof
Multiplexer, 50-20		
PVR3301		FET switch (double pole)
PVA3554		FET switch (double pole)
V390MA3A		Metal oxide varistor

APPENDIX C
MOTHERBOARD VS. OPTION BOARD FAULT ISOLATION

(Rear Panel Configuration Detection)

Overview

Use of a logic analyzer provides a way to isolate faults between the motherboard and a suspect option board. It is indispensable when no other option boards are available for substitution.

During the power on routine, the software checks each rear panel expansion slot for a possible RAM, GPIB, or Digital I/O board.

The logic analyzer is used to see if the motherboard is sending out correct query information. The state display is most useful. Connection onto the expansion slot lines via an extender board is recommended. Picking up the address and data lines on the motherboard U1 MPU is convenient via a 40 pin IC test clip, and will yield the same MPU data, but will not reveal if there are problems with the U25 and U26 buffers.

One trigger or "focal point" for the analyzer storage is the board enable, BD(n), signal for the slot being checked. It is pin 1B for each slot (front right corner pin). Motherboard communication with a RAM expansion board (inside an 8K bank) occurs without using the BD(n) signal — the enable for communications in the 8K window is the $\overline{\text{8KBSRAM}}$ line. This is pin 12B, on the right side of the socket, counting from the front.

The lines that are stored should be A15-A8, AD7-AD0, R/$\overline{\text{W}}$, BD(n) for the socket, and 8KBSRAM. If the qualifier capability available on most analyzers is used, address and data can be stored by the analyzer only when either $\overline{\text{BD(n)}}$ or $\overline{\text{8KBSRAM}}$ are low.

Checking An Empty Slot

Unplug all rear panel option boards. Page C-2 shows the data capture for an empty slot (the righthand expansion slot, board enable address 7**20**). If an option board is plugged in and is recognized, or is otherwise driving the slot, the data exchange will be different. If a different slot is plugged into, the first line of data capture will reflect that slot's enable address (see table 5-3, U24 Decoder Outputs).

Analyzer input data must be captured on the falling edge of E clock (the end of a cycle).

The motherboard U25 bus driver will also buffer the low order address outward during the first half of the cycle. These lines to the analyzer will charge to the correct logic levels. The analyzer input capacitance will stretch the address logic levels to the end of the cycle, where the levels are read as "data", *if* U25 had correctly turned around and the right side of U25 is high impedance.

AS at the slot is not needed as part of the analyzer setup. However, it should be checked with an oscilloscope.

The forced power up routine is initiated as in paragraph 6.4.3.2.4.

Page C-3 shows the menu setups for one logic analyzer, the Arium 4100. The routine must be initiated twice for the Arium analyzer to be triggered.

Explanation Of The General Slot Checking Routine

Near the end of the power on routine, after type checking measurement modules, the software checks each rear panel expansion slot for a possible RAM board, GPIB board, or Digital I/O board, in that order. J7 is checked for all three types of boards, then J8 is checked, then J9, etc.

Software Sequence

1. There is a (MPU) read from the base address of all slots. In the case of J7, this would be address 0720_H.
2. The motherboard writes data of 00 to the base address of all slots.
3. There is a write of data 08_H to the base address of the first slot.
4. **RAM board check.** There are reads from 7FFC and 7FFD of the slot. If the data read back is ASCII [W,C] (57_H, 43_H), the software reads from address 7FFE. If all three do not add up to WCL, then software attempts to store WCL in 7FFC-7FFE. Then, reads occur — in the case of a non-RAM slot, only 7FFC-7FFD tried.
5. **Establishing RAM size.** If a RAM is detected in (4), bank switching is done, and the next higher bank of memory is tried, until the readback test fails. Bank switching data: 18_H, 28_H, 38_H to first address of the slot. Step 5 establishes the number of 64K blocks on the board.
6. If the board in step 4 was a RAM, the motherboard software loops back to step 3 and begins checking the next slot. Otherwise, go to step 7.

7. **GPIB board check.**

   a. Software reads from the slot's base address + 14. (For example, if checking J7, the address would be 734_H.)

   b. If the data read indicates a possible GPIB board, software writes 80_H to the slot's base address + 3; otherwise, it executes step 8.

   c. The motherboard writes 00_H to the slot's base address + 0.

   d. The motherboard reads from the slot's base address + 0.

   GPIB Initialization:

   1) The motherboard writes 80_H to the slot's base address + 3.

   2) The motherboard writes 00_H to the slot's base address + 3.

   3) The motherboard reads from the slot's base address + 4.

   4) The motherboard writes the preceding read data value into the base address + 4.

   5) The motherboard writes 00_H into the slot's base address + 5.

   6) The motherboard writes 00_H into the slot's base address + 6.

   7) The motherboard writes 35_H into the slot's base address + 0.

8. **Digital I/O board check.** The motherboard reads the base address of the slot; the data read will be a 01_H if a digital I/O board. If a digital I/O board is found, the motherboard initializes the board: 00_H is written to the slot's base address +1, and 00_H is written to the slot's base address + 2. Otherwise, the software begins checking the next slot (step 3).

Data Captured By Arium (Empty Slots)

Listed below is the data captured by the Arium analyzer, with the setup on page C-3. Note that only two fields of information are shown here (one displayed in binary, the other in hex): The left field shows the state of the $\overline{\text{8KBSRAM}}$, $\overline{\text{BD(n)}}$, and R/$\overline{\text{W}}$ lines, and the right field shows the state of the data. (The data field shows the low order address, if a read cycle is being done on an empty socket. The TRIGger step read here is from address 0720.) Not shown is the high order 8 bits of the address. The user may connect other analyzer inputs for the high order address bits if desired.

STATE	BIN	HEX	Comments
TRIG	00000101	20	Ongoing storage stops 990 clocks after $\overline{\text{BD1}}$ goes low for first time.
00001	00000100	00	
00002	00000100	08	
00003	00000011	FC	Reads 7FFC. (J7 RAM check.)
00004	00000011	FD	
00005	00000010	57	Writing W.
00006	00000010	43	Writing C.
00007	00000010	4C	Writing L.
00008	00000011	FC	Checking for W.
00009	00000011	FD	End of J7 RAM check.
00010	00000101	34	Checking for GPIB.
00011	00000101	20	Checking for Digital I/O.
00012	00000011	FC	(J8 RAM check.)
00013	00000011	FD	
00014	00000010	57	
00015	00000010	43	
00016	00000010	4C	
00017	00000011	FC	
00018	00000011	FD	
00019	00000011	FC	(J9 RAM check.)
00020	00000011	FD	
00021	00000010	57	
00022	00000010	43	
00023	00000010	4C	
00024	00000011	FC	
00025	00000011	FD	
00026	00000011	FC	(J10 RAM check.)
00027	00000011	FD	
00028	00000010	57	
00029	00000010	43	
00030	00000010	4C	
00031	00000011	FC	
00032	00000011	FD	
00033	00000011	FC	(J11 RAM check).
00034	00000011	FD	
00035	00000010	57	
00036	00000010	43	
00037	00000010	4C	
00038	00000011	FC	
00039	00000011	FD	

The data for the RAM checks for the other slots are captured by the analyzer, since $\overline{\text{8KBSRAM}}$ is one of the qualifiers, and the qualification is A + B, meaning A or B. A is the board enable ($\overline{\text{BD1}}$ in this case), and B is $\overline{\text{8KBSRAM}}$, which is common to all slots.

Arium Logic Analyzer Setup

DISPLAY FORMAT

```
  TIMING:
  Line          1   2   3   4   5   6   7   8   9  10  11  12
               00  01  02  03  04  05  06  07  08  09  10  11

  STATE:
  Field          1     2     3     4     5     6     7     8
  Base         BIN   BIN   BIN   HEX   OFF   OFF   OFF   OFF
  High Probe    31    23    15    07    00    00    00    00
   Low Probe    24    16    08    00    00    00    00    00
  Data Sense   NON   NON   NON   NON   NON   NON   NON   NON
Bases:  A=ASC  B=BIN  C=OCT  D=DEC  E=HEX  F=OFF
Senses: 0=NON (non-inverted), 1=INV

POD MODE (also sets defaults): LOGIC32
f1=LOGIC4   f2=LOGIC8   f3=LOGIC16   f4=LOGIC32
```

CONFIGURATION

```
RECORD WIDTH (4,8,16,32) : 32 bits
RECORD DEPTH             : 1000 words

DATA QUALIFICATION TYPE (32-bit only):
(0=off, 1=comb., 2=state) : comb
COMBINATIONAL QUALIFICATION
Record (0=only, 1=all but) : only
Occurrences of             : A+B
STATE QUALIFICATION (starts enabled)
Reenable record on occur. of: none
  Disable record on occur. of: none

(Type A, B, C or D to alternately include/exclude a trigger word)
```

CLOCK

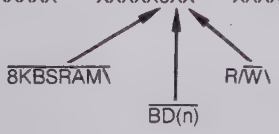
```
SOURCE (0=internal,1=external): External

INTERNAL:
Clock period (10 ns — 200 ms)   : 0080 nsec
  (f1=nsec, f2=usec, f3=msec)
Clock rate                      : 12.5 Mhz
Record time                     : 80.0 μsecs

EXTERNAL:
Clock edge (0=fall,1=rise)      : falling
Qualifier valid                 : always
  (0=low, 1=high, 2=always)
```

TRIGGER DELAY

```
Storage will stop 00990 clocks after the trigger event.

Storage begins up to 00009 clocks before the trigger event.

(A=after, B=before)

In 4 bit mode, Delay is multiple of 40
In 8 bit mode, Delay is multiple of 20
In 16 bit mode, Delay is multiple of 10
In 32 bit mode, Delay is multiple of 5
```

TRIGGER

```
           BIN         BIN         BIN          BIN
A:    XXXXXXXX    XXXXXXXX    XXXXXX0X           XX
      XXXXXXXX    XXXXXXXX    XXXXXX0X     XXXXXXXX
                                  .
                                  .
                                  .
B:    XXXXXXXX    XXXXXXXX    XXXXX0XX           XX
      XXXXXXXX    XXXXXXXX    XXXXX0XX     XXXXXXXX
```



Sequence: A

TRIGGER SEQUENCE ("+" means "or")

A

APPENDIX D
DECIMAL/HEXADECIMAL/BINARY NUMBER EQUIVALENTS

Following are some useful conversions for troubleshooting addressing.

Decimal	Hexadecimal	Binary															
1	0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
3	0003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0004	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
5	0005	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0006	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0007	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
8	0008	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0009	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
10	000A	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
11	000B	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
12	000C	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
13	000D	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
14	000E	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
15	000F	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
16	0010	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
17	0011	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
31	001F	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
32	0020	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
33	0021	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
64	0040	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
96	0060	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
128	0080	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
256	0100	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
512	0200	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
768	0300	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
1024	0400	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1280	0500	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
1536	0600	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
1792	0700	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
1824	0720	0	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0
1856	0740	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0
1888	0760	0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0
1920	0780	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
1952	07A0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0
1984	07C0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
2047	07FF	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
2048	0800	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
4096	1000	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
8192	2000	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
16384	4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24576	6000	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
32764	7FFC	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
32765	7FFD	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
32766	7FFE	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
32767	7FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
32768	8000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

APPENDIX D (Continued)

Decimal	Hexadecimal	Binary															
40960	A000	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
49152	C000	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
57344	E000	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
65532	FFFC	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
65533	FFFD	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
65534	FFFE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
65535	FFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
65536	10000*																
131072	20000*																
196608	30000*																
262144	40000*																
524288	080000*																
1048576	100000*																
1310720	140000*																

*Shown for reference only. The Model 52 does not directly access addresses above 65535.

APPENDIX E.
REMOVING OR REPLACING CHIP RESISTORS AND CAPACITORS

Removal

With a narrow-point tweezers, grab both sides of the chip. Heat both ends of the chip component with a soldering iron. Lift the chip off the board.

Installation

Premelt some solder onto one of the two pads on the circuit board. Lift the new chip part with the tweezers, put in place, and heat the end of the chip that has the solder on the pad until the solder flows around the end of the chip. Allow to cool so that the solder joint hardens. Now solder the other end of the chip component.

APPENDIX F.
REPLACING SMALL OUTLINE IC'S

Required: Narrow-tip soldering iron*, solderwick, narrow-tip metal pick, 60/40 rosin core solder (narrow gage). Operator should have some prior experience doing fine soldering. Read this entire procedure before starting.

Caution

Regard all IC's in the unit as static sensitive unless otherwise identified.

I.C. Removal

1) Touch the metal back of the chassis to ground yourself to the same potential as the circuit, while touching the tip of the iron to the metal back of the chassis to equalize any static charge between the three bodies. If working on a measurement module, also touch the tip of the iron to TP1 (ground) on the measurement module. Touch TP1 ground momentarily yourself.
2) Wick all pins of the bad IC clean of solder using solderwick.
3) Nudge eack pin slightly with a metal probe to free it from the pad on the board. Then remove part.
4) Clean the spot on the board that the part was in with freon.

Installation (Refrain from walking around in the middle of this sequence.)

1) Touch the metal back of the chassis to ground yourself to the same potential as the circuit, while touching the tip of the iron to the metal back of the chassis to equalize any static charge between the three bodies. If working on a measurement module, also touch the tip of the iron to TP1 (ground) on the measurement module. Touch TP1 ground momentarily yourself.
2) Melt a small amount of fresh solder onto one corner pin of the replacement IC.
3) Put IC in correct position on board and align with the tip of your finger.
4) While holding part in correct alignment, heat the corner pin with the soldering iron so that the solder on the pin bonds to the pad.
5) Then solder the pin that is on the opposite corner of the IC to the board.
6) Solder all other pins on the IC to the board. Clean the IC location with freon again.

*Soldering Irons

Any narrow-tip soldering iron can be used provided it is not above 500°-600°F. 700°-800°F irons can be used provided operator skill permits the job to be done very quickly.

Suggested Irons:

1) Antex Model C (15W). Specifically made for S.O. soldering. But the low wattage will unnecessarily slow down experienced operators.
2) Permax QR-SD (800° element). Experienced operators can use this hot iron successfully.
3) Between these two extremes, a lot of irons are available.

APPENDIX G.
MOTHERBOARD POWER LINE DESTINATIONS

Voltage	Device	Schematic Location
B+	U12-3	2D6
	Q2-S	2D4
	R62	2D4
	CR18-K	2D4
	U16-5	2D4
	R60	2D4
	J7-15B	3C5
	J8-15B	3C5
	J9-15B	3C4
	J10-15B	3C3
	J11-15B	3C2
V++	CR5-A	1D4
	CR6-A	1D4
	R54	2C8
	U13-14	2C7
	U13-6	2C7
	U13-1	2C4
	R55	2C7
	R20	2C7
	S1-15	2C6
	R56	2C7
	U15-14, -5	2C5
	C29	2C4
	U14-14	2C3
	R69	2B1
	J7-16B	3C5
	J8-16B	3C5
	J9-16B	3C4
	J10-16B	3C3
	J11-16B	3C2
V+6	C35+	2D3
	CR20-A	2D3
	J12-10	3A5
	J13-10	3A4
	J14-10	3A3
	J15-10	3A2
V+	U1-21, -7	1D7
	R1	1C7
	R2	1C8
	R5	1C8
	U2-20	1D6
	R6	1C6
	R7	1C6
	U5-28	1D1
	R24	1B5
	R25	1B5
	R26	1B5

APPENDIX G (Continued)

Voltage	Device	Schematic Location
	Q3-S	1B5
	U9-16	1B4
	J4-1A	1A3
	U11-20	1B3
	R50	2D6
	U18-16	2B8
	U19-14	2A8
	U20-14	2A7
	U23-16	2B7
	U24-16	2B6
	U22-14	2B3
	U25-20	3D8
	U26-20, -19	3D7
	S1-9	3C6
	J7-18A	3C6
	J8-18A	3C5
	J9-18A	3C4
	J10-18A	3C3
	J11-18A	3C2
	U31-14	3A8
	U30-14	3A7
	U27-40	3C7
	U28-14	3B6
	U29-14	3C2
	J12-1	3B6
	J13-1	3B4
	J14-1	3B3
	J15-1	3B2

MAINTENANCE MANUAL

Model 52A
Datalogger

For complete Model 52A maintenance information, *Maintenance Manual, Models 51 and 52 Data Multimeter* must be used in conjunction with this supplement manual.

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Manual Revision 3/89
Manual Part Number: 1300-00-0539-1

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Wavetek warrants that all products manufactured by Wavetek conform to published Wavetek specifications and are free from defects in materials and workmanship for a period of one (1) year from the date of delivery when used under normal conditions and within the service conditions for which they were furnished.

The obligation of Wavetek arising from a Warranty claim shall be limited to repairing, or at its option, replacing without charge, any product which in Wavetek's sole opinion proves to be defective within the scope of the Warranty. In the event Wavetek is not able to modify, repair or replace non-conforming defective parts or components to a condition as warrantied within a reasonable time after receipt thereof, Buyers shall be credited for their value at the original purchase price.

Wavetek must be notified in writing of the defect or nonconformity within the Warranty period and the affected product returned to Wavetek's factory or to an authorized service center within (30) days after discovery of such defect or nonconformity.

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CONTENTS

SECTION S1 HOW TO USE THIS SUPPLEMENT

S1.1 INTRODUCTION S1-1
S1.2 WHAT IS IN THIS SUPPLEMENT S1-1
S1.3 HOW TO USE THIS SUPPLEMENT S1-1
S1.4 THE OPERATOR'S MANUAL S1-1
S1.5 CONVENTIONS USED IN THIS MANUAL S1-2

SECTION S2 ROUTINE MAINTENANCE

S2.1 CALIBRATION S2-1
S2.2 FUSE REPLACEMENT S2-1
S2.3 BATTERY REPLACEMENT S2-1
S2.3.1 Primary Power Battery S2-1
S2.3.2 RAM Backup Battery S2-1
S2.3.3 RAM/ROM Board and Option 50-12A Batteries S2-1
S2.4 OPTION REPLACEMENT S2-1
S2.5 PROM REPLACEMENT S2-3
S2.6 MEASUREMENT MODULE REPLACEMENT S2-3

SECTION S3 VERIFICATION PROCEDURE

S3.1 VERIFICATION PROCEDURE S3-1
S3.2 REQUIRED TEST EQUIPMENT S3-1
S3.3 INITIAL CHECKS S3-1
S3.4 INITIAL SETUP S3-2
S3.5 MEASUREMENT MODULE CHECKS S3-2
S3.5.1 DC Voltage Check (Options 50-1 and 50-2) S3-2
S3.5.2 Temperature Check (Options 50-1 and 50-2) S3-3
S3.5.3 AC Voltage Check (Option 50-1 only) S3-3
S3.5.4 Zero Resistance Check (Option 50-1 only) S3-4
S3.5.5 Resistance (>1kΩ) Check (Option 50-1 only) S3-4
S3.5.6 Resistance (≤100Ω) Check (Option 50-1 only) S3-4
S3.5.7 DC Current (mA) Check (Option 50-1 only) S3-5
S3.5.8 DC Current (A) Check (Option 50-1 only) S3-5
S3.5.9 AC Current (mA) Check (Option 50-1 only) S3-6
S3.5.10 AC Current (A) Check (Option 50-1 only) S3-6
S3.5.11 Frequency Check (Option 50-1 only) S3-6
S3.5.12 Frequency Sensitivity Check (Option 50-1 only) S3-6
S3.5.13 TTL Sensitivity Check (Option 50-1 only) S3-7
S3.5.14 CMOS5 Sensitivity Check (Option 50-1 only) S3-7
S3.5.15 CMOS12 Sensitivity Check (Option 50-1 only) S3-7
S3.6 RS-232-C CHECK S3-7
S3.7 IEEE-488 CHECK S3-8
S3.8 DIGITAL I/O CHECK S3-8
S3.9 MEMORY EXPANSION CHECK S3-8
S3.10 RECHARGEABLE BATTERY CHECK S3-9
S3.11 MULTIPLEXER CHECK S3-9
S3.12 VERIFICATION RECORD S3-9

CONTENTS (Continued)

SECTION S4 CALIBRATION PROCEDURE

S4.1 FACTORY REPAIR S4-1
S4.2 REQUIRED TEST EQUIPMENT S4-1
S4.3 CALIBRATING THE MODEL 52A S4-1

SECTION S5 CIRCUIT DESCRIPTION

S5.1 MODEL 52A GENERAL DESCRIPTION S5-1
S5.2 RAM/ROM BOARD S5-1
S5.2.1 Introduction S5-1
S5.2.2 RAM/ROM Board Operation S5-1
S5.3 OPTION 50-12A EXPANSION RAM BOARD S5-2
S5.3.1 Introduction S5-2
S5.3.2 Option 50-12A Operation S5-3
S5.4 OPTION 50-15 SECOND RS-232-C BOARD S5-4
S5.4.1 Introduction S5-4
S5.4.2 Backplane Interface S5-5
S5.4.3 Asynchronous Communications Interface Adapter (ACIA) S5-5
S5.4.4 Handshake Enable S5-6
S5.4.5 RS-232-C Interface S5-6

SECTION S6 TROUBLESHOOTING

S6.1 INTRODUCTION S6-1
S6.2 FACTORY REPAIR S6-1
S6.3 TROUBLESHOOTING THE MODEL 52A S6-1
S6.3.1 RAM/ROM Board S6-1
S6.3.2 Expansion RAM Board S6-2
S6.3.3 Second RS-232-C Serial Board S6-2

SECTION S7 PARTS AND SCHEMATICS

S7.1 DRAWINGS S7-1
S7.2 ERRATA S7-1
S7.3 ORDERING PARTS S7-1

LIST OF TABLES

Table S2-1 Possible Option Locations S2-3
Table S3-1 Required Test Equipment S3-1
Table S3-2 DC Voltages S3-2
Table S3-3 AC Voltages S3-3
Table S4-1 Required Test Equipment S4-1
Table S4-2 Calibration Procedure S4-1
Table S5-1 Register Select S5-5

LIST OF ILLUSTRATIONS

Figure S2-1 Top Cover Removal S2-2
Figure S2-2 RAM/ROM Board or RAM Board Option 50-12A S2-2
Figure S2-3 Model 52A Locater S2-3
Figure S3-1 DC Voltage Connections S3-2
Figure S3-2 AC Voltage Connections S3-3
Figure S3-3 Four-Wire Resistance S3-5
Figure S3-4 Digital I/O Check Interconnections S3-9
Figure S4-1 Four-Wire Measurement S4-7
Figure S5-1 RAM/ROM Board Block Diagram S5-2
Figure S5-2 Option 50-12A Block Diagram S5-3
Figure S5-3 RS-232-C Interface Block Diagram S5-4
Figure S5-4 DCE or DTE Headers S5-5

SAFETY FIRST

Protect yourself. Follow these precautions:

- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

WARNINGS

The case of this unit is not connected to earth ground through the AC Adapter. The case may inductively or electrostatically float to a high voltage if used in a strong electromagnetic or electrostatic field. This presents the potential for a nasty shock. To prevent this, the case may be connected to earth ground using the uninsulated banana jack (⏚) on the rear panel.

Ground for the Digital I/O, IEEE-488, and RS-232-C cards are connected internally to the case. If one of these grounds in external equipment is connected to earth ground, this will make unnecessary the precautionary connection of the paragraph above, when the unit would have floated electrostatically.

Measurement modules "float" to approximately the input common mode voltage. The measurement modules have a shield over their midsection. This shield is connected to analog ground (measurement module input LO). With the case cover off, this shield is exposed. This shield is at input LO potential.

This instrument normally contains a lithium battery. Where lithium is prohibited, such as aboard U.S. Navy ships, verify that the lithium battery has been removed.

Do not recharge, short circuit, disassemble, or apply heat to the lithium battery. Violating this rule could release potential harmful lithium. Observe polarity when you replace the battery.

SECTION S1
HOW TO USE THIS SUPPLEMENT

S1.1 INTRODUCTION

This supplement to the *Models 51 and 52 Data Multimeter Maintenance Manual* contains information relating to the testing, calibrating, and servicing the Model 52A Datalogger. Its purpose is to help keep your Model 52A operating correctly.

S1.2 WHAT IS IN THIS SUPPLEMENT

This supplement contains:

Section S2 — Routine preventive maintenance including removal and replacement procedures of options, accessories, and upgrades for the Model 52A. Section 2 of the *Models 51 and 52 Maintenance Manual* covers the routine preventive maintenance items common to the Models 51, 52, and 52A..

Section S3— Verification procedure for the Model 52A.

Section S4— Calibration procedure for the Model 52A.

Section S5 — Circuit description of the RAM/ROM, the Expansion RAM (Option 50-12A), and the Second RS-232-C (Option 50-15) boards. Section 5 of the *Models 51 and 52 Maintenance Manual* covers the circuit description for circuits common to the Models 51, 52, and 52A.

Section S6— Troubleshooting of the RAM/ROM, the Expansion RAM (Option 50-12A), and the RS-232-C (Option 50-15) boards. Section 6 of the *Models 51 and 52 Maintenance Manual* covers the troubleshooting for circuits common to the Models 51, 52, and 52A.

Section S7— The drawing package contains the assemblies, parts lists, and schematics for the RAM/ROM, expansion RAM, and optional RS-232-C boards. Section 7 of the *Models 51 and 52 Maintenance Manual* contains the drawing package for items common to the Models 51, 52, and 52A.

S1.3 HOW TO USE THIS SUPPLEMENT

How you use the material in this supplement depends on the Model 52A's problems. Before you begin troubleshooting, check instrument setup; refer to the *Model 52A Operator's Manual.*

If the Model 52A makes measurement errors, use the verification procedure (section S3) to confirm the existence of a problem. Then use the calibration procedure (section S4) to correct the problem. If the problem can not be corrected by calibration, consult the troubleshooting guides, section 6.

If you suspect problems in a specific circuit block (optional RS-232-C board for example) refer to the troubleshooting guide for that circuit block and follow the instructions.

Sometimes the source of problems are inconspicuous. Therefore, use the verification procedure to "point" to the suspected circuit board. Then use the troubleshooting guides to further isolate the problem to the suspected circuit block.

Troubleshooting guides lead you in isolating the faulty circuit board and circuit block on the circuit board. The troubleshooting guides will not guide you to the faulty component. To isolate to the component level, use the circuit description to understand the function of the circuit, the schematics to understand the circuit at the component level, and the assembly drawings to locate the circuit and components on the actual circuit board.

S1.4 THE OPERATOR'S MANUAL

This supplement does not cover the operation of the Model 52A.

The *Model 52A Operator's Manual* covers
- Datalogger Introduction.
- Physical Familiarization.
- Model 52A Overview.
- Main Menu/Setup.
- DMM.
- Channel Lists.

Programs.
Alarms.
Math.
Recall Data.
Printing and Plotting Data.
Digital I/O.
Remote Operation.
Model 52A Specifications.

S1.5 CONVENTIONS USED IN THIS MANUAL

In the supplement the Model 52A may be referred to as the "datalogger", "unit", or "instrument".

Digital Logic - Throughout this manual, with the exception of RS-232, positive digital logic notation is used. That is, a "0" or low in a table or in the text means the signal is close to ground, and a "1" or high means the signal is close to the positive rail. In most cases digital lines are dynamic rather than static; thus 0s and 1s represent a digital lines activity relative to a moment in time.

SECTION S2
ROUTINE MAINTENANCE

Section S2 covers Model 52A unique routine maintenance items. Those items common to Models 51, 52, and 52A are covered in section 2 of the Models 51 and 52 Maintenance Manual.

To identify which options are installed in the Model 52A, locate and select CONFIGURATION from the main menu. The display lists the options installed (listed by option number and type) and their location (channel number and option connector - figure S2-3). For details on the configuration menu, refer to paragraph 4.4.2 Configuration Response of the *Model 52A Operator's Manual.*

S2.1 CALIBRATION

To maintain accuracy of the Model 52A, it should be calibrated at least once a year using the calibration procedure contained in section S4. For improved accuracy, perform the zero calibrations more often. The measurement modules, Options 50-1 and 50-2, are the only components that require calibration.

Once the calibration procedure has been performed, the Model 52A holds calibration "adjustments" for as long as the internal RAM battery maintains the memory.

S2.2 FUSE REPLACEMENT

Fuse replacement for the Model 52A is identical to Models 51 and 52 fuse replacement. Paragraph 2.2 of the *Models 51 and 52 Maintenance Manual contains:*

Paragraph 2.2.1 - Power Fuse Replacement.

Paragraph 2.2.2 - Current Overload Fuse Replacement.

Paragraph 2.2.3 - Battery Charger Fuse Replacement.

S2.3 BATTERY REPLACEMENT

Model 52A may contain two or more batteries: the RAM and the RAM/ROM board backup batteries. Added expansion RAM boards (Option 50-12A) also contain their own replaceable RAM batteries.

S2.3.1 Primary Power Battery

Model 52A does not use the primary power battery (Option 50-10).

S2.3.2 RAM Backup Battery

RAM battery replacement for the Model 52A is covered in paragraph 2.3.2 of the *Models 51 and 52 Maintenance Manual.*

S2.3.3 RAM/ROM Board and Option 50-12A Batteries

Batteries on the RAM/ROM board and RAM board Option 50-12A should be tested every time the Model 52A is calibrated. To check these batteries,

1. Remove the top cover; see figure S2-1.
2. Refer to figure S2-3 and table S2-1 for board locations.
3. With a battery in its holder, measure the battery voltage; see figure S2-2. Replace the battery if it measures less than 2.75V, or replace it every five years, whether it is used for backup or not. Replace the battery with a "coin cell" lithium battery.
4. Replace the top cover; see figure S2-1.

CAUTION

> Removing the battery for longer than 15 seconds erases all program setups and data stored in the board's memory.

CAUTION

> Unplugging the RAM/ROM or Option 50-12A board can discharge its battery. Leaving a board unplugged for about 1-1/2 days can completely discharge the board's battery.
>
> To prevent a board's battery from being discharged while a board is outside the unit, either remove the battery or place a piece of paper between the positive clip of the battery holder and the battery.

S2.4 OPTION REPLACEMENT

The following procedure describes the installation and replacement of the following boards:

Expansion RAM Board (Option 50-12A)
Second RS-232-C Board (Option 50-15)
IEEE-488 Board (Option 50-13A)
Digital I/O Board (Option 50-14)

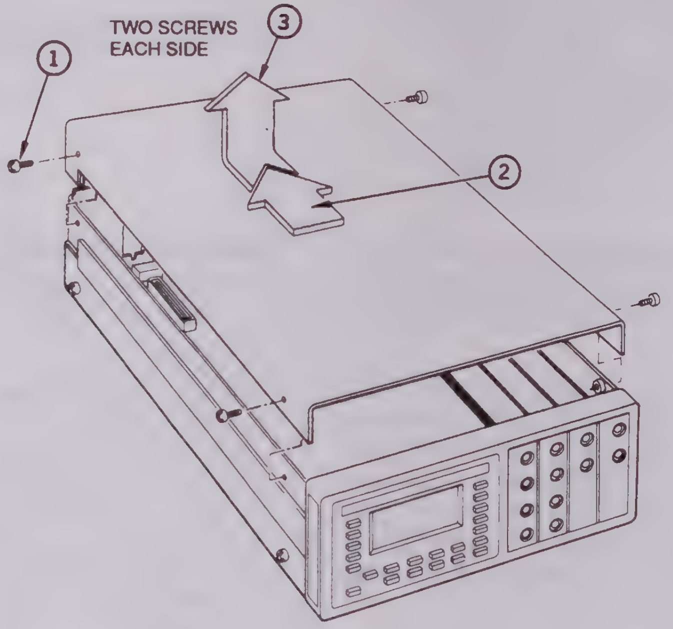


Figure S2-1. Top Cover Removal

NOTE

The RAM/ROM board , shown in figure S2-3, is part of the Model 52A system and only shown for reference.

To identify the options installed, use the CONFIGURATION menu; refer to paragraph 4.4.2 Configuration Response in the *Model 52A Operator's Manual.*

To install, remove, or replace an option board,

1. Disconnect the power source. If using external power, unplug the power source at the rear panel. If using internal power, remove the top cover (figure S2-1) and disconnect the battery connector J6 (figure S2-3).

   CAUTION

   After power is removed, allow longer than 1 minute for power supply discharge before proceeding to the next step, otherwise the option board could be damaged when plugged into the connector.

2. After the top cover has been removed (figure S2-1), remove, install, or replace the option board. Figure S2-3 illustrates the connector location and table S2-1 shows the possible location of the option boards.
3. If applicable, connect the battery (figure S2-3).
4. Replace the top cover (figure S2-1).
5. If applicable, connect the external power source.
6. If a RAM Board (Option 50-12A) has been installed, removed, or relocated, the memory must be cleared by holding down the Clear key while pressing Power on.

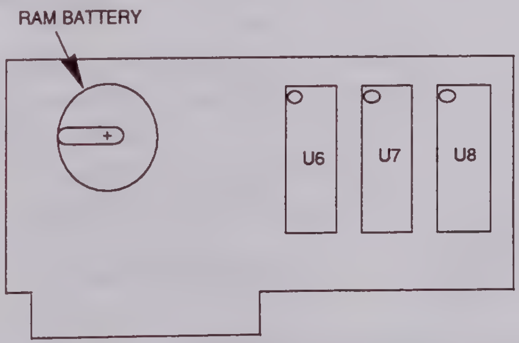


Figure S2-2. RAM/ROM Board or RAM Board Option 50-12A

S2.5 ROM REPLACEMENT

The following procedure describes Read Only Memories (ROMs) replacement.

1. Disconnect the power source. If using external power, unplug the Power connector at the rear

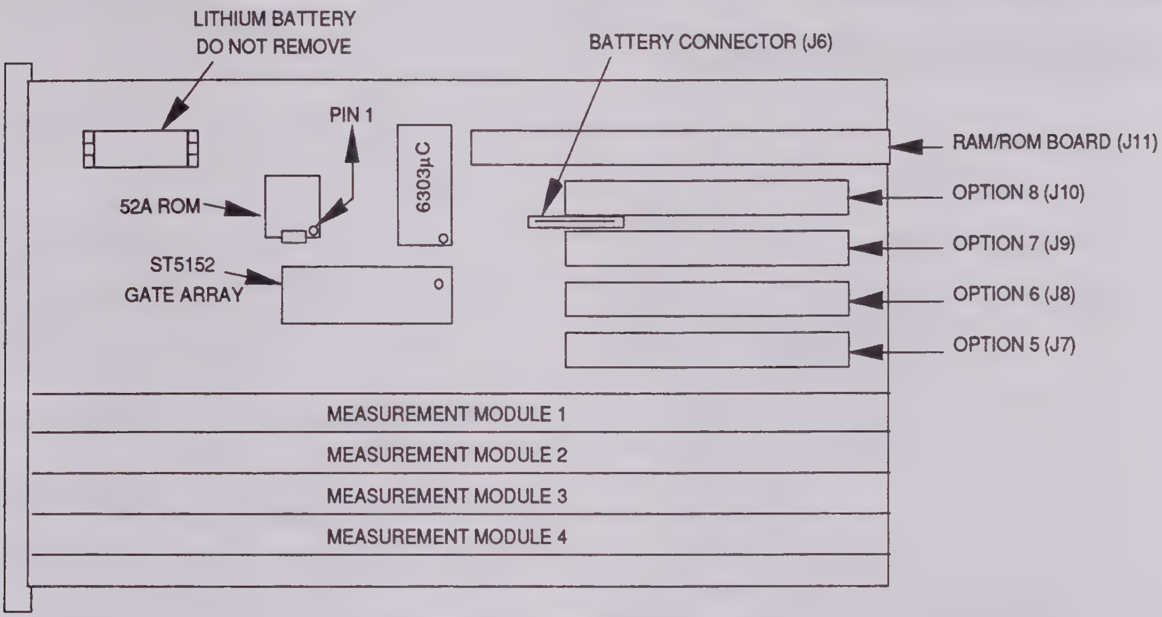

LITHIUM BATTERY
DO NOT REMOVE
BATTERY CONNECTOR (J6)
PIN 1
52A ROM
6303μC
ST5152
GATE ARRAY
RAM/ROM BOARD (J11)
OPTION 8 (J10)
OPTION 7 (J9)
OPTION 6 (J8)
OPTION 5 (J7)
MEASUREMENT MODULE 1
MEASUREMENT MODULE 2
MEASUREMENT MODULE 3
MEASUREMENT MODULE 4

Figure S2-3. Model 52A Locater

Table S2-1. Possible Option Locations

Option Board	**5**	**6**	**7**	**8**
Ram Board (50-12A)	X	X	X	X
IEEE-488 Board (50-13A)				X
Digital I/O Analog Out Board (50-14)	X	X	X	X
Second RS-232-C (50-15)				X

panel. If using internal power, remove the top cover (figure S2-1) and disconnect the Battery Connector J6 (figure S2-3).

CAUTION
After power is removed, allow longer than one minute for power supply discharge, otherwise the RAM/ROM board could be damaged when plugged into the connector.

2. After the top cover has been removed, locate and remove the ROM U5; see figure S2-3. Gently pry loose the ROM and remove it.
3. Plug in the replacement ROM making sure it is placed correctly in the socket. Note the location of pin 1 in figure S2-3.
4. Remove the RAM/ROM board from J11 (figure S2-3). Remove U6, a 27C64, and U7, a 27C101 (figure S2-2).
5. Plug in the replacement U6 and U7, making sure they are placed correctly in the socket. Note the locations of pin 1 (figure S2-2).
6. Replace the RAM/ROM board in J11; verify the board is fully seated in the socket.
7. If applicable, connect the battery (see figure S2-3).
8. Replace the top cover (see figure S2-1).
9. If applicable, connect the power source.
10. When a new ROM is installed, the Model 52A's memory must be cleared by holding down the Clear key while pressing Power on.
11. Verify the ROMs are installed correctly by turning on the power, locating and selecting the CONFIGURATION menu. The configuration screen should show the new software revision on the display.

S2.6 MEASUREMENT MODULE REPLACEMENT

Measurement module replacement is exactly as described in paragraph 2.6 of the *Models 51 and 52 Maintenance Manual.*

SECTION S3
VERIFICATION PROCEDURE

S3.1 VERIFICATION PROCEDURE

This procedure checks out the operation of the following parts of the Model 52A.

Paragraph S3.5	Option 50-1 Measurement Module
Paragraph S3.5	Option 50-2 Measurement Module
Paragraph S3.6	RS-232 Interface (Standard and Option 50-15)
Paragraph S3.7	Option 50-13 IEEE-488 Interface
Paragraph S3.8	Option 50-14 Digital I/O Board
Paragraph S3.9	Option 50-12A Memory Expansion Board
Paragraph S3.10	Option 50-11 Rechargeable Battery
Paragraph S3.11	Option 50-20 Multiplexer

A verification record (paragraph S3.12) follows the verification procedure. Copy the verification record, and use it to record the data from the procedure.

If a check fails, the unit could need calibration. "IF NOT –..." identifies related items in the calibration procedure, section S4. Refer to section S6 Troubleshooting Section 6 or the *Models 51 and 52 Maintenance Manual* if the item can not be calibrated or does not work .

S3.2 REQUIRED TEST EQUIPMENT

The equipment required to perform the verification procedure are listed in table S3-1.

S3.3 INITIAL CHECKS

1. Connect the Model 52A to external power.
2. Set the rear panel DIP switches to the following positions:

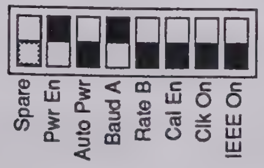


Table S3-1. Required Test Equipment

Equipment	Manufacturer	Specification
Precision Calibrator	Datron 4700 (recommended)	
	Fluke 5100 (alternate)	Wideband Option
Precision Thermometer		±0.1°C Accuracy
Short		<1mΩ
RS-232 Terminals:	ADDS Viewpoint, DEC VT52,VT100 or VT220, Tandy 100 or 200.	Dumb terminal or computer with a terminal mode or program.
Programs:	TERM, VTERM, RED RYDER, or MIRROR.	
IEEE-488 Controller	Commodore 8032. Commodore 64 with IEEE-488 adapter. IBM PC AT or XT with National Instruments or Data Translation IEEE-488 plug-in card.	
Digital I/O Test Connector	Wavetek Accessory 50-32	Wavetek Option 50-14 installed in the Model 52A.

Black in this figure represents the switch handle positions; for example, the Pwr En switch is shown up.

3. Press Power. Main menu is displayed:

```
<DMM
<CHANNEL LISTS
<PROGRAMS
<HELP
```

4. Press Func.

   Select `CALIBRATE`.

Verify the LAST CAL'D date is within the last year.

Verify the line frequency is correct: 50Hz or 60Hz.

NOTE

Changing just the line frequency does not require recalibration of the Model 52A.

S3.4 INITIAL SETUP

1. Set up a test channel list which includes all measurement modules. Refer to Section 6 of the *Model 52A Operator's Manual.*
2. For example: Set up a channel list named TEST.

   Locate and select CHANNEL LISTS from the main menu.

   Select Create New.

   Enter the channel list's name: TEST. Use the ⇕ key to select the character.

   Press Enter four times.

   Press 1, 2, 3, or 4 to select any of the four measurement modules. Or press 1 ±• 4 to select all four measurement modules.

   Press Enter to accept the default setup.

   Function: Vdc,
   Range: Auto Rng.

   Press Enter four times, then Menu to leave the channel list setup menus without running the channel list TEST.

S3.5 MEASUREMENT MODULE CHECKS

The following steps verify the calibration of the Options 50-1 and 50-2 measurement modules.

S3.5.1 DC Voltage Check (Options 50-1 and 50-2)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST from the list of channel lists; and setup all measurement module channels.

   Function: Vdc,
   Range: Auto Rng.

   Refer to paragraph S3.4 or the *Model 52A Operator's Manual.*
3. Short (<1mΩ) the Hi and Lo front panel input connectors of a module. Verify the measurement reads less than six counts. Record the results in the verification record (paragraph S3.12).
4. Repeat step 3 for all remaining measurement modules.

IF NOT – Rezero the measurement module: refer to table S4.2, steps 8 through 15.

5. Disconnect the short.
6. Connect all Hi and Lo input connectors in parallel to the precision dc voltage calibrator; see figure S3-1. In turn apply each of the 16 test voltages listed in table S3-2; verify the measurements fall between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).

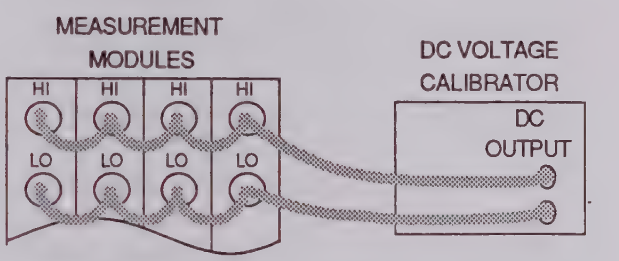


Figure S3-1. DC Voltage Connections

Table S3-2. DC Voltages

Test Voltage	Min. Reading	Max. Reading
+2.000mV	+1.994mV	+2.006mV
–2.000mV	–1.994mV	–2.006mV
+30.000mV	+29.982mV	+30.018mV
–30.000mV	–29.982mV	–30.018mV
+40.000mV	+39.97mV	+40.03mV
–40.000mV	–39.97mV	–40.03mV
+300.000mV	+299.87mV	+300.13mV
–300.000mV	–299.87mV	–300.13mV
+400.000mV	+399.7mV	+400.3mV
–400.000mV	–399.7mV	–400.3mV
+3.00000V	+2.9987V	+3.0013V
–3.00000V	–2.9987V	–3.0013V
+30.0000V	+29.987V	+30.013V
–30.0000V	–29.987V	–30.013V

WARNING
Dangerously high voltages are present in the next two steps.

Test Voltage	Min. Reading	Max. Reading
+300.000V	+299.87V	+300.13V
–300.000V	–299.87V	–300.13V

7. Disconnect the calibrator.

IF NOT – Recalibrate using table S4-2 steps 17 through 30.

S3.5.2 Temperature Check (Options 50-1 and 50-2)

1. Set up the Model 52A as described in paragraph S3.4 .
2. Select TEST from the list of channel lists; and set up all measurement module channels for

   Function: Temp,
   Mods: °C.

   Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*
3. Connect thermocouples to the Hi and Lo inputs of each measurement module. Press Func and select the type of thermocouple; type K thermocouple is the default.
4. Place the thermocouples and precision lab thermometer into a water bath (Water bath temperature of ambient air ±2°C). Once the thermometer has stabilized (about one minute), verify the readings on the Model 52A are within ±1° C of the thermometer.
5. Use step 4 to check remaining measurement modules.

S3.5.3 AC Voltage Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST from the list of channel lists, and set up all measurement modules for

   Function: Vac,
   Mods: AutoRns.

   Refer to paragraph S3.4 or paragraph 6.4.2 the *Model 52A Operator's Manual.*

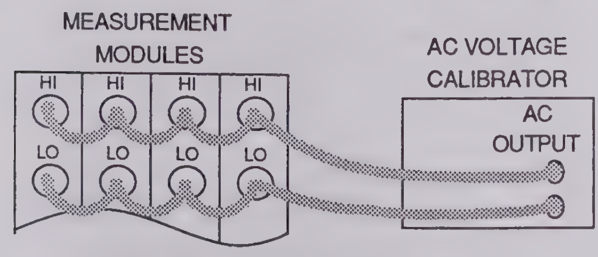


Figure S3-2. AC Voltage Connections

3. Connect all Hi and Lo input connectors in parallel to the precision ac voltage calibrator; see figure S3-2. In turn apply each of the 18 test voltages listed in table S3-3; verify the measurements fall between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).
4. Place the calibrator in the Standby mode.
5. If using the Fluke 5100 calibrator, connect its wideband option outputs to the Hi and Lo input connectors. The calibrator's output must be terminated into 50Ω (±0.1%) at the Hi and Lo inputs.

   If using a Datron 4200 Calibrator, connect its outputs to the Hi and Lo inputs.
6. In turn apply each of the seven test voltages listed in table S3-4; verify the measurement s fall between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).

Table S3-3. AC Voltages

Test Voltage	Freq (Hz)	Min Reading	Max Reading
3.000mV	300	2.925mV	3.075mV
3.000mV	30k	2.900mV	3.100mV
20.000mV	300	19.870mV	20.130mV
20.000mV	10k	19.870mV	20.130mV
20.000mV	30k	19.740mV	20.260mV
40.000mV	10k	39.68mV	40.32mV
40.000mV	30k	39.39mV	40.61mV
200.00mV	50	198.88mV	201.12mV
200.00mV	10k	198.88mV	201.12mV
200.00mV	30k	197.79mV	202.21mV
400.00mV	10k	396.8mV	403.2mV
2.0000V	10k	1.9888v	2.0112V
2.0000V	30k	1.9779V	2.0221V
3.0000V	100	2.9838V	3.0162V
20.000V	10k	19.888V	20.112V
10.000V	30k	9.879V	10.121V

WARNING
Dangerously high voltages are present in the next two steps.

Test Voltage	Freq (Hz)	Min Reading	Max Reading
100.00V	10k	99.29V	100.71V
100.00V	20k	98.79V	101.21V

Table S3-4. AC Voltages

Test Voltage	Freq (Hz)	Min Reading	Max Reading
20.000mV	100k	19.340mV	20.660mV
200.00mV	100k	195.70mV	204.30mV
200.00mV	300k	193.40mV	206.60mV
2.0000V	100k	1.9570V	2.0430V
2.0000V	300k	1.9340V	2.0660V
Change the range to 30V (Range : 30V).			
3.0000V	100k	2.910V	3.090V
3.0000V	300k	2.850V	3.150V

7. Place the calibrator in the standby mode. Disconnect the calibrator.

IF NOT – Recalibrate using table S4-2 steps 36 through 42.

S3.5.4 Zero Resistance Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4 .
2. Select TEST from the lists of channel lists and set up all channel (measurement modules) for

   Function: Ohms,
   Range: 30Ω.

   Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*
3. Connect a short (<1mΩ) across the Hi and Lo inputs of a measurement module to be tested. Verify the measurement is less than 0.005Ω; and record the results in the verification record (paragraph S3.12).
4. Repeat step 3 of this check for each Option 50-1 measurement module.

IF NOT – Recalibrate using table S4-2 steps 44 through 50.

5. Remove the short.

S3.5.5 Resistance (>1kΩ) Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST from the channel lists and setup all channels (measurement modules) for

   Function: Ohms,
   Range: AutoRng.

   Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*
3. In turn connect each of the five test resistors listed below to first Hi and Lo input connectors. Verify the measurements fall between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).

Test Resistor	Min. Reading	Max. Reading
10MΩ	9.979MΩ	10.021MΩ
1MΩ	0.9989MΩ	1.0011MΩ
100kΩ	99.92kΩ	100.08kΩ
10kΩ	9.992kΩ	10.008kΩ
1kΩ	0.9992kΩ	1.0008kΩ

4. Use step 3 to check remaining Option 50-1 measurement modules.

IF NOT – Recalibrate using table S4-2 steps 52 through 55.

5. Disconnect the test resistors.

S3.5.6 Resistance (≤100Ω) Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4. For this check use the four-wire measurement setup. Four-wire measurement requires selecting the rear panel Hi and Lo inputs (1_{00}, 2_{00}, 3_{00}, or 4_{00}).
2. Select TEST from the channel lists and set up all channels (measurement modules) for

   Function: Ohms,
   Range: AutoRng.

   Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*
3. Set up the first measurement module four four-wire resistance measurements; refer to figure S3-3 and paragraph 6.5.5.2 Ohms of the *Model 52A Operator's Manual.*
4. In turn connect each of the two test resistors listed below to the Hi and Lo input connectors. Verify the measurements fall between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).

Test Resistor	Min. Reading	Max. Reading
100Ω	99.92Ω	100.08Ω
10Ω	9.986Ω	10.014Ω

5. Use step 4 to check remaining Option 50-1 measurement modules.

IF NOT- Recalibrate using table S4-2 steps 58 through 60.

6. Disconnect the test resistors.

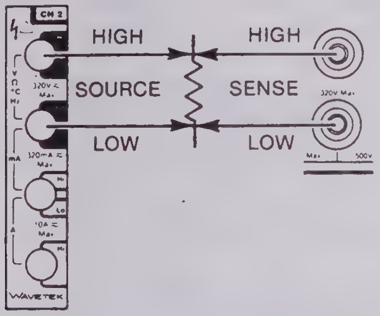


Figure S3-3. Four-Wire Resistance

S3.5.7 DC Current (mA) Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST from the channel lists and set up all channels (measurement modules) for

   Function: Adc,
   Range: mA.

   Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*
3. Connect a precision current calibrator to the middle two inputs (mA) of the first measurement module. In turn apply each of the two test currents listed below; verify the measurements fall between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).

Test Current	Min. Reading	Max. Reading
+20.000mA	+19.980mA	+20.020mA
−20.000mA	−19.980mA	−20.020mA
+200.00mA	+199.85mA	+200.15mA
−200.00mA	−199.85mA	−200.15mA
+1.000mA	+0.994mA	+1.006mA
−1.000mA	−0.994mA	−1.006mA

4. Use step 3 to check remaining Option 50-1 measurement modules.

IF NOT – Recalibrate using table S4-2 steps 64 through 69.

5. Disconnect the calibrator.

S3.5.8 DC Current (A) Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST from the channel lists and set up all channels (measurement modules) for

   Function: Adc,
   Range: 3A.

   Refer to paragraph 6.4.2 of the *Models 52A Operator's Manual.*
3. Connect a precision current calibrator to the bottom two inputs (A) of the first measurement module. In turn apply each of the two test currents listed below; verify the measurements fall between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).

Test Current	Min. Reading	Max. Reading
+1.99999A	+1.9974A	+2.0026A
−1.99999A	−1.9974A	−2.0026A

4. Use step 3 to check remaining Option 50-1 measurement modules.

IF NOT – Recalibrate using table S4-2 step 70 through 72.

5. Change the range to 10A.
6. Connect a precision current calibrator to the bottom two inputs (A) of the first measurement module. In turn apply each of the two test currents listed below; verify the measurements fall between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).

Test Current	Min. Reading	Max. Reading
+1.99999A	+1.997A	+2.003A
−1.99999A	−1.997A	+2.003A

7. Use step 6 to check remaining Option 50-1 measurement modules.

IF NOT – Recalibrate using tables 4-2 steps 73 and 74.

8. Disconnect the current source.

S3.5.9 AC Current (mA) Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST from the channel lists and set up all channels (measurement modules) for

   Function: Aac,
   Range: mA AutoRng.

Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*

3. Connect a precision ac current calibrator to the middle two inputs (mA) of the first measurement module. In turn apply each or the three test currents listed below; verify the measurements fall between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).

Test Current	Freq (Hz)	Min. Reading	Max. Reading
20.000mA	300	19.840mA	20.160mA
3.0000mA	300	2.895mA	3.105mA
200.00mA	300	198.88mA	201.12mA

4. Use step 3 to check remaining Option 50-1 measurement modules.

IF NOT – Recalibrate using table S4-2 steps 75 through 77.

5. Disconnect the current source.

S3.5.10 AC Current (A) Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST from the channel lists and set up all channels (measurement modules) for

   Function: Aac,
   Range: 3A.

   Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*

3. Connect a precision ac current calibrator to the bottom two inputs (A) of the first measurement module. Apply the test current listed below; verify the measurement falls between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).

Test Current	Freq (Hz)	Min. Reading	Max. Reading
1.99999A	300	1.9810A	2.0190A

4. Use step 3 to check remaining Option 50-1 measurement modules.

IF NOT – Recalibrate using table S4-2 steps 78 and 79.

5. Change the range to 10A. Apply the test current listed below; verify the measurement falls between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12).

Test Current	Freq (Hz)	Min. Reading	Max. Reading
1.99999A	300	1.978A	2.022A

6. Use step 5 to check remaining Option 50-1 measurement modules.
7. Place the calibrator in standby, and disconnect it from the unit.

IF NOT – Recalibrate using table S4-2 step 80.

S3.5.11 Frequency Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST channel list from the channel lists and set up all channels (measurement modules) for

   Function: Freq,
   Range: AutoRng,
   Disp: RES 9999999.

   Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*

3. Connect a precision frequency source to the Hi and Lo inputs Apply one of the five test frequencies listed below; verify the measurements fall between the minimum and maximum readings; and record the results in the verification record (paragraph S3.12). Only one of the five frequencies needs to be checked.

Test Resistor	Min. Reading	Max. Reading
1.000000 MHz	0.999975 MHz	1.000025 MHz
100.0000 kHz	99.9975kHz	100.0025 kHz
10.00000 kHz	9.99975 kHz	10.00025 kHz
1.000000 kHz	0.999975 kHz	1.000025 kHz
100.000 Hz	99.9975 Hz	100.0025 Hz

4. Use step 3 to check remaining Option 50-1 measurement modules.
5. Disconnect the frequency source.

IF NOT – Recalibrate using table S4-2 step 81.

S3.5.12 Frequency Sensitivity Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4 INITIAL SETUP.
2. Select TEST from the channel lists and set up all channels (measurement modules) for

   Function: Freq,
   Range: AutoRng,
   Disp: RES 9999999.

Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*

3. Connect all Hi and Lo input connectors to the precision frequency source. Set the frequency source to 10kHz, 350 mVrms. Verify all measurements are the same frequency; and record the results in the verification record (paragraph S3.12).
4. Disconnect the frequency source.

S3.5.13 TTL Sensitivity Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST from the channel lists and set up all channels (measurement modules) for

   Function: `Logic,`
   Mods: `Type TTL.`

   Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*
3. Connect a precision voltage source to all the Hi and Lo inputs.
4. Increase the input voltage from 0.0V to +2.2V. Verify that each channel reading changes from "0" to "1" when the input voltage is between +1.8v and +2.2V. Record the results in the verification record (paragraph S3.12).
5. Decrease the input voltage from +2.2V to 0.0V. Verify that each channel reading changes from "1" to "0" when the input voltage is between +1.0V and +0.6V. Record the results in the verification record (paragraph S3.12).
6. Disconnect the voltage source.

S3.5.14 CMOS5 Sensitivity Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST from the channel lists and set up all channels (measurement modules) for

   Function: `Logic,`
   Mods: `Type CMOS5.`

   Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*
3. Connect a precision voltage source to all the Hi and Lo inputs.
4. Increase the input voltage from 0.0V to +3.7V. Verify that each channel reading changes from "0" to "1" when the input voltage is between +3.3V and +3.7V. Record the results in the verification record (paragraph S3.12).
5. Decrease the input voltage from +3.7V to 0.0V. Verify that each channel reading changes from "1" to "0" when the input voltage is between +1.7V and +1.3V. Record the results in the verification record (paragraph S3.12).
6. Disconnect the voltage source.

S3.5.15 CMOS12 Sensitivity Check (Option 50-1 only)

1. Set up the Model 52A as described in paragraph S3.4.
2. Select TEST from the channel lists and set up all channels (measurement modules) for

   Function: `Logic,`
   Mods: `Type CMOS12.`

   Refer to paragraph 6.4.2 of the *Model 52A Operator's Manual.*
3. Connect a precision voltage source to all the Hi and Lo inputs.
4. Increase the input voltage from 0.0V to +8.4V. Verify that each channel reading changes from "0" to "1" when the input voltage is between +7.2V and +8.4V. Record the results in the verification record (paragraph S3.12).
5. Decrease the input voltage from +8.4 to 0.0V. Verify that each channel reading changes from "1" to "0" when the input voltage is between +6.4V and +3.6V. Record the results in the verification record (paragraph S3.12).
6. Disconnect the voltage source

S3.6 RS-232-C CHECK

The following procedure verifies the operation of the standard RS-232-C port and the optional second RS-232-C port (Option 50-15).

1. Connect an RS-232-C terminal to the appropriate RS-232-C connector on the Model 52A. Refer to paragraph 2.3
2. Set the baud rate of the Model 52A to match the baud rate of the RS-232-C terminal. Refer to paragraphs 2.3, and 4.4.2 (Comm Port 1: Comm Port 1 Setup and RS-232-C Responses; Comm Port 2: Comm Port 2 Setup and RS-232-C Responses) of the *Model 52A Operator's Manual.*
3. Send a "DIR" command to the Model 52A. Refer to section 13, remote operation and paragraph 13.6.15, remote command format, of the *Model 52A Operator's Manual.*
4. Verify the Model 52A returns a listing of all stored channel lists and programs. All directory listings terminate with "*END". Record the results in the verification record (paragraph S3.12).

   For example:

   ```
   TEST.L
   *END
   ```

5 Use step 4 to check the second, optional RS-232-C port. If the second RS-232 port is checked after the standard RS-232 port, the Model 52A must be returned to the local mode before the second port will be recognized as a remote master. To place the Model 52A in the local mode, refer to section 13 of the *Model 52A Operator's Manual.*

   HINT: The quickest way to place the Model 52A in the local mode is to turn the power off and on.

6. Disconnect the RS-232-C terminal.

S3.7 IEEE-488 CHECK

1. Power on the Model 52A.

   NOTE

   The IEEE-488 option will only operate when the Model 52A is powered from an appropriate external power source.

2. From the main menu select `CONFIGURATION`.
3. Verify the Model 52A contains an IEEE-488 (GPIB) board (Option 50-13A). Return to the main menu.
4. Connect the IEEE-488 controller to the Model 52A. Refer to paragraph 2.3 of the *Model 52A Operator's Manual.*
5. Set the IEEE-488 address of the Model 52A to match the IEEE-488 address used by the controller. Refer to paragraph 4.4.1 of the *Model 52A Operator's Manual.*
6. Send a "DIR" command to the Model 52A. Refer to section 13, remote operation, and paragraph 13.6.15, remote command format, of the *Model 52A Operator's Manual.*
7. Verify the Model 52A returns a listing of all stored cannel lists and programs. All directory listings terminate with "*END". If no channel lists or programs are stored in the datalogger, the Model 52A will return only "*END". Record the results in the verification record (paragraph S3.12).

   For example:

   ```
   TEST.L
   *END
   ```

8 Disconnect the IEEE-488 controller.

S3.8 DIGITAL I/O CHECK

1. Power on the Model 52A.
2. From the main menu, select `CONFIGURATION`. Verify the Model 52A contains a digital I/O board. Note the digital I/O channels numbers. Return to the main menu.
3. Set up a channel list that includes all digital I/O channels. Refer to section 6 of the *Model 52A Operator's Manual*.
4. Connect the digital I/Os outputs to its inputs on the same connector; see figure S3-4.

   HINT: Using the Wavetek Accessory 50-32 simplifies the task.

5. Select the channel list from the list and run it. Refer to section 6 of the *Model 52A Operator's Manual.*
6. Compare the displayed output byte with the displayed input byte; they must read the same. The digital output byte should increment each time the output channel is read. Adding a 0.2 second delay to the channel list makes the observations much easier. Record the results in the verification record (paragraph S3.12)
6. Use steps 3 through 6 to check all remaining digital I/O channels.
7. Disconnect the multiplexer.

S3.9 MEMORY EXPANSION CHECK

1. Power on the Model 52A.
2. From the main menu select `CONFIGURATION`.
3. Verify the location and capacity of the RAM boards. Return to the main menu.
4. From the main menu select `MEMORY STATUS,` and note the Total RAM.
5. Verify the total memory capacity from step 3 equals the total capacity displayed in step 4.
6. Return to the main menu. Select the channel list TEST from the channel lists. Locate the channel list item `DATA TO` and select `RAM`; refer to paragraph 6.5.4 of the *Model 52A Operator's Manual.* Once again return to the main menu.
7. Run the channel list TEST for about one minute; refer to paragraph 6.4.4 of the *Model 52A Operator's Manual.*
8. Return to the main menu. Locate and select `RECALL DATA`. From the `Data To` menu, select `Display` and `Sort`. From the `SORT BY` menu, pick `Name` then select `TEST.L` from the list.
9. Verify the display shows the data stored from the channel list. Record the results in the verification record (paragraph S3.12)

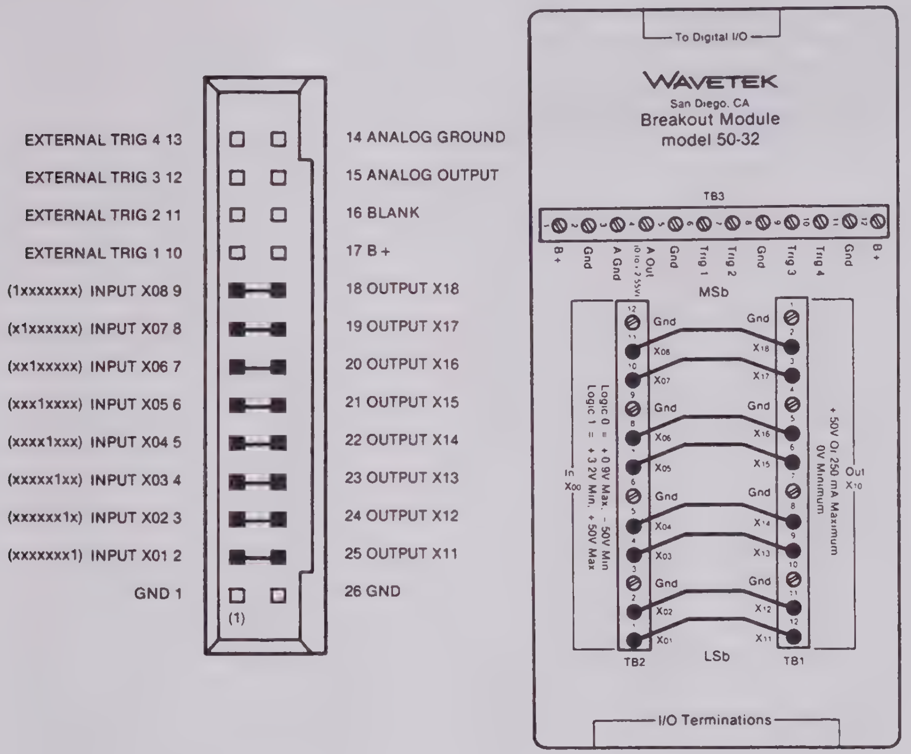

EXTERNAL TRIG 4 13
EXTERNAL TRIG 3 12
EXTERNAL TRIG 2 11
EXTERNAL TRIG 1 10
(1xxxxxxx) INPUT X08 9
(x1xxxxxx) INPUT X07 8
(xx1xxxxx) INPUT X06 7
(xxx1xxxx) INPUT X05 6
(xxxx1xxx) INPUT X04 5
(xxxxx1xx) INPUT X03 4
(xxxxxx1x) INPUT X02 3
(xxxxxxx1) INPUT X01 2
GND 1
(1)
14 ANALOG GROUND
15 ANALOG OUTPUT
16 BLANK
17 B +
18 OUTPUT X18
19 OUTPUT X17
20 OUTPUT X16
21 OUTPUT X15
22 OUTPUT X14
23 OUTPUT X13
24 OUTPUT X12
25 OUTPUT X11
26 GND
To Digital I/O
WAVETEK
San Diego, CA
Breakout Module
model 50-32
TB3
B +
Gnd
A Gnd
A Out
Gnd
Trig 1
Trig 2
Gnd
Trig 3
Trig 4
Gnd
B +
MSb
Gnd
X08
X07
X06
X05
X04
X03
X02
X01
X18
X17
X16
X15
X14
X13
X12
X11
In X00
Logic 0 = + 0.9V Max. - 50V Min
Logic 1 = + 3.2V Min. + 50V Max
Out X10
+ 50V Or 250 mA Maximum
0V Minimum
TB2
LSb
TB1
I/O Terminations

Figure S3-4. Digital I/O Check Interconnections

S3.10 RECHARGEABLE BATTERY CHECK

1. With the Model 52A connected to an external power source and turned on, unplugged the external power.
2. Verify the Model 52A remains on. Record the results in the Verification Procedure paragraph S3.12.
3. Connect the external power.

S3.11 MULTIPLEXER CHECK

1. Connect a multiplexer, Option 53-1, 53-2, or 50-20 to the Model 52A.

   For the Option 53-1 or 53-2, refer to paragraph 3.2.4 or 3.3.4 of the *Options 53-1 and 53-2 Instruction Manual.*

   For the Option 50-20, refer to paragraph B.3 of the *Model 52A Operator's Manual.*

2. Set up the multiplexer for single ended configuration and for multiplexer channel 6.

   For the Option 53-1, refer to paragraph 3.2.3.1 of the *Option 53-1 and 53-2 Instruction Manual.*

   For the Option 53-2, refer to paragraph 3.3.3.1 of the *Option 53-1 and 53-2 Instruction Manual.*

   For the Option 50-20, refer to paragraph B.3 "Single Ended Setup" of the *Model 52A Operator's Manual*

3. Power on the Model 52A.
4. Set up the Model 52A to read a single input on channel 106 using the DMM mode. Refer to section 5 of the *Model 52A Operator's Manual.*

   Locate and select DMM from the main menu.

   Press Chan, 1, 0 ♪, and 6 to enter the multiplexed channel number.

5. Connect a 1.5Vdc source to multiplexer channel number six.
6. Verify the Model 52A display reads the multiplexed input voltage. Record the results in the verification procedure (paragraph S3.12).

S3.12 VERIFICATION RECORD

The verification record provides a place to record data taken during the Verification Procedure. This record should be copied and used with the procedure. The paragraph numbers (¶ S3.5 for example) in the record refers to the paragraph numbers in the procedure.

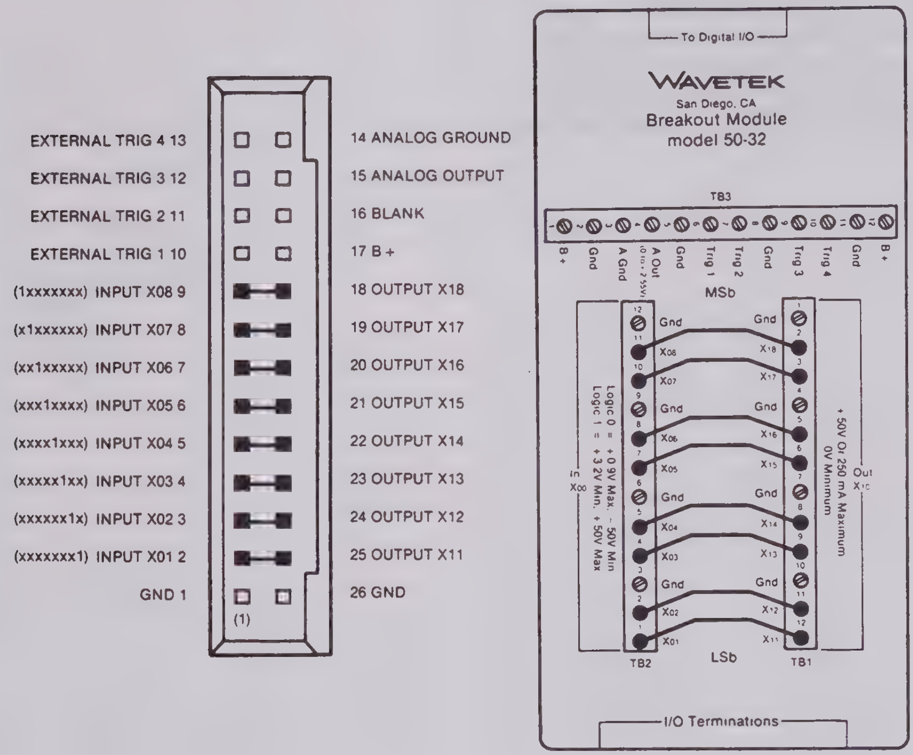

EXTERNAL TRIG 4 13
EXTERNAL TRIG 3 12
EXTERNAL TRIG 2 11
EXTERNAL TRIG 1 10
(1xxxxxxx) INPUT X08 9
(x1xxxxxx) INPUT X07 8
(xx1xxxxx) INPUT X06 7
(xxx1xxxx) INPUT X05 6
(xxxx1xxx) INPUT X04 5
(xxxxx1xx) INPUT X03 4
(xxxxxx1x) INPUT X02 3
(xxxxxxx1) INPUT X01 2
GND 1
(1)
14 ANALOG GROUND
15 ANALOG OUTPUT
16 BLANK
17 B+
18 OUTPUT X18
19 OUTPUT X17
20 OUTPUT X16
21 OUTPUT X15
22 OUTPUT X14
23 OUTPUT X13
24 OUTPUT X12
25 OUTPUT X11
26 GND
To Digital I/O
WAVETEK
San Diego, CA
Breakout Module
model 50-32
TB3
B+
Gnd
A Gnd
A Out
Gnd
Trig 1
Trig 2
Gnd
Trig 3
Trig 4
Gnd
B+
MSb
Gnd
X08
X07
X06
X05
X04
X03
X02
X01
X18
X17
X16
X15
X14
X13
X12
X11
Logic 0 = +0.9V Max. -50V Min
Logic 1 = +3.2V Min. +50V Max
In X00
+50V Or 250 mA Maximum
0V Minimum
Out X10
TB2
LSb
TB1
I/O Terminations

Figure S3-4. Digital I/O Check Interconnections

S3.10 RECHARGEABLE BATTERY CHECK

1. With the Model 52A connected to an external power source and turned on, unplugged the external power.
2. Verify the Model 52A remains on. Record the results in the Verification Procedure paragraph S3.12.
3. Connect the external power.

S3.11 MULTIPLEXER CHECK

1. Connect a multiplexer, Option 53-1, 53-2, or 50-20 to the Model 52A.

   For the Option 53-1 or 53-2, refer to paragraph 3.2.4 or 3.3.4 of the *Options 53-1 and 53-2 Instruction Manual.*

   For the Option 50-20, refer to paragraph B.3 of the *Model 52A Operator's Manual.*
2. Set up the multiplexer for single ended configuration and for multiplexer channel 6.

   For the Option 53-1, refer to paragraph 3.2.3.1 of the *Option 53-1 and 53-2 Instruction Manual.*

   For the Option 53-2, refer to paragraph 3.3.3.1 of the *Option 53-1 and 53-2 Instruction Manual.*

   For the Option 50-20, refer to paragraph B.3 "Single Ended Setup" of the *Model 52A Operator's Manual*
3. Power on the Model 52A.
4. Set up the Model 52A to read a single input on channel 106 using the DMM mode. Refer to section 5 of the *Model 52A Operator's Manual.*

   Locate and select DMM from the main menu.

   Press Chan, 1, 0 ♪, and 6 to enter the multiplexed channel number.
5. Connect a 1.5Vdc source to multiplexer channel number six.
6. Verify the Model 52A display reads the multiplexed input voltage. Record the results in the verification procedure (paragraph S3.12).

S3.12 VERIFICATION RECORD

The verification record provides a place to record data taken during the Verification Procedure. This record should be copied and used with the procedure. The paragraph numbers (¶ S3.5 for example) in the record refers to the paragraph numbers in the procedure.

Model 52A
VERIFICATION RECORD

Date: ______/_______/_______

Serial Number ____

Last Calibration Date (¶ S3.3): ______/_______/_______

Line Frequency (¶ S3.3): ______/_______/_______

DC VOLTAGE CHECK (¶ S3.5.1)

Enter Reading

Test Voltage	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
Short				
+2mV				
-2mV				
+30mV				
-30mV				
+40mV				
-40mV				
+300mV				
-300mV				
+400mV				
-400mV				
+3V				
-3V				
+30V				
-30V				
+300V				
-300V				

TEMPERATURE CHECK (¶ S3.5.2)

Lab Thermometer Reading (water bath temperature): _______________

	Ch 1	**Ch 2**	**Ch 3**	**Ch 4**
Thermocouple Type				
Model 52A Reading				

AC VOLTAGE CHECK (¶ S3.5.3)

Enter reading

Test Voltage	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
3mV @ 300 Hz				
3mV @ 30 kHz				
20mV @ 300 Hz				
20mV @ 10 kHz				
20mV @ 30 kHz				
40mV @ 10 kHz				
40mV @ 30 kHz				
200mV @ 50 Hz				
200mV @ 10 kHz				
200mV @ 30 KHz				
400mV @ 10 kHz				
2V @ 10 kHz				

AC VOLTAGE CHECK (¶S3.5.3) (CONTINUED)

Enter Reading

Test Voltage	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
2V @ 30 kHz				
3V @ 100 Hz				
20V @ 10 kHz				
10V @ 30 kHz				
100V @ 10 kHz				
100V @ 20 kHz				
20mV @ 100 kHz				
200mV @ 100 kHz				
200mV @ 300 kHz				
2V @ 100 kHz				
2V @ 300 kHz				
3V @ 100 kHz				
3V @ 300 kHz				

ZERO RESISTANCE CHECK (¶ S3.5.4)

Enter reading

	Ch 1	**Ch 2**	**Ch 3**	**Ch 4**
Short				

RESISTANCE (>1KΩ) CHECK (¶ S3.5.5)

Enter reading

Test Resistor	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
10MΩ				
1MΩ				
100kΩ				
10kΩ				
1kΩ				

RESISTANCE (<1KΩ) CHECK (¶ S3.5.6)

Enter reading

Test Resistor	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
100Ω				
10Ω				

DC CURRENT (MA) CHECK (¶ S3.5.7)

Enter reading

Test Current	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
+20mA				
-20mA				
+200mA				
-200mA				
+1mA				
-1mA				

DC CURRENT (A) CHECK, RANGE: 3A (¶ S3.5.8)

Enter reading

Test Current	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
+1.99999mA				
-1.99999mA				

DC CURRENT (A) CHECK, RANGE: 10A (¶S3.5.8)

Enter reading

Test Current	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
+1.99999mA				
-1.99999mA				

AC CURRENT (MA) CHECK (¶S3.5.9)

Enter reading

Test Current	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
20mA @ 300 Hz	________	________	________	________
3mA @ 300 Hz	________	________	________	________
200mA @ 300 Hz	________	________	________	________

AC CURRENT (A) CHECK, RANGE: 3A (¶ S3.5.10)

Enter reading

Test Current	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
1.99999A @ 300 Hz	________	________	________	________

AC CURRENT (A) CHECK, RANGE 10A (¶ S 3.5.10)

Enter reading

Test Current	**Ch 1**	**Ch 2**	**Ch 3**	**Ch 4**
1.99999A @ 300 Hz	________	________	________	________

FREQUENCY CHECK (¶ S3.5.11)

Enter reading

	Ch 1	**Ch 2**	**Ch 3**	**Ch 4**
See ¶ S3.5.11, Step 3	________	________	________	________

INPUT SENSITIVITY CHECK (¶ S3.5.12)

Enter reading

	Ch 1	**Ch 2**	**Ch 3**	**Ch 4**
Record displayed frequency	________	________	________	________

INPUT SENSITIVITY (TTL) CHECK (¶ 3.5.13)

Enter transition voltage

	Ch 1	**Ch 2**	**Ch 3**	**Ch 4**
Record "0" to "1" level	________	________	________	________
Record "1" to "0" level	________	________	________	________

INPUT SENSITIVITY (CMOS) CHECK (¶ S3.5.13)

Enter transition voltage

	Ch 1	**Ch 2**	**Ch 3**	**Ch 4**
Record "0" to "1" level	________	________	________	________
Record "1" to "0" level	________	________	________	________

RS-232-C CHECK (¶ S 3.6)

Standard - Model 52A returns directory: ______(✓)
Option 50-15 - Model 52A returns directory: ______(✓)

IEEE-488 CHECK (¶ S3.7)

Model 52A returns directory: _______(✓)

DIGITAL I/O CHECK (¶ S 3.8)

	Ch 5	**Ch 6**	**Ch 7**	**Ch 8**
Digital input reads digital output.	________(✓)	________(✓)	________(✓)	________(✓)

MEMORY EXPANSION CHECK (¶ S3.9)

Total memory capacity from "Configuration" menu equals total memory capacity from "Memory Status" menu: ___________ (✓).

Stored Recall - Correct stored data recalled: ____________ (✓).

MULTIPLEXER CHECK (¶ S3.10)

Cold junction temperatures displayed: ___________ (✓).

SECTION S4
CALIBRATION PROCEDURE

S4.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

S4.2 REQUIRED TEST EQUIPMENT

The test equipment required to perform the calibration procedures are listed in table S4-1.

Table S4-1. Required Test Equipment

Equipment	Manufacturer	Specification
Precision Calibrator	Datron 4700 (Recommended)	
	Fluke 5100 (Alternate)	With wideband option
Precision Thermometer		±0.1°C Accuracy
Precision Frequency Source		2ppm or better, 1MHz WWV down converter or equivalent.
DMM Short		<1mΩ

S.4.3 CALIBRATING THE MODEL 52A

Models 52A uses a calibration process called "Flex-Cal". Flex-Cal means there is no need to open the box or make internal adjustments. All adjustments are made with internal software. To calibrate the Model 52A, set up the unit and apply the proper input as shown in table S4-2. The Model 52A does the rest.

NOTE

The completion of the calibration procedure returns the instrument to correct alignment.

CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS

Instrument specifications are given in Appendix A of the Model 52A Operators Manual.

Table S4-2. Calibration Procedure

Step	Check	Calibrator Set Up	52A Set Up	Remarks
1	Initial Power Procedure		Select CAL ENable on rear panel DIP switch.	See Paragraph 2.3, Item 6.[1] Set all other switches as required.
2			Connect power.	If power on, turn it off.
3	Initialize		Hold in **Clear** while pressing **Power**.	If "Cals Corrupted" appears, select "OK" to load default calibration.

[1] Refer to *Model 52A Operator's Manual.*

Table S4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	52A Set Up	Remarks
4	**Time/Date**		Select Time/Date from main menu. Select Time.	Verify time is correct. If incorrect, set the time (see paragraph 4.4.2).[1] — Time and Date Responses.
			Select Date.	Verify Date is correct. If incorrect, set the date (see paragraph 4.4.2).[1] — Time and Data Responses.
5			Press **Menu**.	
6	Calibration Setup		This calibration procedure requires you to create a channel list that includes each of the measurement modules in the unit.	
7			Select "CHANNEL LIST". Enter Channel List name (for example: "CAL 5"). Press **Func** and select Vdc. Press **Range** and select 30 mV.	For more information, see Section 6[1]. (Set up each channel for Vdc; 20mV.) Allow unit to warmup 5 minutes before calibration.
8	**Vdc** CAL 0		Short Hi to Lo inputs of each channel.	
9			Select the first channel to be zeroed.	To select a channel, push the key next to the channel number (channel number highlighted).
10			Press **Range**. Select 30 mV. Press **Mods**; select CAL and Select Cal 0.	Verify 30 mV range is selected. Wait
11			When the Mods screen appears, press **Range**. Select 300mV. Press **Mods**; select CAL and Cal 0	Wait
12			When the Mods screen appears press **Range** and select 3V. Press **Mods**; select CAL and Cal 0.	Wait
13			When the Mods screen appears, press **Range** and select 30V. Press **Mods**; select CAL and Cal 0.	Wait

---

[1] Refer to *Model 52A Operator's Manual*

Table S4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	52A Set Up	Remarks
14			When the Mods screen appears, press Range and select 300V. Press Mods; select CAL and Cal 0.	Wait
15			When the Mods screen appears press Range and select Auto Rng.	If the reading is >2 counts off, recalibrate zero for the 30 mV range (step 9).
16			Press Enter to return to the channel list display. Repeat steps 9 through 15 for all other channels.	
17	**DC Volts**		Remove short from input.	
18				Connect the calibrator to Hi/Lo inputs.
19			Select the first channel.	
20	+ 20 mV	Set for + 20.000 mV	Press Func and select Vdc. Press Range and select Auto Rng. Press Mods; select CAL and Cal.	Wait until "CALIBRATED" appears.
21	− 20 mV	Set for − 20.000 mV		Wait until "CALIBRATED" appears.
22	+ 200 mV	Set for + 200.000mV		Wait until "CALIBRATED" appears.
23	− 200 mV	Set for − 200.000 mV		Wait until "CALIBRATED" appears.
24	+ 2V	Set for + 2.00000V		Wait until "CALIBRATED" appears.
25	− 2V	Set for − 2.00000V		Wait until "CALIBRATED" appears.
26	+ 20V	Set for + 20.0000V		Wait until "CALIBRATED" appears.
27	− 20V	Set for − 20.0000V		Wait until "CALIBRATED" appears.

Table S4-2. Calibration Procedure (Continued)

WARNING

DANGEROUSLY HIGH VOLTAGES ARE PRESENT IN THE NEXT TWO STEPS.

Step	Check	Calibrator Set Up	52A Set Up	Remarks
28	+ 200V	Set for + 200.000V	Select CAL	Wait until "CALIBRATED" appears.
29	− 200V	Set for − 200.000V		Wait until "CALIBRATED" appears.
30		Output Off (4700) Standby (5100) For safety.	Press Enter to return to the channel list display. Repeat steps 20 through 29.	
31	Temperature Test		Select Func: Temp, Mods: °C, Enter.	
32			Connect thermocouples to Hi/Lo inputs. Select thermocouple type — Range: K, J, T, E, S, or R. (Type K is the default.) Only one type of thermocouple need be tested.	Place thermocouples and precision lab thermometer in a water bath (water bath: ambient ± 2 °C). Wait til the temperature stabilizes (≤60s).
33				Read the thermometer; verify that Model 52A reads ± 1°C of the thermometers' reading.

Table S4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	52A Set Up	Remarks
34				Repeat steps 31 through 33 for each measurement module.

NOTE
If using a multiplexer (Option 50-20, 53-1, or 53-2) for temperature measurements, repeat steps 31 through 33 for every eight multiplexer channels to improve temperature measurements.

35	This completes calibration of the Option 50-2 module. The remaining calibration steps apply to the Option 50-1 module.			
36	**AC Volts**		Select the first channel. Press Func and select Vac. Press Range and select Auto Rng.	These steps calibrate both the Vac and Vac + dc functions. The only evidence you will have that the Vac + dc function is being calibrated will be two clicks of the relays.
37			Disconnect any input to a Option 50-2 module.	
38	20 mV	20.000 mV at 300 Hz	Press Mods and select CAL.	Wait until the relay clicks twice and "CALIBRATED" appears.
39	200 mV	200.000 mV at 300 Hz		Wait until the relay clicks twice and "CALIBRATED" appears.
40	2V	2.00000V at 300 Hz		Wait until the relay clicks twice and "CALIBRATED" appears.

WARNING

DANGEROUSLY HIGH VOLTAGES ARE PRESENT.

CAUTION

Setting the Calibrator to 20V may place the calibrator in standby. If so, reset the calibrator.

Table S4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	52A Set Up	Remarks
41	20V	20.0000V at 300 Hz		Wait until the relay clicks twice and "CALIBRATED" appears.
42	200V	200.000V at 300 Hz		Wait until the relay clicks twice and "CALIBRATED" appears.
43				Repeat steps 37-42 for each of the Option 50-1 modules.
44	**Ohms** 30Ω Zero		Select the first channel. Press Func and select Ohms. Press Range and select 30Ω. Short the Hi and Low input to the first channel. Press Mods; select CAL and Cal 0.	Wait until the Mods menu appears. If the reading is >0.005 repeat the process.
45	300Ω Zero		Press Range and select 300Ω. Press Mods; select CAL and Cal 0.	Wait until the Mods menu appears before continuing on.
46	3kΩ Zero		Press Range and select 3kΩ. Press Mods; select CAL and Cal 0.	Wait until the Mods menu appears before continuing.
47	30kΩ Zero		Press Range and select 30kΩ. Press Mods; select CAL and Cal 0.	Wait until the Mods menu appears before continuing.
48	300kΩ Zero		Press Range and select 300kΩ. Press Mods; select CAL and Cal 0.	Wait until the Mods menu appears before continuing.
49	3MΩ Zero		Press Range twice and select 3MΩ. Press Mods; select CAL and Cal 0.	Wait until the Mods menu appears before continuing.
50	30MΩ Zero		Press Range and select 30MΩ. Press Mods; select CAL and Cal 0.	Wait until the Mods menu appears before continuing.
51				Repeat steps 44 through 50 for all of the Option 50-1 modules channels.

Table S4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	52A Set Up	Remarks
52	Ohms Calibration 10MΩ	10MΩ	Remove short and connect Test Resistor across Hi and Lo inputs. Press **Range** and Select Auto Rng. Press **Mods**; select CAL and Cal.	Wait until "CALIBRATED" appears before continuing
53	1MΩ	1MΩ		Wait until "CALIBRATED" appears before continuing.
54	100kΩ	100kΩ		Wait until "CALIBRATED" appears before continuing.
55	10kΩ	10kΩ		Wait until "CALIBRATED" appears before continuing.
56	1kΩ	1kΩ		Wait until "CALIBRATED" appears before continuing.
57				Repeat steps 53 through 58 for all the Option 50-1 modules.
58	100Ω	100Ω	Connect the 100Ω resistor as shown in figure S4-1.	The following resistance calibration steps require the unit be setup for four-wire measurements (paragraph 6.5.5.2)[1]. It will be easier to select the DMM mode. Press **Menu**, select DMM.[1]

[1] Refer to the *Model 52A Operator's Manual*

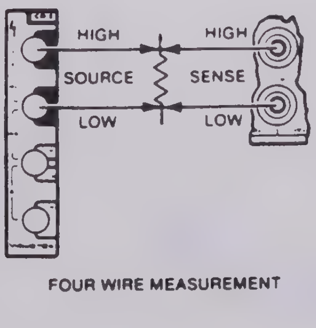


Figure S4-1. Four Wire Measurement

Table S4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	52S Set Up	Remarks
59			Press **Chan** and enter the rear panel subscript (for example, to select the rear panel inputs for channel 1: press **Chan**, **1**, **0**, **0**). Press **Func** and select OHMS. Press **Mods** and select CAL.	Wait until "CALIBRATED" appears before continuing.
60	10Ω	10Ω	Connect the 10Ω resistor as shown in figure S4-1. Press **Mods**; select CAL and Cal.	Wait until "CALIBRATED" appears before continuing.
61	MΩ		Disconnect all inputs. Press **Chan** and select the front panel inputs. Press **Func** and select OHMS. Press **Range** twice and select Auto MΩ. Press **Mods** and select CAL.	Wait until "CALIBRATED" appears before continuing. Reading must be "OVRRNG".
62	100 MΩ TEST	100 MΩ 0.1% resistor	Connect 100 MΩ resistor to front panel inputs.	Reading must be between 95.30 and 103.8MΩ.
63	Optional 1000 MΩ TEST	1000 MΩ 1% resistor	Connect 1000MΩ resistor to front panel inputs.	Reading must be between 960 and 1060MΩ. Repeat steps 53 through 56 and 58 through 62 for all the Option 50-1 channels.
64	**Adc**		Connect the calibrator to the middle two (mA) inputs of the measurement module to be calibrated. Select the first Option 50-1 channel. Press **Func** and select Adc. Press **Range** and select Auto Rng mA.	

Table S4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	52A Set Up	Remarks
65	+ 20 mA	+ 20.000 mA	Press Mods and select CAL.	Wait until "CALIBRATED" appears before continuing.
66	− 20 mA	− 20.000 mA		Wait until "CALIBRATED" appears before continuing.
67	+ 200 mA	+ 200.000 mA		Wait until "CALIBRATED" appears before continuing.
68	− 200 mA	− 200.000 mA		Wait until "CALIBRATED" appears before continuing.
69	+ 1mA TEST	+ 1.000 mA		Reading must be between 0.995 and 1.005 mA. If not check the CAL 0 of 30 mVdc.
70	3A		Press Range and select 3A. Connect the calibrator to the bottom two inputs (A) of the measurement module to be calibrated.	
71	+ 3 A	+ 1.99999 A	Press Mods and select CAL.	Wait until "CALIBRATED" appears before continuing.
72	− 3 A	− 1.99999 A		Wait until "CALIBRATED" appears before continuing.
73	− 10 A	− 1.999999A	Press Range and select 10A.	Wait until "CALIBRATED" appears before continuing. Press Mods and select CAL.
74	+ 10 A	+ 1.99999 A		Wait until "CALIBRATED" appears before continuing. Repeat steps 64 through 74 for all the Option 50-1 channels.
75	**AC Amps**		Connect the calibrator to the middle to (mA) input connectors. Select the first Option 50-1 channel. Press Func and select Aac. Press Range and select Auto Rng mA.	
76	20 mA	20.000 mA at 300 Hz.	Press Mods and select CAL.	Wait until "CALIBRATED" appears before continuing.

Table S4-2. Calibration Procedure (Continued)

Step	Check	Calibrator Set Up	52A Set Up	Remarks
77	200 mA	200.00 mA at 300 Hz.	Press Mods and select CAL.	Wait until "CALIBRATED" appears before continuing.
78	3 A		Connect the calibrator to the bottom two (A) input connectors. Press Range and select 3A.	
79		1.99999A at 300 Hz.	Press Mods and select CAL.	Wait until "CALIBRATED" appears before continuing.
80		1.99999A 300 Hz.	Press Range and select 10A. Press Mods and select CAL.	Wait until "CALIBRATED" appears before continuing. Repeat steps 76 through 80 for all Option 50-1 modules.
81	**Frequency**	Frequency calibration requires a precision frequency source of 1.000000 MHz (100k, 10k, or 100 Hz are acceptable) 2 Vrms.	Connect the precision frequency source to the Hi and Lo inputs to any Option 50-1 module Select any Option 50-1 module. Press Func and select FREQ. Press Mods and select CAL The input sensitivity must be changed if the reference frequency voltage is not 2 Vrms; refer to paragraph 6.5.5.4[1] — Frequency and Period. Press Enter twice.	Only one Option 50-1 module needs to be calibrated. Wait until "CALIBRATED" appears before continuing. This calibrates all the frequency functions on all the Option 50-1 modules.
82			Select Menu and delete the calibration channel list; see paragraph 6.4.3[1].	This deletes the calibration channel list.
83	CAL ENABLE		Select CAL ENable off (switch closed). See paragraph 2.3 item 6[1].	This protects the calibration.

[1] Refer to *Model 52A Operator's Manual.*

SECTION S5
CIRCUIT DESCRIPTION

S5.1 MODEL 52A GENERAL DESCRIPTION

This circuit description covers only those circuits unique to the Model 52A:

The RAM/ROM board - Paragraph S5.2.
The Option 50-12A Expansion RAM board - Paragraph S5.3.
The Option 50-15 Second RS-232-C board - Paragraph S5.4.

Section 5 of the *Models 51 and 52 Maintenance Manual* covers all circuits common to the Models 51, 52, and 52A.

S5.2 RAM/ROM BOARD

S5.2.1 Introduction

The RAM/ROM board, part of the Model 52A system, contains two functions. First, it contains a portion of the Model 52A operating firmware. Second, it contains Model 52A 128K data and program storage RAM. Every unit contains one RAM/ROM board which plugs into motherboard connector J11; see figure S2-3.

The RAM/ROM board is divided into five circuits: the RAM, the ROMs, the address latches, the bank selector, and the control logic; see figure S5-1. The RAM - Random Access Memory, U8, provides storage for Model 52A data and programs. The ROMs- Read Only Memories, U6 and U7, contains part of the Model 52A operating firmware. The motherboard processor accesses the 128K ROM, U7, through the RAM/ROM board operating cycle, while the 8K ROM, U6, is accessed directly by the the motherboard processor. The address latches, U4 and U5, select the RAM or ROM storage locations to be use by the motherboard processor. The bank selector; U3, U1A/B, and U2C; enables either the RAM or ROM (U7 only). The chosen bank maps into an 8K window of the motherboard processor memory space. The control logic, U2A/B and U9A, enables the RAM and ROM outputs, selects RAM and ROM read or write, and clocks the bank selector.

S5.2.2 RAM/ROM Board Operation

Operation of the RAM/ROM board has two distinct phases. In the first phase, the motherboard processor selects and enables the RAM, U8, or the ROM, U7. In the second phase, the motherboard processor performs multiple RAM read and write cycles or ROM read cycles. Refer to the schematic 0103-00-3181 in section S7 of this supplement.

To select a bank, the motherboard processor must initiate a write-only cycle to part of the bank selector, U3. This bank selector is a 6-bit latch which is controlled by its control logic, U1B. The bank select cycle begins when the motherboard logic enables the RAM/ROM board by placing the board enable ($\overline{\mathrm{BD(n)}}$) line low. Next, the address latch, U5, demultiplexes the address/data lines (AD0\ through AD7\) by latching address lines A0 through A7 on the rising edge of address strobe (AS\). The rising edge of the E clock (E\) signals the beginning of the write cycle. The board select logic, U1B, determines when there is a valid write cycle which will clock ($\overline{\mathrm{WR{*}BDN}}$) the bank selector, U3. When the E clock (E\) falls, approximately 400ns later, the bank selector latches the data on the address/data bus (AD0\ through AD5\) into its registers. The outputs from the latch produces the address lines A13, A14, A15, A16, and A17 and $\overline{\mathrm{MEMPROT}}$.

> Address lines A13, A14, A15, and A16 select one of the 16-8K banks. These four lines drive the four most significant RAM and ROM address lines (A13, A14, A15, and A16).
>
> Address line A17 selects the RAM or ROM. When the line is low (0), the RAM, U8, is selected. When the line is high (1), the ROM, U7, is selected.
>
> $\overline{\mathrm{MEMPROT}}$ controls access to the RAM or ROM on this board. A low (0) on this line disables the memories from read and write access regardless of the bank settings. A high (1) on this line places the currently selected bank in the 8K window of the motherboard processor memory map.

The lines $\overline{\mathrm{MEMPROT}}$ and A17 drive the one of four selector, U1A. This selector provides the actual memory selection ($\overline{\mathrm{CS1}}$ enables the 128K ROM, U7, and $\overline{\mathrm{CS2}}$ enables 128K RAM, U8) and access control to the

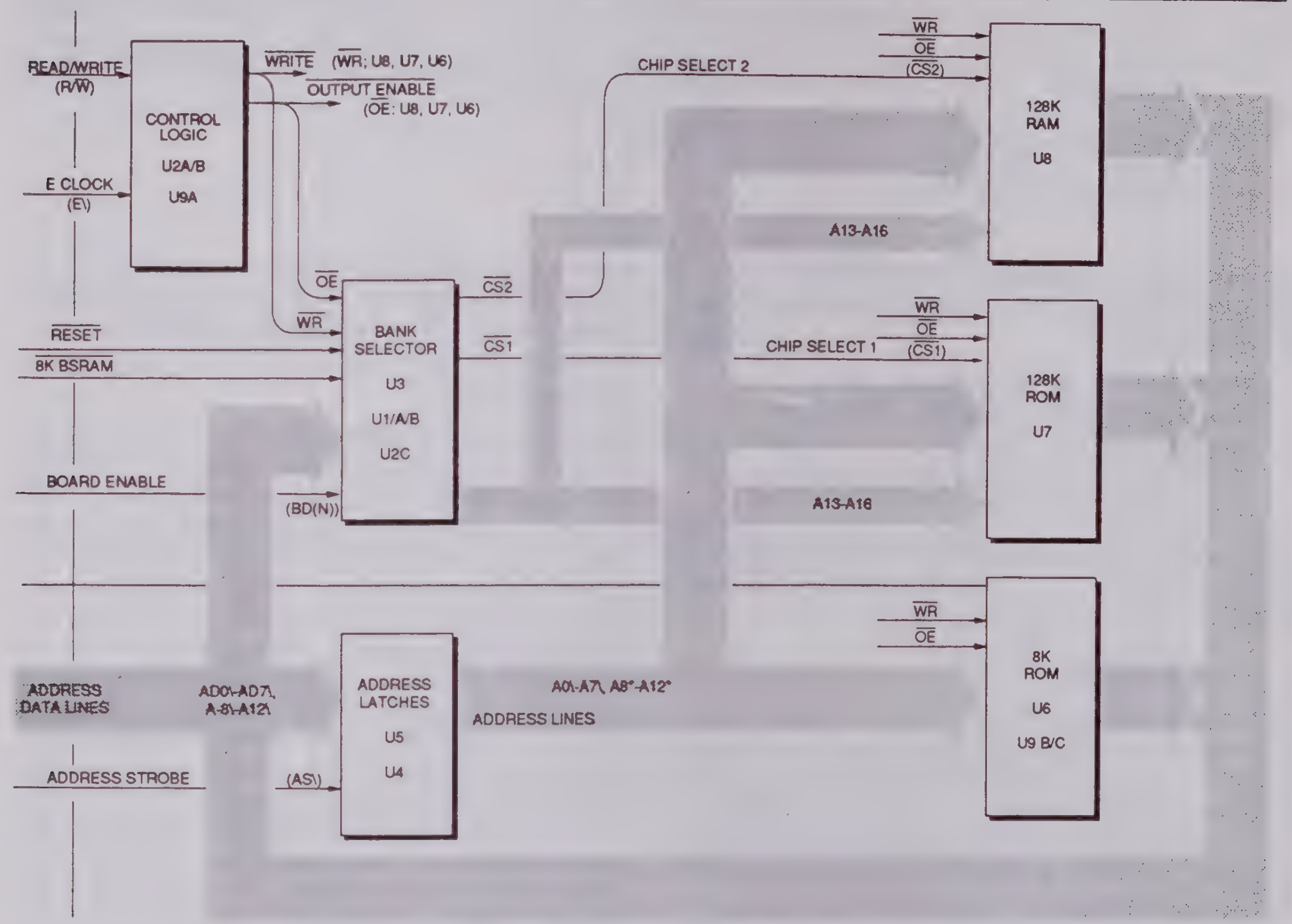

READ/WRITE
(R/W)
E CLOCK
(E\)
CONTROL
LOGIC
U2A/B
U9A
WRITE
(WR; U8, U7, U6)
OUTPUT ENABLE
(OE: U8, U7, U6)
CHIP SELECT 2
WR
OE
(CS2)
128K
RAM
U8
A13-A16
OE
WR
CS2
CS1
RESET
8K BSRAM
BANK
SELECTOR
U3
U1/A/B
U2C
CHIP SELECT 1
(CS1)
128K
ROM
U7
BOARD ENABLE
(BD(N))
A13-A16
ADDRESS
DATA LINES
AD0\-AD7\,
A-8\-A12\
ADDRESS
LATCHES
U5
U4
A0\-A7\, A8*-A12*
ADDRESS LINES
8K
ROM
U6
U9 B/C
ADDRESS STROBE
(AS\)

Figure S5-1. RAM/ROM Board Block Diagram

memories. The RAM/ROM board shares the same 8K banks with the option 50-12A boards. Only the board with its MEMPROT line low can be accessed.

Once selected, the 8K memory bank appears like a standard read/write memory to the motherboard's processor. The processor accesses the memory using a standard memory cycle. During the standard memory cycle, the address latches, U4 and U5, latch the address data presented on the rising edge of the address strobe (AS\). The latched address lines (A0\ through A7\ and A8* through A12*) combine with the already selected bank select lines (A13 through A16) to provide an address for the enabled memory. Data flow to and from the memory is controlled by the write (WR) line and output enable (OE) line.

The 8K ROM, U6, is accessed directly by the motherboard processor. That is, the ROM, U6, can be accessed without enabling the RAM/ROM board (BD(n) line) and without going through the bank-select routine. The motherboard processor enables the ROM by placing the 6KBSROM line low and accessing the ROM using the standard memory cycle.

S5.3 OPTION 50-12A EXPANSION RAM BOARD

S5.3.1 Introduction

The Option 50-12A, an option to the Model 52A system, expands the Model 52A data and program memory beyond the standard 128K. There are two types of option 50-12A boards: the -12A-128 provides 128K additional memory per board and the -12A-256 provides 256K additional memory per board. The Model 52A can hold up to four of these expansion RAM boards. For option 50-12A placement, refer to paragraph S2.4 of this supplement.

The expansion RAM board is divided into four circuits: the RAMs, the address latches, the bank selector, and the control logic; see figure S5-2. The RAM - Random

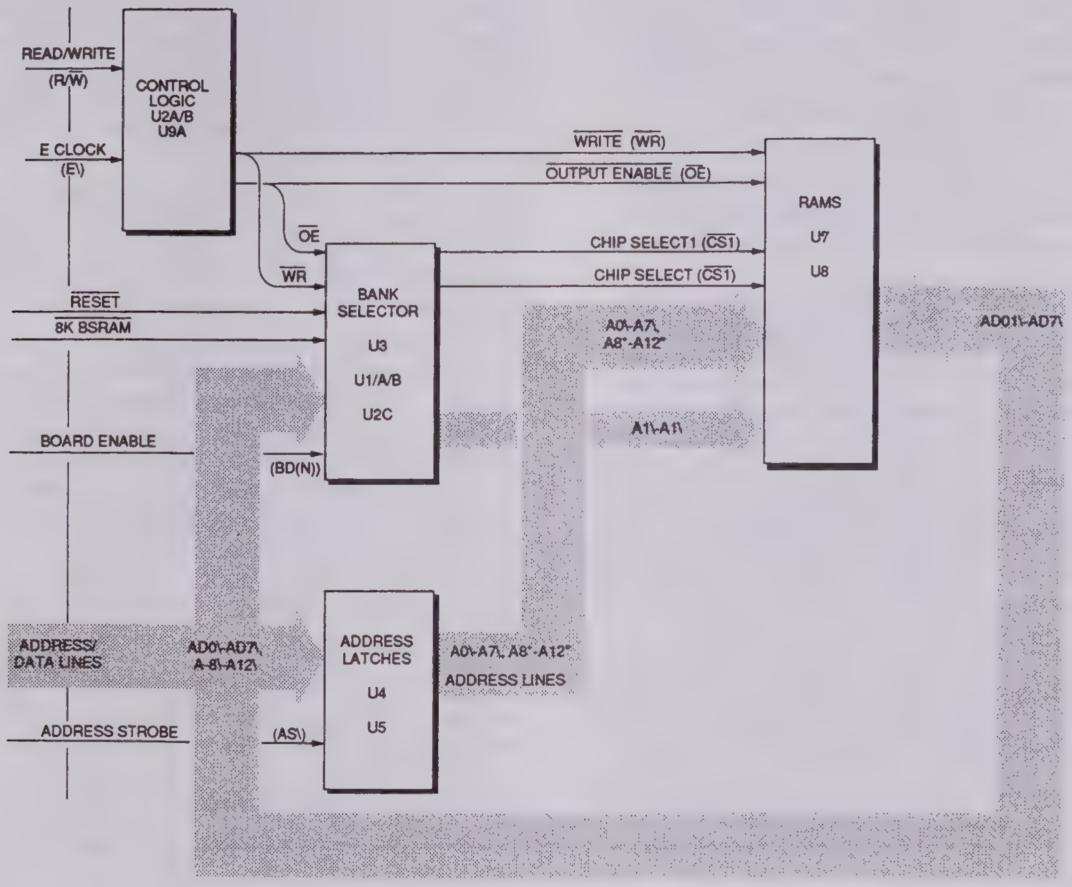

READ/WRITE
(R/W)
CONTROL LOGIC
U2A/B
U9A
E CLOCK
(E\)
WRITE (WR)
OUTPUT ENABLE (OE)
RAMS
U7
U8
OE
WR
CHIP SELECT1 (CS1)
CHIP SELECT (CS1)
RESET
8K BSRAM
BANK SELECTOR
U3
U1/A/B
U2C
A0\-A7\,
A8*-A12*
AD01\-AD7\
A1\-A1\
BOARD ENABLE
(BD(N))
ADDRESS/
DATA LINES
AD0\-AD7\,
A-8\-A12\
ADDRESS LATCHES
U4
U5
A0\-A7\, A8*-A12*
ADDRESS LINES
ADDRESS STROBE
(AS\)

Figure S5-2. Option 50-12A Block Diagram

Access Memory, U7 and U8, provides storage of Model 52A data and programs.

The address latches, U4 and U5, select the storage location for the motherboard processor. The bank selector, U3 and U1A, enables one of the two RAMs and selects the 8K byte section (bank) of the 128K RAM. The chosen bank maps into an 8K window of the Model 52A memory space. The -12A-128 uses 16-8K banks, and the -12A-256 uses 32-8K banks. The control logic; U2A, U2B, and U9A; enables the RAM outputs, selects the RAM read or write, and clocks the bank selector.

S5.3.2 Option 50-12A Operation

Operation of the expansion RAM board has two distinct phases. In the first phase, the motherboard processor selects and enables a RAM bank. In the second phase, the processor performs multiple RAM read and write cycles to the selected RAM bank. Refer to schematic 0103-00-3181 in section S7 of this supplement.

To select a bank, the motherboard processor must initiate a write-only cycle to the bank selector, U3. This bank selector is a 6-bit latch which is controlled by its control logic; U2B, U9A, and U1B. The bank select cycle begins when the motherboard processor enables the expansion RAM board by placing the board enable $\overline{\text{BD(n)}}$ line low. Next, the address latch, U5, demultiplexes the address/data lines (AD0\ through AD7\) by latching address lines A0 through A7 on the rising edge of address strobe (AS\). The rising edge of the E clock (E\) signals the beginning of the write cycle. The control logic; U9A, U2B, and U1B; determines when there is a valid write cycle which will clock ($\overline{\text{WR*BDN}}$) the bank selector, U3. When the E clock (E\) falls, approximately 400ns later, the bank selector latches the data on the address/data bus (AD0\ through AD5\) into its registers.

The outputs from the latch produce the address lines A13, A14, A15, A16, and A17 and $\overline{\text{MEMPROT}}$.

> Address lines A13, A14, A15, and A16 select one of the 16-8K banks These four lines drive the four most significant RAM address lines (A13, A14, A15, and A16).
>
> Address line A17 selects the RAM. When the line is low (0), the RAM, U8, is selected. When the line is high (1), the RAM, U7, is selected.
>
> $\overline{\text{MEMPROT}}$ controls RAM access. A low (0) on this line disables the RAM from read and write access regardless of the bank selection or addresses. A high (1) on this line places the currently selected bank in the 8K window of the motherboard processor memory map.

The lines $\overline{\text{MEMPROT}}$ and A17 drive the one of four selector, U1A. This selector provides the actual RAM chip selection ($\overline{\text{CS1}}$ and $\overline{\text{CS2}}$) and RAM access control to the memories. All option 50-12A boards share the same 8K banks, only the option 50-12A board with its access bit ($\overline{\text{MEMPROT}}$) enabled can be used.

Once selected, the 8K memory bank appears like a standard read/write RAM to the motherboard's processor. The processor accesses the RAM using a standard memory cycle. During the standard memory cycle, the address latches, U4 and U5, latches the address data presented on the rising edge of the address strobe (AS\). The latched address lines (A0\ through A7\ and A8* through A12*) combine with the already selected bank select lines (A13 through A16) to provide an address for the enabled RAM. Data flow to and from the RAM is controlled by the write ($\overline{\text{WR}}$) line and output enable ($\overline{\text{OE}}$) line.

S5.4 OPTION 50-15 SECOND RS-232-C BOARD

S5.4.1 Introduction

The option 50-15, a second RS-232-C board, is a general purpose asynchronous serial adapter which contains a single bidirectional channel that conforms to RS-232-C specifications. This board supports eight different serial bit rates, variable parity and word length, and the necessary hardware control signals for modem interfacing. Only one option 50-15 can be installed in a Model 52A. Option 50-15 must plug into option position 8 (J10); see paragraph S2.4. Model 52A firmware allows the option 50-15 to serve as a remote controller port, as an Model 54 Printer interface, or as a general serial data port.

The option 50-15 consists of four circuits: the Model 52A backplane interface, the Asynchronous Communication Interface Adapter (ACIA), the handshake enable, and the RS-232-C interface; see figure S5-3. The backplane interface demultiplexes address/data line

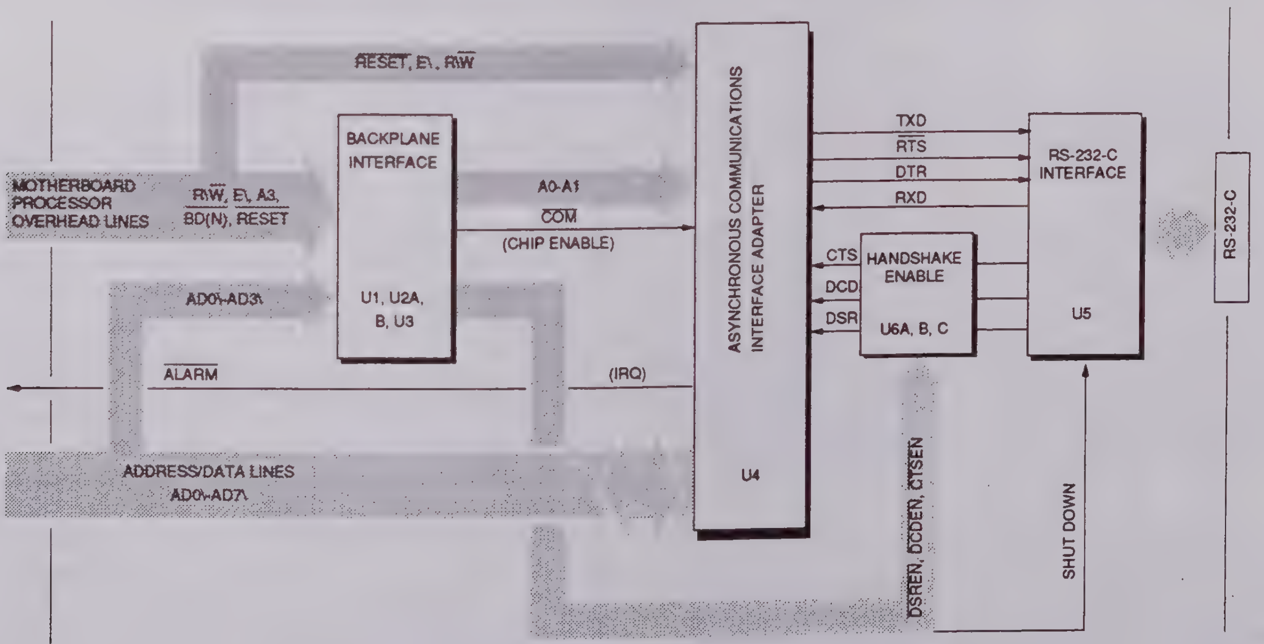

RESET, E\, R/W
MOTHERBOARD PROCESSOR OVERHEAD LINES
R/W, E\, A3, BD(N), RESET
AD0\-AD3\
ALARM
ADDRESS/DATA LINES AD0\-AD7\
BACKPLANE INTERFACE
U1, U2A, B, U3
A0-A1
COM
(CHIP ENABLE)
(IRQ)
ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER
U4
TXD
RTS
DTR
RXD
CTS
DCD
DSR
HANDSHAKE ENABLE
U6A, B, C
DSREN, DCDEN, CTSEN
RS-232-C INTERFACE
U5
SHUT DOWN
RS-232-C

Figure S5-3. RS-232-C Interface Block Diagram

under the control of the motherboard processor overhead lines. The ACIA, U4, is responsible for the serial to parallel and parallel to serial data conversion, the data bit rate generation, the interface handshake line control, and the motherboard interrupt signal generation. The handshake enable controls three line (CTS, DCD, and DSR) between the RS-232-C interface and the ACIA. The RS-232-C line support shifts the interface voltage levels for use with the interface. This option can appear externally either as DCE or DTE which is selectable using the two 26-pin headers; see figure S5-4.

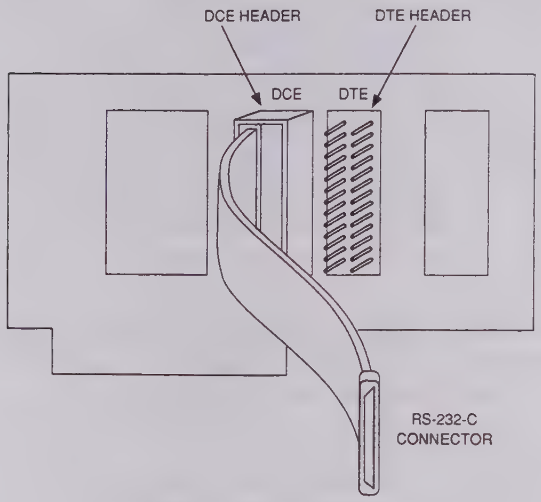


Figure S5-4. DCE or DTE Headers

S5.4.2 Backplane Interface

The backplane interface (see schematic 0103-00-3095 in section S7 of this supplement) consists of the lower-order address latch, U1; the higher-order address latch, U3; and the two decoders, U2A and U2B. The latch, U1, reads the address/data line lower four of the eight-bits (AD0\ through AD3\) on the falling edge of the address strobe (AS\). Two of the latch output lines (A0 and A1) selects ACIA internal registers: RS0 and RS1; see table S5-1. Two other latch output lines (A2 and A3) drive the first decoder, U2A. When this decoder is enabled ($\overline{\text{BD(n)}}$ low), its outputs select the ACIA ($\overline{\text{CS1}}$ low) and enable the second decoder ($\overline{\text{CONTROL}}$ low). When the second decoder, U2B, is enabled, it decodes the E clock line (E\ high) and read/write line (R/$\overline{\text{W}}$ low) to supply the clock ($\overline{\text{WAPORT}}$) for the higher-order address latch, U3. Outputs from this latch ($\overline{\text{DSREN}}$, $\overline{\text{DCDEN}}$, $\overline{\text{CTSEN}}$, and SHUTDOWN) controls the handshake enable circuit; U6A, U6B, and U6C; and the RS-232-C interface, U5.

The option 50-15 board resides in a 32 byte space of Model 52A memory; the memory address is determined by the board location; see paragraph 5.2.8.5.9 of the *Model 52A Maintenace Manual.* The motherboard processor addresses the option 50-15 board using the following mapping (relative to the board base address - 0780_H) :

Offsets 0 through 3 (0780 through 0783) select the ACIA internal registers, RS0 and RS1.
Offsets 4 through 7 (0784 through 0787) control the latch, U3.

S5.4.3 Asynchronous Communications Interface Adapter (ACIA)

The Asynchronous Communication Interface Adapter (ACIA), U4, controls data communications between the motherboard processor and external serial communication devices. The ACIA contains a programmable internal bit rate generator (50 to 19200 Baud). Also, the ACIA has programmable word length, parity type, and number of bit stops. Its serial interface is full duplex with buffered receivers and transmitters.

Model 52A firmware sets up the ACIA using four of the 32 addresses allocated to the board. To enable the ACIA, its $\overline{\text{CS1}}$ line ($\overline{\text{COM}}$) must be pulled low. Two ACIA lines (RS0 and RS1) originating from the backplane interface, U1 select internal ACIA registers; see table S5-1.

Table S5-1. Register Select

RS1	RS0	Register Operation	
		R/$\overline{\text{W}}$ = Low	R/$\overline{\text{W}}$ = High
L	L	Write Transmit Data Register	Read Receiver Data Register
L	H	Program Reset (Data is "Don't care")	Data Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

Model 52A firmware configures the ACIA to generate an IRQ ($\overline{\text{ALARM}}$) whenever the ACIA receives a complete serial character. Then the motherboard reads the receive data register at address offset 0 clearing the IRQ; transmitted data does not use the IRQ. Characters are transmitted by continually reading the status register at address offset 1 until the transmit buffer is empty. The ACIA then writes the byte to be transmitted to the data register at address offset 0. Both the read and write data registers share the same offset but are differentiated by the state of he read/write (R/$\overline{\text{W}}$) line; table S5-1.

Data is transmitted from the ACIA on its TXD line in the following format:

- First, the start bit is sent.
- Second, the serial data is sent starting with the least significant bit.
- Finally, the stop bit (one or more) is sent.

The ACIA receives data via its RXD line in the following format:

- First, the start bit is received.
- Second, the serial data is received starting with the least significant bit.
- Finally, the stop bit (one or more) is received.

The ACIA under Model 52A firmware control monitors the modem control lines (DTR, CTS, DCD, and DSR). Three of these modem control lines (DSR, DCD, and CTS) can be selectively enabled or disabled by the motherboard processor via backplane interface latch, U3, and the handshake enable circuit.

S5.4.4 Handshake Enable

The handshake enable circuit consists of three AND gates; U6A, U6B, and U6C; which enables and disables the modem control lines (CTS, DCD, and DSR) to the ACIA. A low (0) on $\overline{\text{DSEN}}$, $\overline{\text{DCDEN}}$, and $\overline{\text{CTSEN}}$ enables the appropriate gate. A high (1) on these lines disables the signals forcing the CTS, DCD, or DSR lines true.The three control lines ($\overline{\text{DSREN}}$, $\overline{\text{DCDEN}}$, and $\overline{\text{CTSEN}}$) are supplied by the backplane latch, U3.

S5.4.5 RS-232-C Interface

The RS-232-C interface, U5, shifts the boards input and output voltage levels from those used on the RS-232-C lines (±12V) to those used on the option 50-15 board (+V logic). The RS-232-C interface consists of a single device which contains five receiver drivers (RXD, CTS, DCD, and DSR) and five transmitter drivers (DCD, $\overline{\text{TXD}}$, RTS, DTR). Internal charge pumps on the interface help generate the voltage needed for the RS-232-C lines. Four of the driver lines (RXD, CTS, DCD, and DSR) are routed through the handshake enable circuit to the ACIA. A single line to the interface (SHUTDOWN) allows the Model 52A firmware to power down the interface driver.

Two headers, J1 and J2, allows the board to be configured for DTE, J1, or DCE, J2, operation. The RS-232-C connector must plug into one of these headers.

SECTION S6
TROUBLESHOOTING

S6.1 INTRODUCTION

This supplement presents information which when used with the verification procedures (S3), circuit descriptions (sections 5 and S5), calibration procedure (S4), and assembly drawings (section 7 and S7) returns the Model 52A and its options to normal operation. Table 6-1 of the *Models 51 and 52 Maintenance Manual* lists test equipment that may be required for troubleshooting this instrument. Isolating some problems may require user competence with a signature analyzer or logic analyzer.

Appendix B of the *Models 51 and 52 Maintenance Manual* contains a listing of recommended spare parts for user who wish to repair their own units.

S6.2 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the personnel or test equipment to troubleshoot the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the problem and symptoms should be sent with the unit to minimize turnaround time.

Use the following steps when returning Wavetek equipment to Wavetek for repair.

1. **Save the packing material.** Always return equipment to Wavetek in its original packing material and boxes. If you use inadequate packing material, you will have to pay to repair any shipping damage as carriers will not pay claims on incorrectly packed equipment.
2. **Call Wavetek for a Return Authorization.** Wavetek's customer service representative will ask for a name of the person returning the equipment, telephone number, company name, equipment type, and a description of the problem.
3. **Pack and ship the equipment.** Return the equipment to:

   Customer Service
   Wavetek San Diego, Inc.
   9045 Balboa Ave.
   San Diego, CA 92123

S6.3 TROUBLESHOOTING THE MODEL 52A

Troubleshooting the Model 52A is the same as covered in section 6 of the *Models 51 and 52 Maintenance Manual,* except for the RAM/ROM board, expansion RAM board, and second RS-232-C serial board, which are covered in this supplement.

RAM/ROM Board	Paragraph S6.3.1
Expansion RAM Board	Paragraph S6.3.2
Second RS-232-C Board	Paragraph S6.3.3

Those boards common to the Models 51, 52, and 52A are covered in section 6 of the *Models 51 and 52 Maintenance Manual.*

Motherboard	6.4.4.2
Measurement Modules	6.4.4.3
Keyboard	6.4.4.4
Display	6.4.4.5
Digital I/O	6.4.4.6
Expansion RAM Board	6.4.4.7
GPIB Board	6.4.4.8
Multiplexer	6.4.4.9
Rechargeable Battery	6.4.4.10

S6.3.1 RAM/ROM Board

Schematic: 0103-00-3181
Assembly Drawing: 1100-00-3181
Circuit Description: Paragraph S5.2
Verification Procedure: Paragraph S3.9

To troubleshoot the RAM/ROM board,

1. Check the digital control lines to the RAM/ROM board. Verify the overhead signals work correctly (E Clock, Read/Write, Address Strobe, and Board Enable). Refer to paragraph 5.2.5 of the *Models 51 and 52 Maintenance Manual.*
2. Check the digital lines on the RAM/ROM board; refer to paragraph S5.2 of this supplement and paragraph 5.8 of the *Models 51 and 52 Maintenance Manual.*

   ROM - Check the $\overline{\text{6KBSROM}}$ (U9C-10) and $\overline{\text{6KCE}}$ (U6-20) lines; these lines are active during routine unit operation.

ROM - Check the chip enable $\overline{\text{CS1}}$ (U7-22) line; this line is active during the Help, Configuration, and other main menu items. The chip enable ($\overline{\text{CS1}}$) line may be active during the running of channel lists and programs.

3. Verify the battery voltage is greater than 3.0V. Low battery voltage could result in loss of data.

A ROM failure, U6 or U7, may allow the unit to power up, but the main menu may not be displayed.

To check the RAM, create a channel list which stores its data in memory, run the channel list, and recall the stored data. Verify the data is correct.

The Model 52A always fills the RAM on boards with programs, channel lists, etc. beginning with those boards plugged into the lowest numbered option slot (5) to the highest numbered option slot (9 - the RAM/ROM board).

The Model 52A always fills the RAM on boards with data beginning with those boards plugged into the highest numbered option slot (9 - RAM/ROM board) to the lowest numbered option slot (5).

S6.3.2 Expansion RAM Board

Schematic: 0103-00-3181
Assembly Drawing: 1100-00-03182
Circuit Description: Paragraph S5.3
Verification Procedure: Paragraph S3.9

To troubleshoot the RAM board,

1. Check the digital control lines to the expansion RAM board. Verify the overhead signals work correctly (E Clock, Read/Write, Address Strobe, and Board Enable). Refer to paragraph 5.2.5 of the *Models 51 and 52 Maintenance Manual* .
2. Check the digital lines on the expansion RAM board; refer to paragraph S5.3 of this supplement and paragraph 5.8 of the *Models 51 and 52 Maintenance Manual.*
3. Verify the battery voltage is greater than 3.0V. Low battery voltage could result in loss of data.

To check the RAM, create a channel list which stores its data in memory, run the channel list, and recall the stored data. Verify the data is correct.

The Model 52A always fills the RAM on boards with programs, channel lists, etc. beginning with those boards plugged into the lowest numbered option slot (5) to the highest numbered option slot (9 - the RAM/ROM board).

The Model 52A always fills the RAM on boards with data beginning with those boards plugged into the highest numbered option slot (9 - RAM/ROM board) to the lowest numbered option slot (5).

S6.3.3 Second RS-232-C Serial Board

Schematic: 0103-00-3095
Assembly Drawing: 1100-00-3095
Circuit Description: Paragraph S5.4
Verification Procedure: Paragraph S3.6

To troubleshoot the option 50-15 (second RS-232-C) board,

1. Check the digital control lines to the RAM board. Verify the overhead signals work correctly (E Clock, Read/Write, Address Strobe, and Board Enable). Refer to paragraph 5.2.5 of the *Models 51 and 52 Maintenance Manual.*
2. Check the digital lines on the RS-232-C serial board; refer to paragraph S5.4 of this supplement.

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit and, if applicable, the function performed.

7.3 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavekek instrument as quickly as developement and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted inside the shipping carton with this manual.

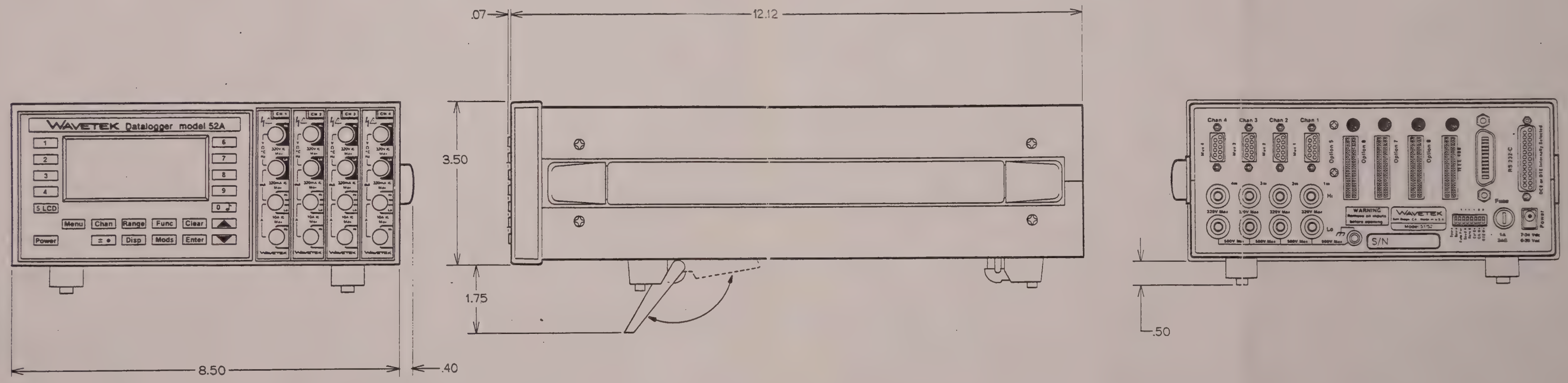
	DRAWING	**DRAWING NUMBER**
Model 52	Outline Drawing	0002-00-0440
	Instrument Schematic	0004-00-0440
	Model 52 Assembly Drawing	1000-00-0490
	Model 52 Parts List	1000-00-0490
	Chassis	
	Assembly	1101-00-2617
	Parts List	1101-00-2617
	Mother Board	
	Schematic	0103-00-1808
	Assembly Drawing	1100-00-1808
	Parts List	1100-00-1808
	Rear Panel	
	Assembly Drawing	1206-00-2618
	Parts List	1206-00-2618
	Keyboard	
	Schematic	0103-00-2414
	Assembly Drawing	1208-00-2414
	Parts List	1208-00-2414
	Bottom Cover	
	Assembly Drawing	1206-00-2620
	Parts List	1206-00-2620
	Top Cover	
	Assembly Drawing	1206-00-2621
	Parts List	1206-00-2621

	DRAWING	DRAWING NUMBER
	Bottom Cover	
	Assembly Drawing	1206-00-2620 *
	Parts List	1206-00-2620 *
	Top Cover	
	Assembly Drawing	1206-00-2621 *
	Parts List	1206-00-2621 *
Option 50-1	*Measurement Module*	
	Assembly Drawing	1000-00-0464 *
	Parts List	1000-00-0464 *
	Table 7-1. Measurement Module Signal Sources and Destinations *	
	Table 7-2. Measurement Module Power Line Destination *	
	PC Board	
	Schematic	0103-00-3178
	Assembly Drawing	1100-00-3178
	Parts List	1100-00-3178
	Parts List	1208-00-2864
	W-10 Cable	
	Assembly Drawing	1207-00-2806 *
	Parts List	1207-00-2806 *
Option 50-2	*Measurement Module*	
	Assembly Drawing	1000-00-0465 *
	Parts List	1000-00-0465 *
	PC Board	
	Schematic (See Option 50-1)	0103-00-3178
	Assembly Drawing	1100-00-3177
	Parts List	1100-00-3177
	Parts List	1208-00-2865
Option 50-10	*Primary Cell Battery*	
	Assembly Drawing	1000-00-0466*
	Parts List	1000-00-0466*
	Battery Holder	
	Assembly Drawing	1207-00-2869*
	Parts List	1207-00-2869*
Option 50-11	*Rechargeable Battery*	
	Assembly Drawing	1000-00-0467 *
	Parts List	1000-00-0467 *
	Recharger Board	
	Schematic	0103-00-2724 *
	Assembly Drawing	1100-00-2724 *
	Parts List	1100-00-2724 *
Option 50-12A	*128K Expansion RAM*	
	Assembly Drawing	1000-00-0511
	Parts List	1000-00-0511

	DRAWING	**DRAWING NUMBER**
	PC Board	
	Schematic (See RAM/ROM Board)	0103-00-3181
	Assembly	1100-00-3182
	Parts List	1100-00-3182
	256K Expansion RAM	
	Assembly Drawing	1000-00-0512
	Parts List	1000-00-0512
	PC Board (See 128K Expansion RAM)	
Option 50-13A	*IEEE-488 Board*	
	Assembly Drawing	1000-00-0525
	Parts List	1000-00-0525
	PC Board	
	Schematic	0103-00-3176
	Assembly Drawing	1100-00-3176
	Parts List	1100-00-3176
	Parts List	1208-00-2866
Option 50-14	*Digital I/O Board*	
	Assembly Drawing	1000-00-0472 *
	Parts List	1000-00-0472 *
	PC Board	
	Schematic	0103-00-3147
	Assembly Drawing	1100-00-3147
	Parts List	1100-00-3147
Option 50-15	*Second RS-232-C Board*	
	Assembly Drawing	1000-00-0540
	Parts List	1000-00-0540
	PC Board	
	Schematic	0103-00-3095
	Assembly Drawing	1100-00-3095
	Parts List	1100-00-3095
Option 50-20	*High Voltage Multiplexer*	
	Outline Drawing	0002-00-0473 *
	Assembly Drawing	1000-00-0473 *
	Parts List	1000-00-0473 *
	PC Board	
	Schematic	0103-00-2656 *
	Assembly Drawing	1100-00-2656 *
	Parts List	1100-00-2656 *
Accessory 50-32	*Digital I/O Module*	
	Outline Drawing	0002-00-0486 *
	Assembly Drawing	1000-00-0486 *
	Parts List	1000-00-0486 *

	DRAWING	**DRAWING NUMBER**
	PC Board	
	Schematic	0103-00-2856 *
	Parts List	1100-00-2856 *
Option 53-1	*32/64 Multiplexer*	
	Reference Schematic	0004-00-0499 *
	Assembly Drawing	1000-00-0499 *
	Parts List	1000-00-0499 *
	PC Board	
	Schematic	0103-00-2877 *
	Assembly Drawing	1100-00-2877 *
	Parts List	1100-00-2877 *
	Parts List	1208-00-2954 *
Option 53-2	*16/32 Multiplexer*	
	Reference Schematic	0004-00-0498 *
	Assembly Drawing	1000-00-0498 *
	Parts List	1000-00-0498 *
	PC Board	
	Schematic	0103-00-2886 *
	Assembly Drawing	1100-00-2886 *
	Parts List	1100-00-2886 *
	Parts List	1208-00-2953 *

REV	ECN	BY	DATE	APP
A	RELEASE PER ERO NO. 9584	MAG	2-22-88	


WAVETEK Datalogger model 52A
1
2
3
4
5 LCD
6
7
8
9
0
Menu
Chan
Range
Func
Clear
Power
± ●
Disp
Mods
Enter
CH 1
CH 2
CH 3
CH 4
WAVETEK
8.50
.40
.07
12.12
3.50
1.75
Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
Option 9
RS 232 C
WARNING
WAVETEK
Fuse
Power
S/N
.50

1. UNIT WEIGHT: 3.85 KG.(8.5 LBS.) NET,
(WITH BATTERY OPTION ADD 1.25 KG.(2.75 LBS.);
SHIPPING (WITHOUT BATTERY): 5.0 KG.(11.00 LBS.).

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN M. GROVES
DATE 2-22-88
PROJ ENGR
3-2-88
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.050
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
OUTLINE DRAWING,
MODEL 52 A
MODEL NO 52A
DWG NO. 0002-00-0539
REV A
CODE IDENT 23338
SHEET 1 OF 1

0002-00-0539 A

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A3708

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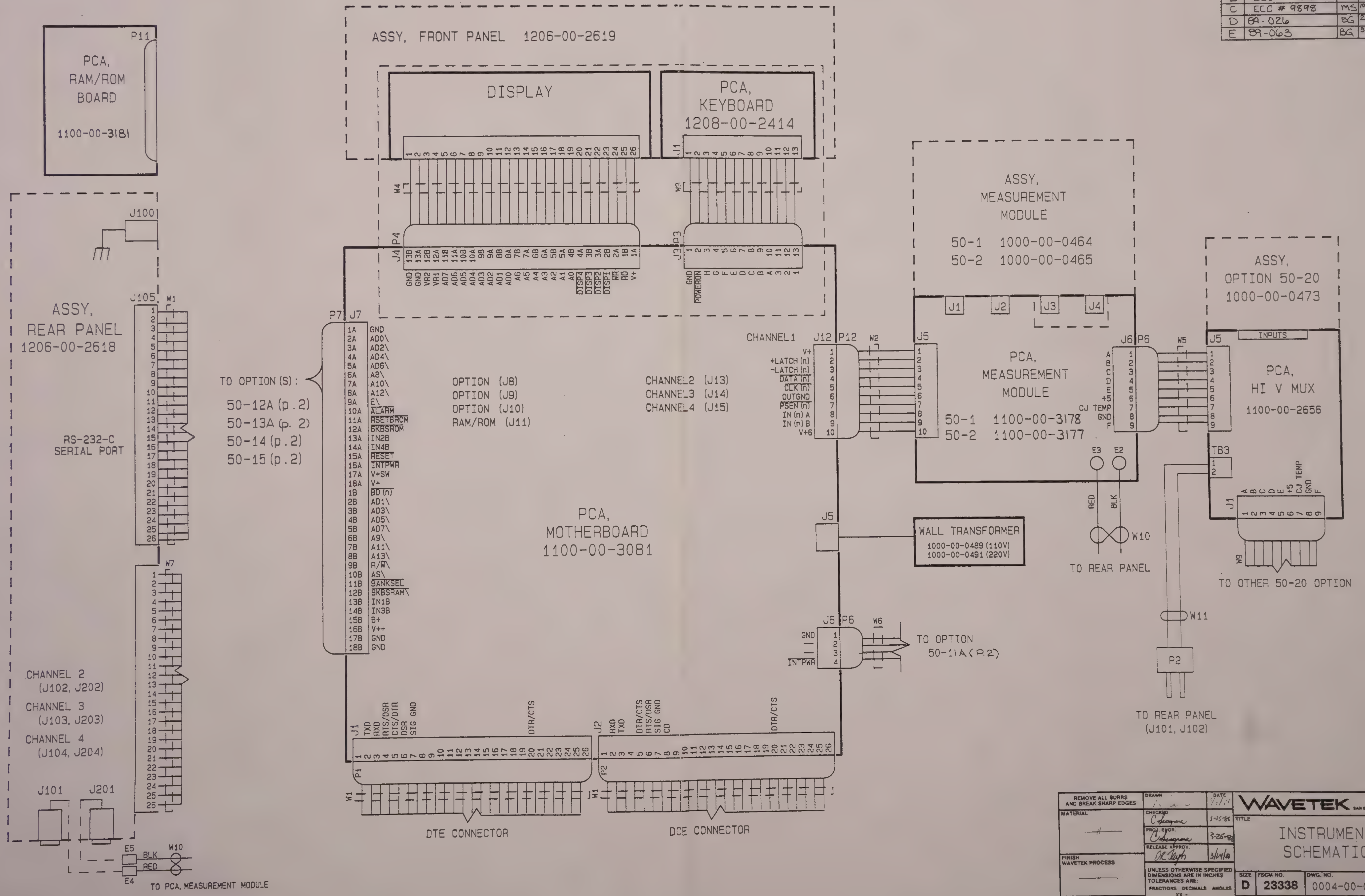
C	ECO # 9898	MS	10/27/88	
D	89-026	BG	2/15/89	
E	89-063	BG	9/16/89	KA



PCA, RAM/ROM BOARD
1100-00-3181
P11
ASSY, FRONT PANEL 1206-00-2619
DISPLAY
PCA, KEYBOARD 1208-00-2414
J1
W4
W3
P4
J4
P3
J3
13B 13A 12B 12A 11B 11A 10B 10A 9B 9A 8B 8A 7B 7A 6B 6A 5B 5A 4B 4A 3B 3A 2B 2A 1B 1A
GND GND VR2 VR1 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 A6 A5 A4 A3 A2 A1 A0 DISP4 DISP3 DISP2 DISP1 WR RD V+
GND POWERON H G F E D C B A 3 2 1
J100
ASSY, REAR PANEL 1206-00-2618
J105
W1
RS-232-C SERIAL PORT
W7
CHANNEL 2 (J102, J202)
CHANNEL 3 (J103, J203)
CHANNEL 4 (J104, J204)
J101
J201
E5
E4
BLK
RED
W10
TO PCA, MEASUREMENT MODULE
TO OPTION (S):
50-12A (p.2)
50-13A (p. 2)
50-14 (p.2)
50-15 (p.2)
P7
J7
1A GND
2A AD0\
3A AD2\
4A AD4\
5A AD6\
6A A8\
7A A10\
8A A12\
9A E\
10A ALARM
11A RSETBROM
12A 6KBSROM
13A IN2B
14A IN4B
15A RESET
16A INTPWR
17A V+SW
18A V+
1B BD (n)
2B AD1\
3B AD3\
4B AD5\
5B AD7\
6B A9\
7B A11\
8B A13\
9B R/W\
10B AS\
11B BANKSEL
12B 8KBSRAM\
13B IN1B
14B IN3B
15B B+
16B V++
17B GND
18B GND
OPTION (J8)
OPTION (J9)
OPTION (J10)
RAM/ROM (J11)
CHANNEL2 (J13)
CHANNEL3 (J14)
CHANNEL4 (J15)
PCA, MOTHERBOARD 1100-00-3081
CHANNEL1
J12
P12
W2
V+
+LATCH (n)
-LATCH (n)
DATA (n)
CLK (n)
OUTGND
PSEN (n)
IN (n) A
IN (n) B
V+6
J5
WALL TRANSFORMER
1000-00-0489 (110V)
1000-00-0491 (220V)
J6
P6
W6
GND
INTPWR
TO OPTION 50-11A (P.2)
J1
TXD RXD RTS/DSR CTS/DTR DSR SIG GND
DTR/CTS
P1
W1
DTE CONNECTOR
J2
RXD TXD DTR/CTS RTS/DSR SIG GND CD
DTR/CTS
P2
DCE CONNECTOR
ASSY, MEASUREMENT MODULE
50-1 1000-00-0464
50-2 1000-00-0465
J1 J2 J3 J4
PCA, MEASUREMENT MODULE
50-1 1100-00-3178
50-2 1100-00-3177
A B C D E +5 CJ TEMP GND F
J6 P6
W5
E3 E2
RED BLK
W10
TO REAR PANEL
ASSY, OPTION 50-20 1000-00-0473
INPUTS
PCA, HI V MUX 1100-00-2656
TB3
J1
A B C D E +5 CJ TEMP GND F
W9
TO OTHER 50-20 OPTION
W11
P2
TO REAR PANEL (J101, J102)

NOTE: UNLESS OTHERWISE SPECIFIED

0004-00-0539 E

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN

CHECKED C. Seagrave 3-25-88

PROJ. ENGR. C. Seagrave 3-25-88

RELEASE APPROV. 3/24/88

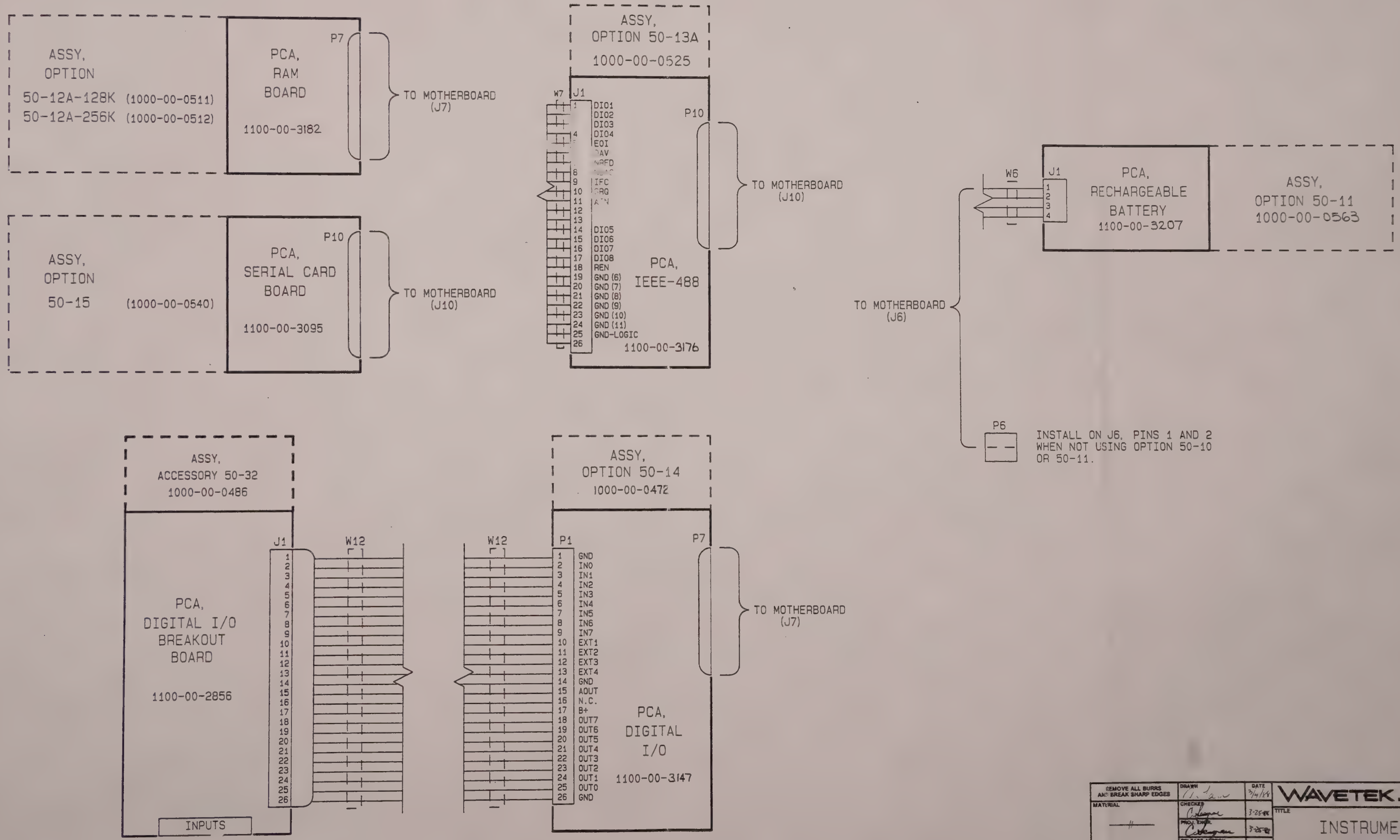
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
INSTRUMENT SCHEMATIC

SIZE D
FSCM NO. 23338
DWG. NO. 0004-00-0539
REV E
SCALE NONE
MODEL 52A
SHEET 1 OF 2

REV	ECO	BY	DATE	APP
SEE SHT #1				

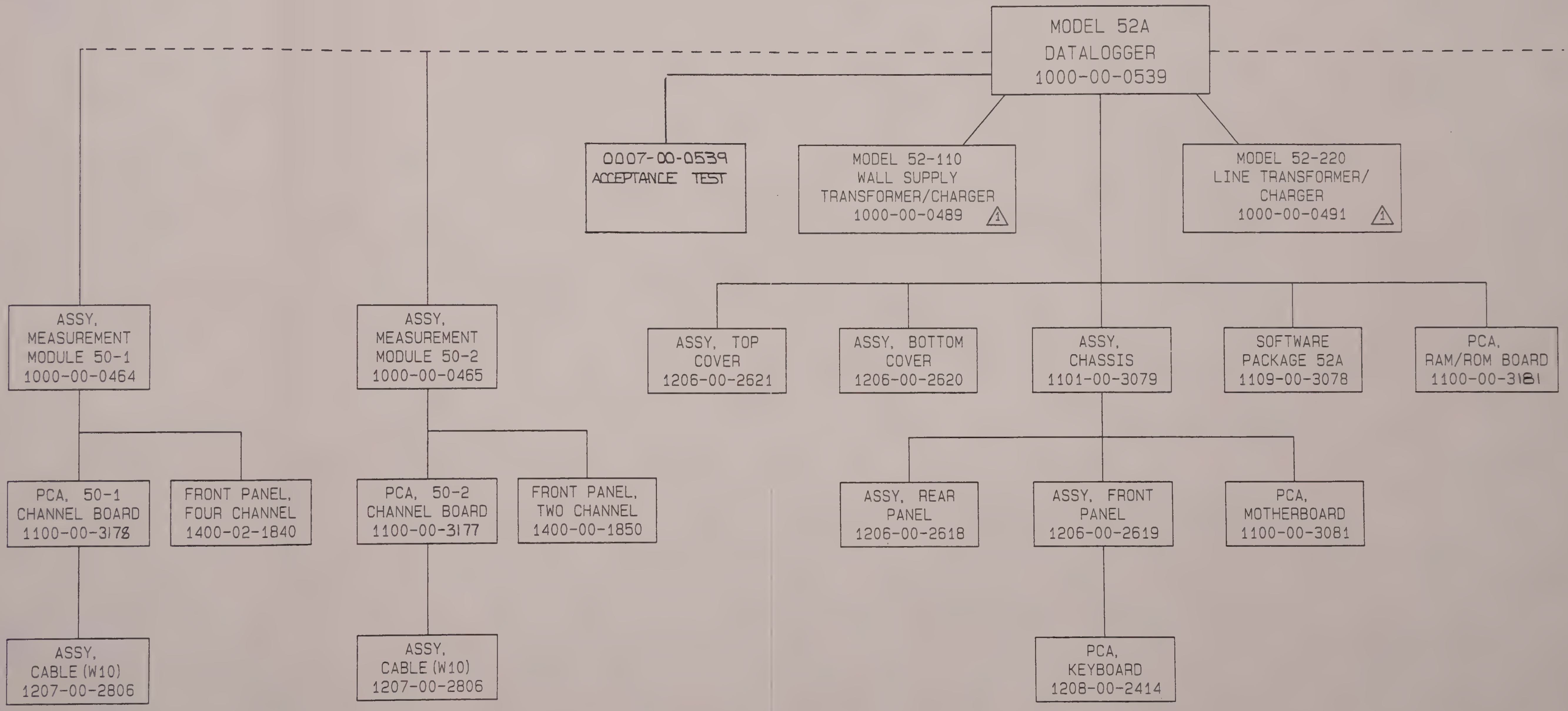

ASSY,
OPTION
50-12A-128K (1000-00-0511)
50-12A-256K (1000-00-0512)
PCA,
RAM
BOARD
1100-00-3182
P7
TO MOTHERBOARD
(J7)
ASSY,
OPTION
50-15 (1000-00-0540)
PCA,
SERIAL CARD
BOARD
1100-00-3095
P10
TO MOTHERBOARD
(J10)
ASSY,
OPTION 50-13A
1000-00-0525
W7
J1
1 DIO1
DIO2
DIO3
4 DIO4
EOI
DAV
NRFD
8 NDAC
9 IFC
10 SRQ
11 ATN
12
13
14 DIO5
15 DIO6
16 DIO7
17 DIO8
18 REN
19 GND (6)
20 GND (7)
21 GND (8)
22 GND (9)
23 GND (10)
24 GND (11)
25 GND-LOGIC
26
PCA,
IEEE-488
1100-00-3176
P10
TO MOTHERBOARD
(J10)
W6
J1
1
2
3
4
PCA,
RECHARGEABLE
BATTERY
1100-00-3207
ASSY,
OPTION 50-11
1000-00-0563
TO MOTHERBOARD
(J6)
P6
INSTALL ON J6, PINS 1 AND 2
WHEN NOT USING OPTION 50-10
OR 50-11.
ASSY,
ACCESSORY 50-32
1000-00-0486
PCA,
DIGITAL I/O
BREAKOUT
BOARD
1100-00-2856
INPUTS
J1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
W12
W12
ASSY,
OPTION 50-14
1000-00-0472
P1
1 GND
2 IN0
3 IN1
4 IN2
5 IN3
6 IN4
7 IN5
8 IN6
9 IN7
10 EXT1
11 EXT2
12 EXT3
13 EXT4
14 GND
15 AOUT
16 N.C.
17 B+
18 OUT7
19 OUT6
20 OUT5
21 OUT4
22 OUT3
23 OUT2
24 OUT1
25 OUT0
26 GND
PCA,
DIGITAL
I/O
1100-00-3147
P7
TO MOTHERBOARD
(J7)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 3/4/88	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL —	CHECKED	3-25-88	TITLE INSTRUMENT SCHEMATIC	
	PROJ. ENGR.	3-25-88		
FINISH WAVETEK PROCESS —	RELEASE APPROV.	3/24/88		
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 0004-00-0539	REV E
DO NOT SCALE DRAWING			SCALE NONE · MODEL 52A	SHEET 2 OF 2

0004-00-0539 E

REV	ECO	BY	DATE	APP
A	FOR RELEASE PER ERO # 9584	MAG	3-3-88	
B	ECO #9816	M.S.	8/4/88	NM
C	ECO # 9898	MS	10/27/88	
D	ECO # 89-026	BG	3/6/89	KA


MODEL 52A
DATALOGGER
1000-00-0539
0007-00-0539
ACCEPTANCE TEST
MODEL 52-110
WALL SUPPLY
TRANSFORMER/CHARGER
1000-00-0489
1
MODEL 52-220
LINE TRANSFORMER/
CHARGER
1000-00-0491
1
ASSY,
MEASUREMENT
MODULE 50-1
1000-00-0464
ASSY,
MEASUREMENT
MODULE 50-2
1000-00-0465
ASSY, TOP
COVER
1206-00-2621
ASSY, BOTTOM
COVER
1206-00-2620
ASSY,
CHASSIS
1101-00-3079
SOFTWARE
PACKAGE 52A
1109-00-3078
PCA,
RAM/ROM BOARD
1100-00-3181
PCA, 50-1
CHANNEL BOARD
1100-00-3178
FRONT PANEL,
FOUR CHANNEL
1400-02-1840
PCA, 50-2
CHANNEL BOARD
1100-00-3177
FRONT PANEL,
TWO CHANNEL
1400-00-1850
ASSY, REAR
PANEL
1206-00-2618
ASSY, FRONT
PANEL
1206-00-2619
PCA,
MOTHERBOARD
1100-00-3081
ASSY,
CABLE (W10)
1207-00-2806
ASSY,
CABLE (W10)
1207-00-2806
PCA,
KEYBOARD
1208-00-2414

△1 SELECT ONE TRANSFORMER/CHARGER.

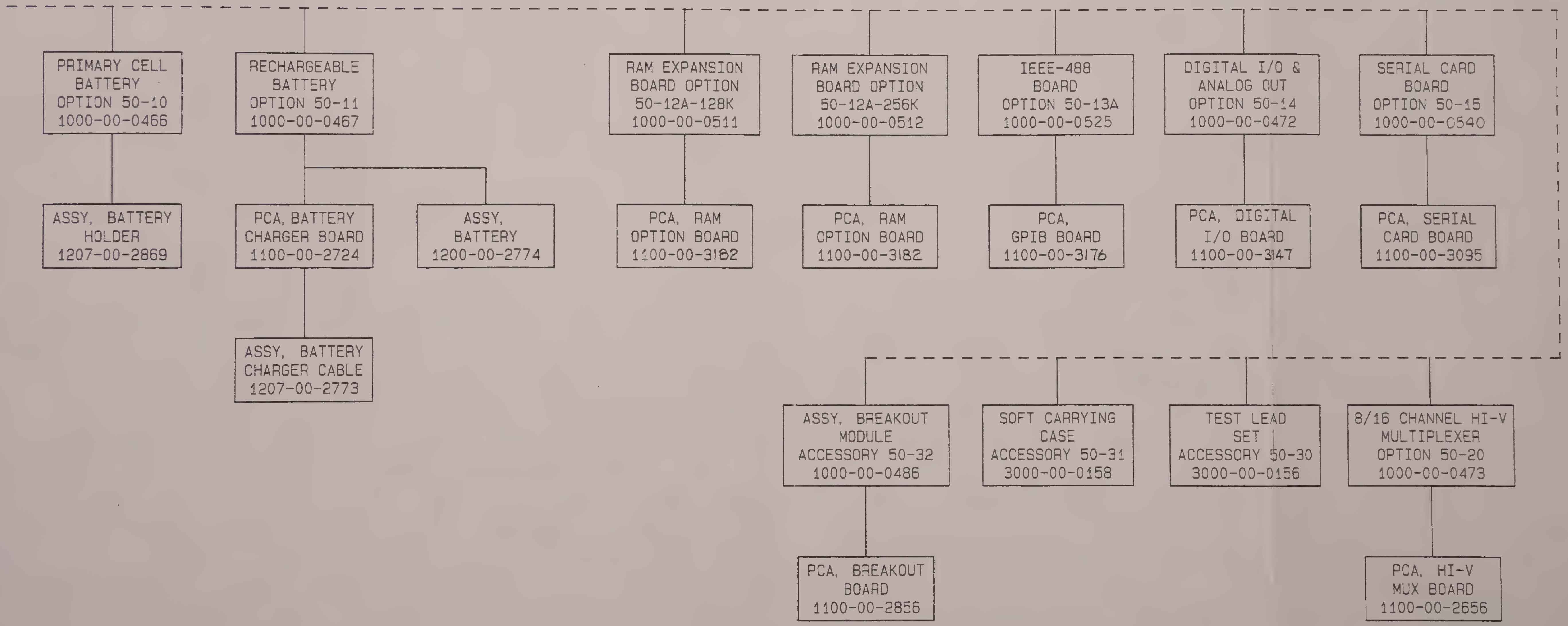
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 3/7/88	**WAVETEK** SAN DIEGO • CALIFORNIA
MATERIAL —	CHECKED N. S. Smith	3/31/88	TITLE PRODUCT STRUCTURE DRAWING
	PROJ. ENGR	3-25-88	
FINISH WAVETEK PROCESS —	RELEASE APPROV.	3/24/88	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 0010-00-0539 · REV D
DO NOT SCALE DRAWING			SCALE NONE · MODEL 52A · SHEET 1 OF 2

0010-00-0539 D

REV	ECO	BY	DATE	APP

SEE SHT #1


PRIMARY CELL BATTERY OPTION 50-10 1000-00-0466
ASSY, BATTERY HOLDER 1207-00-2869
RECHARGEABLE BATTERY OPTION 50-11 1000-00-0467
PCA, BATTERY CHARGER BOARD 1100-00-2724
ASSY, BATTERY 1200-00-2774
ASSY, BATTERY CHARGER CABLE 1207-00-2773
RAM EXPANSION BOARD OPTION 50-12A-128K 1000-00-0511
PCA, RAM OPTION BOARD 1100-00-3182
RAM EXPANSION BOARD OPTION 50-12A-256K 1000-00-0512
PCA, RAM OPTION BOARD 1100-00-3182
IEEE-488 BOARD OPTION 50-13A 1000-00-0525
PCA, GPIB BOARD 1100-00-3176
DIGITAL I/O & ANALOG OUT OPTION 50-14 1000-00-0472
PCA, DIGITAL I/O BOARD 1100-00-3147
SERIAL CARD BOARD OPTION 50-15 1000-00-0540
PCA, SERIAL CARD BOARD 1100-00-3095
ASSY, BREAKOUT MODULE ACCESSORY 50-32 1000-00-0486
PCA, BREAKOUT BOARD 1100-00-2856
SOFT CARRYING CASE ACCESSORY 50-31 3000-00-0158
TEST LEAD SET ACCESSORY 50-30 3000-00-0156
8/16 CHANNEL HI-V MULTIPLEXER OPTION 50-20 1000-00-0473
PCA, HI-V MUX BOARD 1100-00-2656

0010-00-0539 C

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN G. Tan	DATE 3/9/88	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	CHECKED N. S. Mult	3/31/88	TITLE PRODUCT STRUCTURE DRAWING
	PROJ. ENGR.	3-25-88	
FINISH WAVETEK PROCESS —	RELEASE APPROV.	3/24/88	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 0010-00-0539 · REV D
DO NOT SCALE DRAWING			SCALE NONE · MODEL 52A · SHEET 2 OF 2

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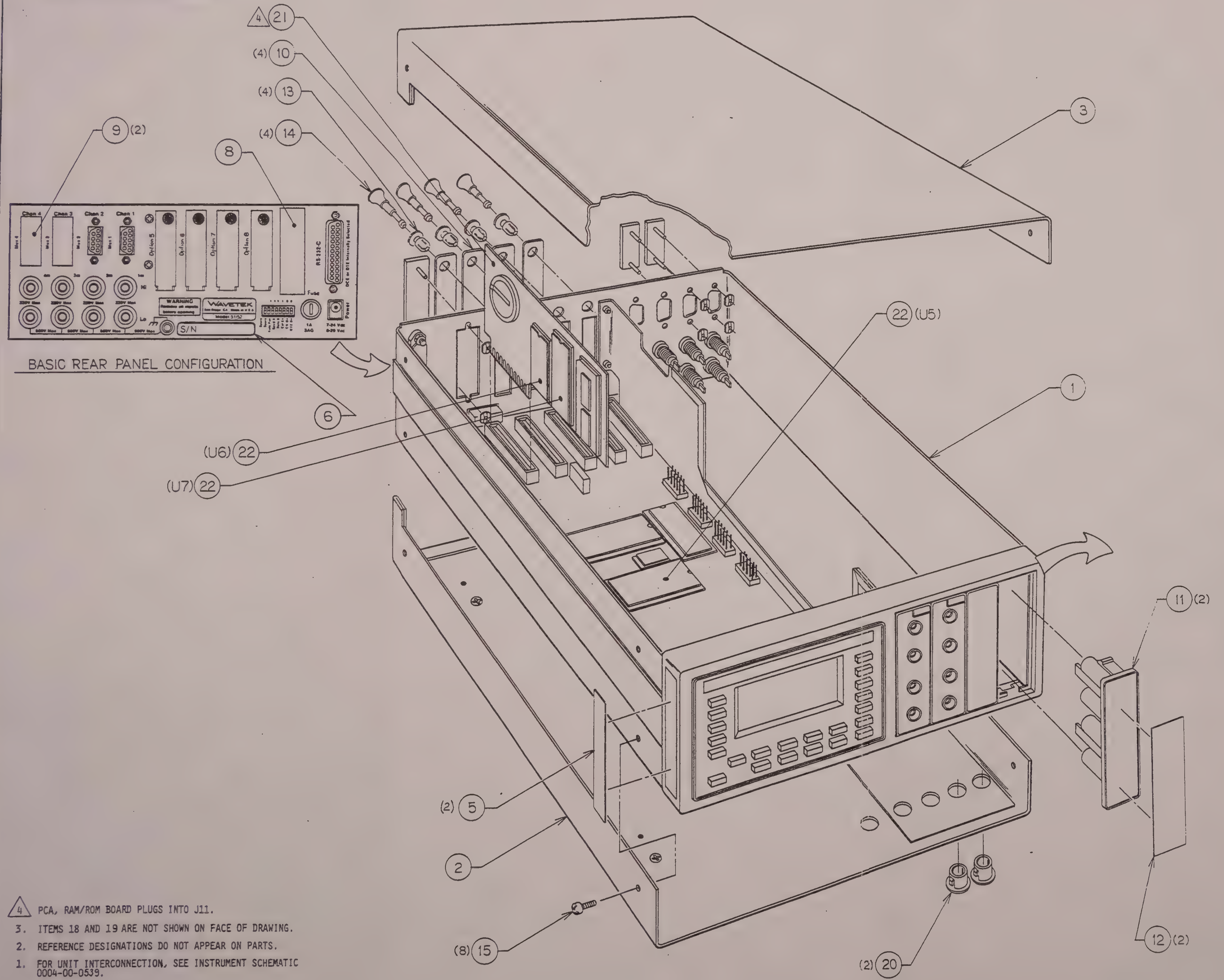
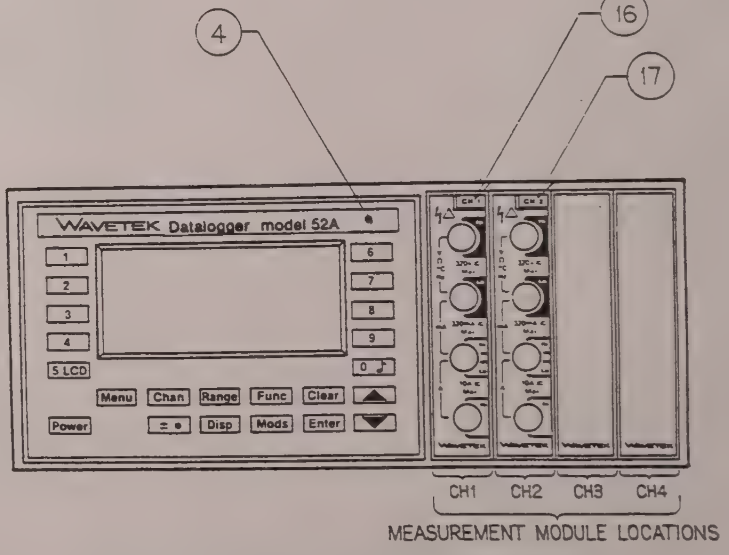
REV	ECN	BY	DATE	APP
A	RELEASE PER ERO NO. 9584	MAG	2-22-88	CJ
B	9892 (SOFTWARE UPDATE)	BG	9/88	
C	9976 (SOFTWARE UPDATE	BG	9/88	
D	89-026	BG	3/16/89	KA



4 21
(4) 10
(4) 13
(4) 14
9 (2)
8
3
22 (U5)
1
6
(U6) 22
(U7) 22
11 (2)
(2) 5
2
(8) 15
(2) 20
12 (2)
Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS-232-C
DCE or DTE Internally Selected
Hi
Lo
WARNING
WAVETEK
Model 51/52
S/N
Fuse
1A
3AG
Power
7-24 Vdc
8-20 Vac

BASIC REAR PANEL CONFIGURATION



4
16
17
WAVETEK Datalogger model 52A
1
2
3
4
5 LCD
6
7
8
9
0
Menu
Chan
Range
Func
Clear
Power
±
Disp
Mods
Enter
CH1
CH2
CH3
CH4
MEASUREMENT MODULE LOCATIONS

SAMPLE FRONT PANEL CONFIGURATION

4. PCA, RAM/ROM BOARD PLUGS INTO J11.
3. ITEMS 18 AND 19 ARE NOT SHOWN ON FACE OF DRAWING.
2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0539.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0539

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN M. GROVES DATE 2-22-88
PROJ ENGR C. Leagrave 3-3-88
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
MODEL 52A
DATALOGGER
MODEL NO. 52A
DWG NO. 1000-00-0539
REV D
CODE IDENT 23338
SHEET 1 OF 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	OUTLINE DRAWING-52A	0002-00-0539	WVTK	0002-00-0539	1
NONE	SCHEMATIC, INSTRUMENT-52A	0004-00-0539	WVTK	0004-00-0539	1
NONE	ACCEPTANCE TEST PROCEDURE	0007-00-0539	WVTK	0007-00-0539	1
NONE	PCA, RAM/ROM BD 52A	1100-00-3181	WVTK	1100-00-3181	1
1	ASSY, CHASSIS	1101-00-3079	WVTK	1101-00-3079	1
22	SOFTWARE PACKAGE-52A	1109-00-3078	WVTK	1109-00-3078	1
2	ASSY, BOTTOM COVER	1206-00-2620	WVTK	1206-00-2620	1
3	ASSY, TOP COVER	1206-00-2621	WVTK	1206-00-2621	1
NONE	OPERATORS MANUAL 52A	1300-00-0539	WVTK	1300-00-0539	1.5
6	SERIAL TAG MODEL 602	602-6950	WVTK	1400-01-6950	1
11	FRONT PANEL, BLANK CHANNEL	52-0860	WVTK	1400-02-0860	2
16	LABEL CHANNEL 1	52-1110	WVTK	1400-02-1110	1
17	LABEL, CHANNEL 2	52-1120	WVTK	1400-02-1120	1
18	LABEL CHANNEL, 3	52-1130	WVTK	1400-02-1130	1
19	LABEL CHANNEL, 4	52-1140	WVTK	1400-02-1140	1

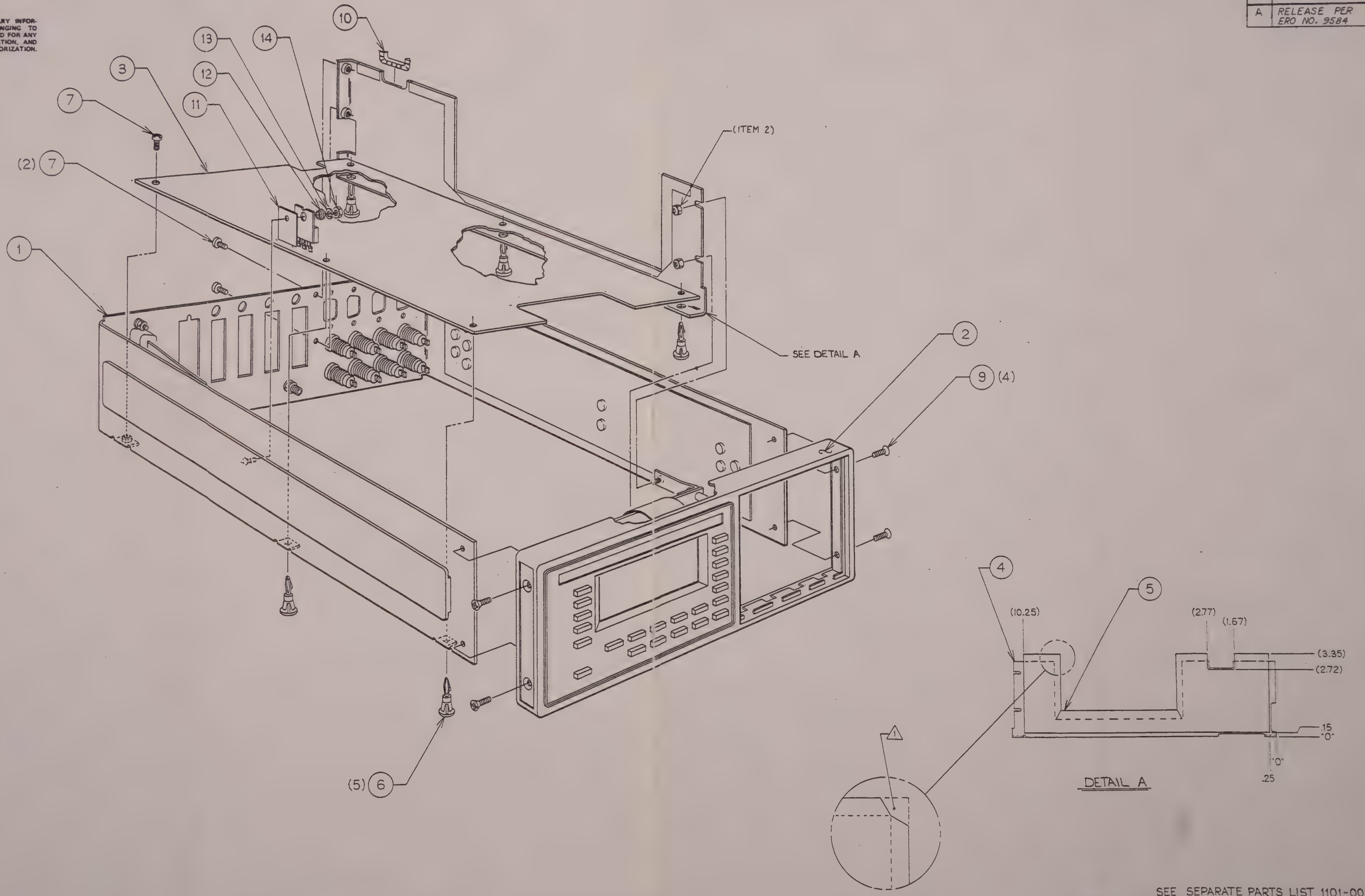
WAVETEK PARTS LIST	TITLE MODEL 52A DATALOGGER	ASSEMBLY NO. 1000-00-0539 PAGE 1	REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
12	DECAL, BLANK CHANNEL	52-1150	WVTK	1400-02-1150	2
5	DECAL, SIDE TRIM	52-1200	WVTK	1400-02-1200	2
10	COVER, DIGITAL I/O	1400-02-1593	WVTK	1400-02-1593	4
4	DECAL, FRONT PANEL	1400-02-4270	WVTK	1400-02-4270	1
15	SCREW MACHINE, PANHEAD, PHLPS, W/NYLOCK PATCH	6-32X3/16 PAN LOK BLK	CMRCL	2800-23-6103	8
20	PLUG BUTTON, NYLON, 17/32 HEAD, BLACK	2633	HEYCO	2800-35-0007	2
13	GROMMET, NYLATCH, 1/4 HOLE ONE OF TWO PARTS	HN4G43-1	HART	2800-60-0004	4
14	PLUNGER, NYLATCH, 1/4 HOLE, ONE OF TWO PARTS	HN4P43-4-1	HART	2800-60-0005	4
NONE	TEST LEAD SET, 48 INCH	3000-00-0156	WVTK	3000-00-0156	1
NONE	101-18 INSERT	101-18	WVTK	3300-00-0015	1
NONE	CARTON	101-18A	WVTK	3300-01-0012	1
8	COVER, CONNECTOR CUT-OUT	12-24R BLACK	PEPER	3300-03-0002	1
9	COVER, CONNECTOR	10-9 BLACK	PEPER	3300-03-0003	2

WAVETEK PARTS LIST	TITLE MODEL 52A DATALOGGER	ASSEMBLY NO. 1000-00-0539 PAGE 2	REV D

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE				DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES		WAVETEK Wavetek Inc.
x/x ± 1/64	.xxx ± .005	.xx ± .01	∠ ± 1°	DRAWN	DATE	TITLE PARTS LIST MODEL 52A DATALOGGER
MATERIAL:				CHKD		
				ENG APPR.		
FINISH:				MFG APPR.		SIZE D · MODEL NO. 52A · DRAWING NO. 1000-00-0539 · REV D
				ISSUED		SCALE: · CODE IDENT 23338 · SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	RELEASE PER ERO NO. 9584	MAG	2-22-88	


10
13
14
3
12
7
11
(2) 7
1
(ITEM 2)
SEE DETAIL A
2
9 (4)
4
5
(10.25)
(2.77)
(1.67)
(3.35)
(2.72)
.15
"0"
"0"
.25
1
DETAIL A
(5) 6

1 SMOOTH INSULATOR (ITEM 5) OVER EDGES OF CENTER SHIELD (ITEM 4) AND FOLD IT DOWN ONTO REAR SIDE, FOLD CORNER OVER FIRST THEN FOLD ADJACENT SIDES OVER ON TOP OF CORNER, HOLDING IT DOWN.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1101-00-3079

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN M. GROVES DATE 2-22-88
PROJ ENGR C [illegible] 3-2-98
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
ASSEMBLY, CHASSIS

MODEL NO 52A
DWG NO. 1101-00-3079
REV A
CODE IDENT 23338
SHEET 1 OF 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
3	PCA, MOTHER BD-52A	1100-00-3081	WVTK	1100-00-3081	1
1	ASSY, REAR PANEL	1206-00-2618	WVTK	1206-00-2618	1
2	ASSY, FRONT PANEL-52	1206-00-2619	WVTK	1206-00-2619	1
4	CENTER SHIELD	1400-02-3213	WVTK	1400-02-3213	1
5	INSULATOR, CENTER SHIELD	1400-02-3220	WVTK	1400-02-3220	1
12	WASHER	B51547F015	MOT	2800-11-0015	1
14	NUT, HEX, 4-40	MS35649-244	COML	2800-14-4100	1
7	SCREW, 4-40X1/4 PHP, Z	4C25PX	CMRCL	2800-38-4104	3
13	#4 LOCKWASHER, PLATED	#4SRLW	CMRCL	2800-42-4000	1
6	SPACER, LOCKING PC SUPPORT, NYLON	RLCBSR-4-01	RICH	2800-60-0001	5
9	SCREW MACH. 100 DEG, FLAT HD SS NYLOK PATCH	6-32X3/16 100D SS FH L	CMRCL	2800-61-6103	4
10	GROMET STRIP, GEN PURPOSE, POLYETHYLENE	GROMSTRIP GSPC-2	ICO	3000-00-0155	1.2
11	INSULATOR (TO-220)	60-11-8302-1674	CHOMR	3100-00-0010	1

WAVETEK
PARTS LIST
TITLE
ASSY, CHASSIS
ASSEMBLY NO. 1101-00-3079
REV A
PAGE 1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/x	.xxx	.xx	∠
± 1/64	± .005	± .01	± 1°

MATERIAL:
FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

	DATE
DRAWN	
CHKD	
ENG APPR.	
MFG APPR.	
ISSUED	

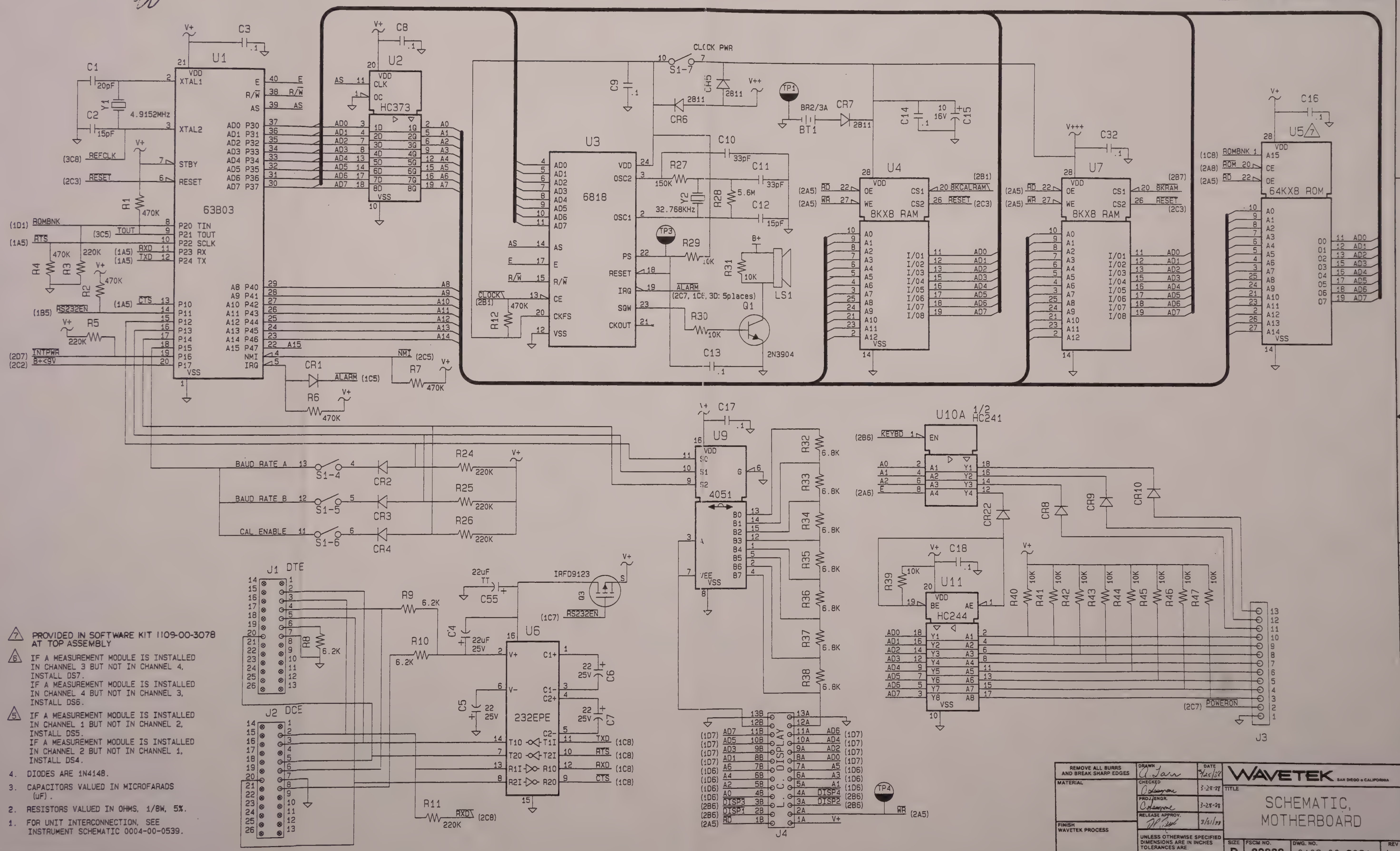
WAVETEK
Wavetek Inc.

TITLE
PARTS LIST
ASSY, CHASSIS

SIZE D
MODEL NO. 52A
DRAWING NO 1101-00-3079
REV A
SCALE:
CODE IDENT 23338
SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECO	BY	DATE	APP
A	FOR RELEASE PER ERO #9584	MAS	3-28-88	CJ



U1 63B03
U2 HC373
U3 6818
U4 8KX8 RAM
U7 8KX8 RAM
U5 64KX8 ROM
U6 232EPE
U9 4051
U10A 1/2 HC241
U11 HC244
Y1 4.9152MHz
Y2 32.768KHz
Q1 2N3904
Q3 IRFD9123
LS1
BT1 BR2/3A
S1-7 CLOCK PWR
S1-4 BAUD RATE A
S1-5 BAUD RATE B
S1-6 CAL ENABLE
J1 DTE
J2 DCE
J3
J4 L.C. DISPLAY
TP1
TP3
TP4

△7 PROVIDED IN SOFTWARE KIT 1109-00-3078 AT TOP ASSEMBLY

△6 IF A MEASUREMENT MODULE IS INSTALLED IN CHANNEL 3 BUT NOT IN CHANNEL 4, INSTALL DS7.
IF A MEASUREMENT MODULE IS INSTALLED IN CHANNEL 4 BUT NOT IN CHANNEL 3, INSTALL DS6.

△5 IF A MEASUREMENT MODULE IS INSTALLED IN CHANNEL 1 BUT NOT IN CHANNEL 2, INSTALL DS5.
IF A MEASUREMENT MODULE IS INSTALLED IN CHANNEL 2 BUT NOT IN CHANNEL 1, INSTALL DS4.

4. DIODES ARE 1N4148.
3. CAPACITORS VALUED IN MICROFARADS (uF).
2. RESISTORS VALUED IN OHMS, 1/8W, 5%.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0539.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

DRAWN A. Tarr — DATE 3/25/88
CHECKED — 3-28-88
PROJ. ENGR. — 3-28-88
RELEASE APPROV. — 3/31/88

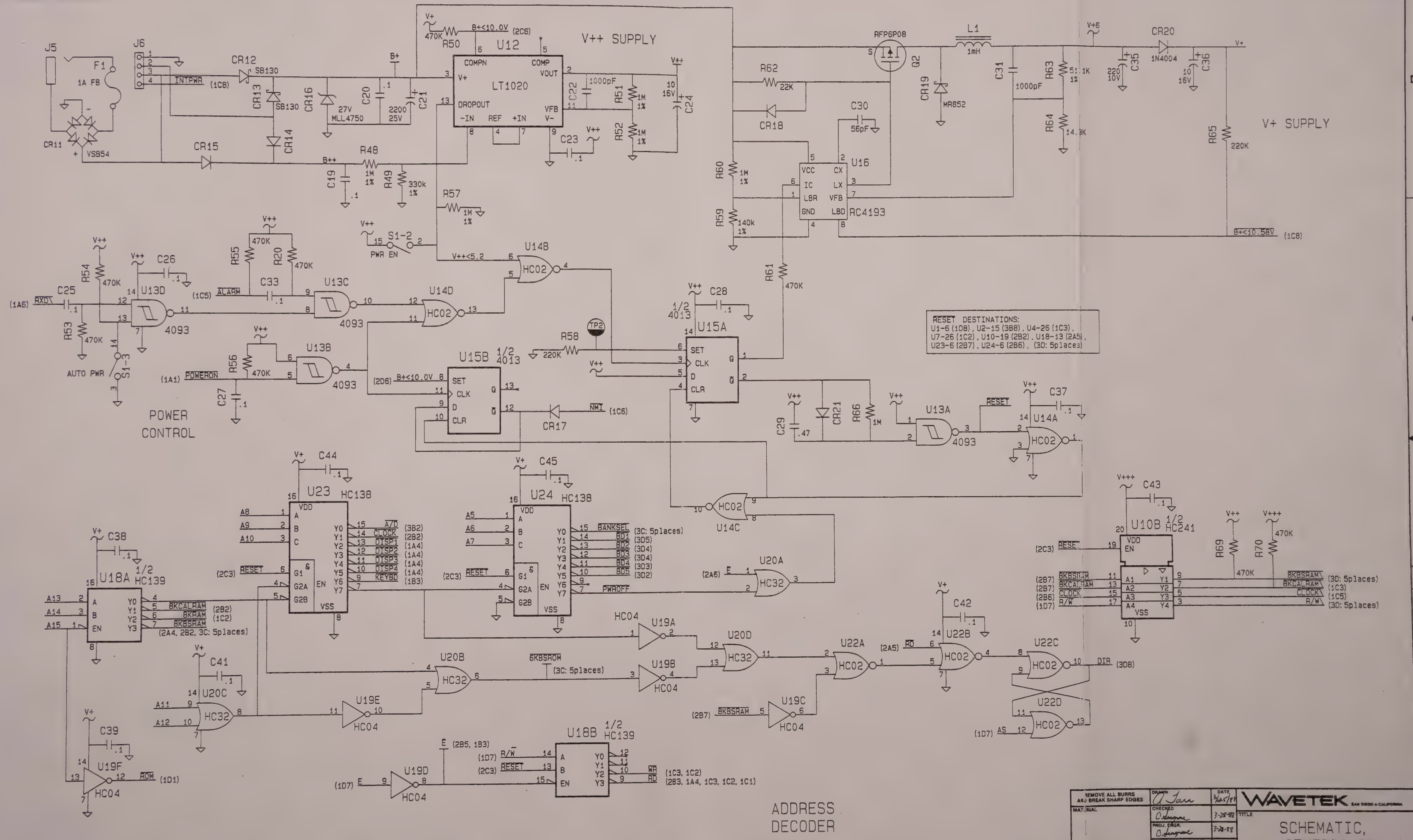
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC, MOTHERBOARD

SIZE D
FSCM NO. 23338
DWG. NO. 0103-00-3081
REV A
SCALE NONE
MODEL 52A
SHEET 1 OF 3

0103-00-3081 A


V++ SUPPLY
V+ SUPPLY
POWER CONTROL
ADDRESS DECODER
J5
F1 1A FB
CR11 VSB54
J6
INTPWR (1C8)
CR12 SB130
CR13 SB130
CR14
CR15
CR16 27V MLL4750
C20 .1
C21 2200 25V
U12 LT1020
R50 470K
B+<10.0V (2C6)
C22 1000pF
R51 1M 1%
R52 1M 1%
C23 .1
C24 10 16V
R48 1M 1%
R49 330K 1%
C19 .1
R57 1M 1%
S1-2 PWR EN
V++<5.2
L1 1mH
RFP6P08 Q2
CR19 MR852
C31 1000pF
R63 51.1K 1%
R64 14.3K
C35 220 10V
CR20 1N4004
C36 10 16V
R65 220K
R62 22K
CR18
C30 56pF
U16 RC4193
R60 1M 1%
R59 140k 1%
R61 470K
B+<10.58V (1C8)
U14B HC02
R55 470K
R20 470K
U13C 4093
U14D HC02
C33 .1
ALARM (1C5)
R54 470K
C26 .1
C25 .1
RXD (1A6)
U13D 4093
R53 470K
S1-3 AUTO PWR
U13B 4093
R56 470K
POWERON (1A1)
C27 .1
U15B 1/2 4013
B+<10.0V (2D6)
CR17
NMI (1C6)
R58 220K
TP2
C28 .1
U15A 1/2 4013
C29 .47
CR21
R66 1M
U13A 4093
U14A HC02
C37 .1
RESET
U14C HC02
C44 .1
U23 HC138
A8 A9 A10
A/D (3B2)
CLOCK (2B2)
DISP1 (1A4)
DISP2 (1A4)
DISP3 (1A4)
DISP4 (1A4)
KEYBD (1B3)
C45 .1
U24 HC138
A5 A6 A7
BANKSEL (3C: 5places)
BD1 (3D5)
BD2 (3D4)
BD3 (3D4)
BD4 (3D3)
BD5 (3D2)
PWROFF
U20A HC32
E (2A6)
C38 .1
U18A 1/2 HC139
A13 A14 A15
BKCALRAM (2B2)
BKRAM (1C2)
BKBSRAM (2A4, 2B2, 3C: 5places)
RESET (2C3)
C41 .1
U20C HC32
A11 A12
U20B HC32
BKBSROM (3C: 5places)
U19E HC04
U19A HC04
U19B HC04
U20D HC32
U22A HC02
RD (2A5)
U22B HC02
C42 .1
U22C HC02
DIR (3D8)
U22D HC02
AS (1D7)
U19C HC04
BKBSRAM (2B7)
C39 .1
U19F HC04
ROM (1D1)
U19D HC04
E (2B5, 1B3)
E (1D7)
R/W (1D7)
U18B 1/2 HC139
WR RD (1C3, 1C2) (2B3, 1A4, 1C3, 1C2, 1C1)
C43 .1
U10B 1/2 HC241
R69 470K
R70 470K
BKBSRAM (3D: 5places)
BKCALRAM (1C3)
CLOCK (1C5)
R/W (3D: 5places)
V+ V++ V+++ V+6 B+ B++

RESET DESTINATIONS:
U1-6 (1D8), U2-15 (3B8), U4-26 (1C3),
U7-26 (1C2), U10-19 (2B2), U18-13 (2A5),
U23-6 (2B7), U24-6 (2B6), (3D: 5places)

REV	ECO	BY	DATE	APP

NOTE: UNLESS OTHERWISE SPECIFIED

0103-00-3081 A

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN O. Tarr 3/25/88
CHECKED C. Seagrave 3-28-88
PROJ. ENGR. C. Seagrave 3-28-88
RELEASE APPROV. 3/31/88

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

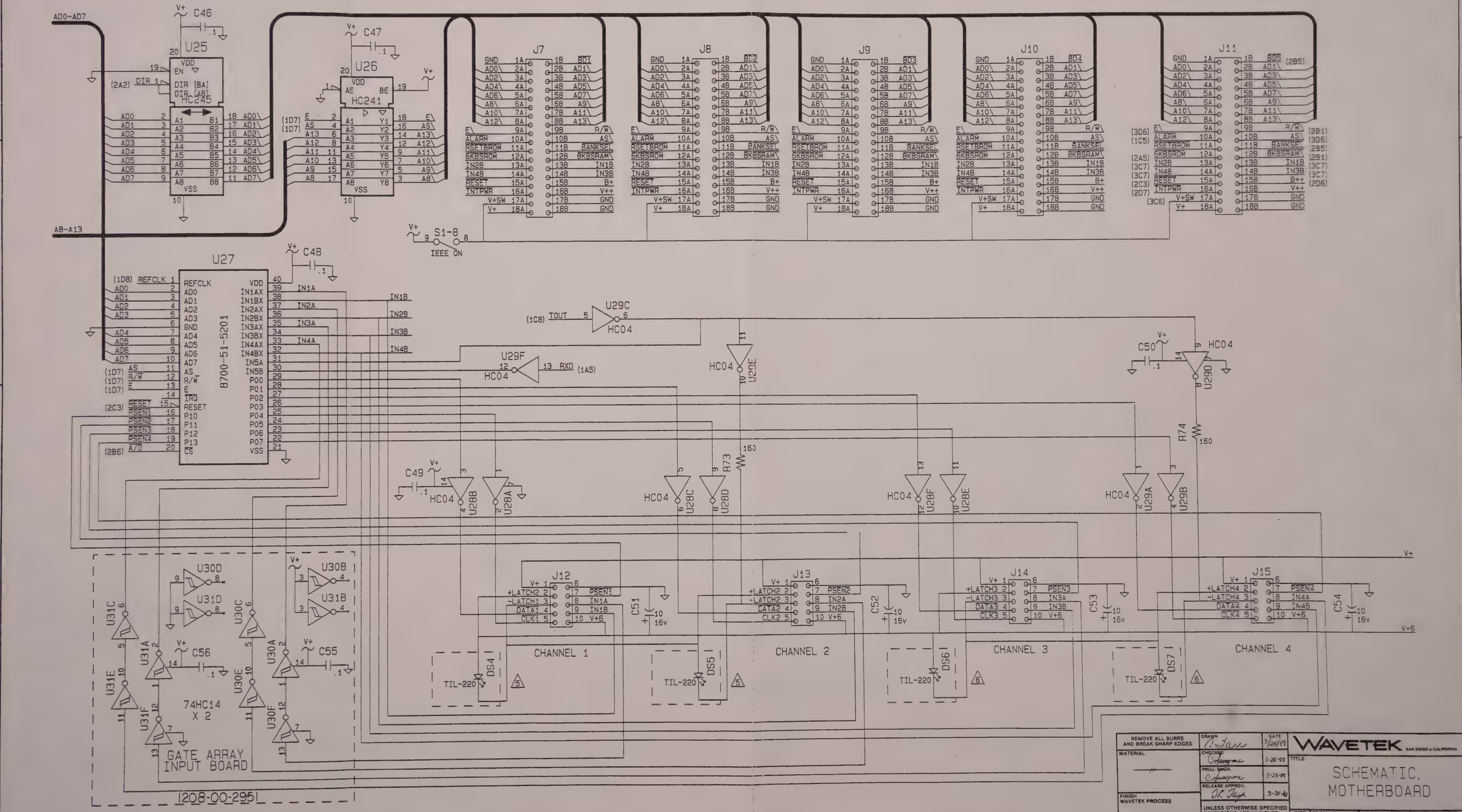
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
MOTHERBOARD

SIZE D | FSCM NO. 23338 | DWG. NO. 0103-00-3081 | REV A

SCALE NONE | MODEL 52A | SHEET 2 OF 3

REV	ECO	BY	DATE	APP


AD0-AD7
A8-A13
U25
HC245
C46
U26
HC241
C47
U27
8700-51-5201
C48
J7
J8
J9
J10
J11
S1-8
IEEE ON
U29C
HC04
U29F
U29E
U29D
C50
R74
160
R73
160
C49
U28B
U28A
U28C
U28D
U28F
U28E
U29A
U29B
J12
J13
J14
J15
C51
C52
C53
C54
DS4
DS5
DS6
DS7
TIL-220
CHANNEL 1
CHANNEL 2
CHANNEL 3
CHANNEL 4
U30D
U31D
U30B
U31B
U31C
U31A
U31E
U31F
U30C
U30A
U30E
U30F
C56
C55
74HC14
X 2
GATE ARRAY
INPUT BOARD
1208-00-2951
V+
V+6

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL —//—

FINISH WAVETEK PROCESS —//—

DO NOT SCALE DRAWING

DRAWN T. Tarr DATE 3/25/88
CHECKED 3-28-88
PROJ. ENGR. 3-26-88
RELEASE APPROV. 3-31-88

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

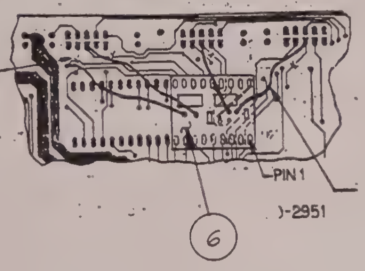
TITLE SCHEMATIC, MOTHERBOARD

SIZE D FSCM NO. 23338 DWG. NO. 0103-00-3081 REV A
SCALE NONE MODEL 52A SHEET 3 OF 3

0103-00-3081 A

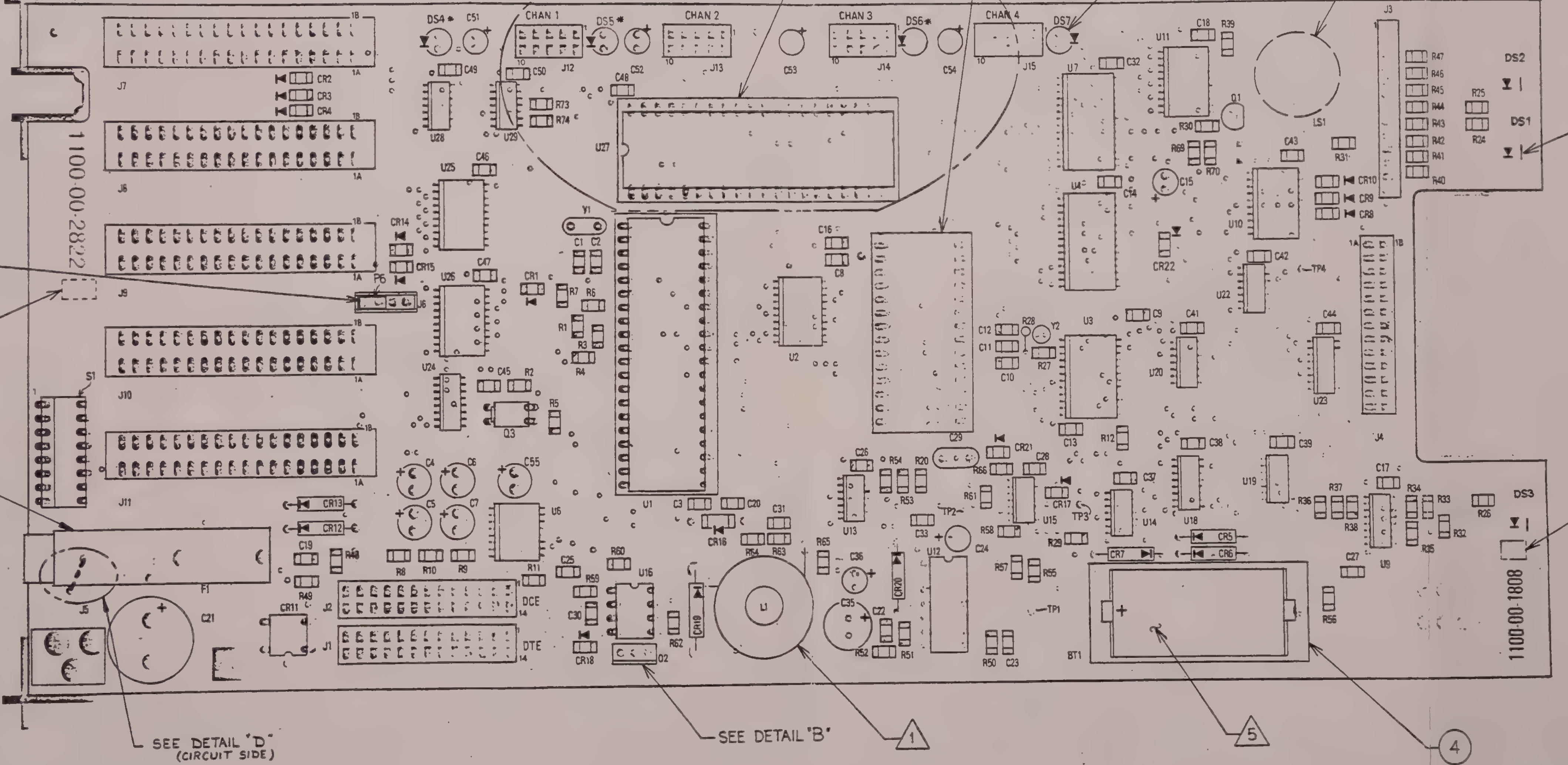
A	RELEASE PER ERO NO. 9584	MAG	2-22-88	

DETAIL "E"
CIRCUIT SIDE

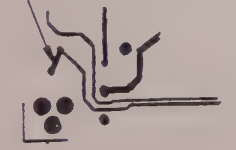


CUT TRACES 4 PLACES "X" ON CIRCUIT SIDE. ORIENT 1208-00-2951 ASSY OVER SOLDER PADS OF U27. AS SHOWN AND SOLDER 1208-00-2951 ASSY TO MOTHER BOARD AT PINS 1 THRU 8 & 33 THRU 40. CAUTION: CHECK THAT PINS 9 & 32 OF U27 ARE SOLDERED TO MOTHER BOARD BEFORE INSTALLING 1208-00-2951

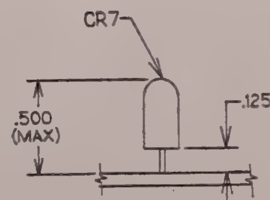
INSTALL INSULATE WIRE JUMPER (30 GA) 4 PLACES AS SHOWN AND SOLDER IN PLACE.


SEE DETAIL "E"
5 (2)
3
SEE DETAIL "A"
6
1
SEE DETAIL "C"
7
8
2
MARK ASSEMBLY REVISION LETTER IN AREA SHOWN
SEE DETAIL "D" (CIRCUIT SIDE)
SEE DETAIL "B"
1
5
4
1100-00-2822
1100-00-1808
CHAN 1
CHAN 2
CHAN 3
CHAN 4
DS1
DS2
DS3
DS4*
DS5*
DS6*
DS7
J1
J2
J3
J4
J5
J6
J7
J9
J10
J11
J12
J13
J14
J15
P6
S1
F1
LS1
BT1
L1
Y1
Y2
Q1
Q2
Q3
U1
U2
U3
U4
U5
U7
U9
U10
U11
U12
U13
U14
U15
U16
U18
U19
U20
U22
U23
U24
U25
U26
U27
U28
U29
DCE
DTE
TP1
TP2
TP3
TP4

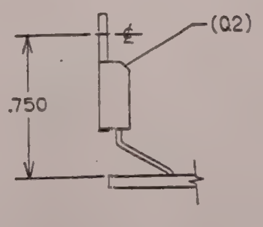
SOLDER INSULATED WIRE JUMPER (30 GA) TO PADS ON CIRCUIT SIDE



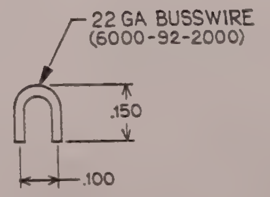
DETAIL "D"
CIRCUIT SIDE


CR7
.500 (MAX)
.125

DETAIL "A"



DETAIL "B"


22 GA BUSSWIRE (6000-92-2000)
.150
.100

DETAIL "C"
(3 PLACES)

8. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.

7. INSTALL P6 ON J6 PINS 1 & 2. REMOVE WHEN USING BATTERY OPTION 50-10 OR 50-11.

6. INSTALL LS1 ON CIRCUIT SIDE OF BOARD.

5. INSTALL BATTERY (BT1) USING A THIN PIECE OF MYLAR (OR EQUIV.) TO INSULATE "+" END OF BATTERY FROM IT'S CONTACT ONLY AFTER ALL SOLDER OPERATIONS ARE COMPLETED.

4. * = TRIM. INSTALLATION TO BE DETERMINED AT UNIT TEST.

3. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

2. SEE 0103-00-3081 FOR SCHEMATIC.

1. APPLY RTV (WAVETEK #1600-03-0004) PERMANENTLY BONDING L1 TO SURFACE OF CIRCUIT BOARD.

NOTES:

SEE SEPARATE PARTS LIST 1100-00-3081

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. GROVES	DATE 2-22-88	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Coleman	3-2-88	TITLE PCA, MOTHER BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 52A · DWG NO 1100-00-3081 · REV A
	SCALE 2/1		CODE IDENT 23338 · SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3004

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PCA MOTHER BOARD	0103-00-3081	WVTK	0103-00-3081	1
6	ASSY, GATE ARRAY PIGGYBACK	1208-00-2951	WVTK	1208-00-2951	1
C29	CAP, CER, MON, .47UF, 20%, 50V, 25U	CRC230Z5U474M050	CORNG	1500-04-7406	1
C15 C24 C36 C51 C52 C53 C54	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	7
C35	CAP, ELECT, 220MF/10V	ECEA1AU221	PANAS	1500-32-2001	1
C4 C5 C55 C6 C7	CAP, ELECT, 22MF, 25V, RADIAL	SRA25VB22MC	UNCON	1500-32-2002	5
C21	CAP, ELECT, 2200MF, 25V RADIAL LEAD	ECEA1EV222S	PANAS	1500-32-2202	1
C22 C31	CAP, SMD CER 5% 50V 1000PF	C1206C102J2GAC	KEMET	1500-81-0201	2
C13 C14 C16 C17 C18 C19 C20 C23 C25 C26 C27 C28 C3 C32 C33 C37 C38 C39 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C8 C9	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	30
C12 C2	CAP, SMD CER 5% 50V 15PF	C1206C150J2GAC	KEMET	1500-81-5001	2
C1	CAP, SMD CER 2% 50V	C1206C200G5GAC	KEMET	1500-82-0001	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, MOTHER BD-52A	1100-00-3081 PAGE 1	B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	20PF				
C10 C11	CAP, SMD CER 5% 50V 33PF	C1206C330J2GAC	KEMET	1500-83-3001	2
C30	CAP, SMD CER 5% 50V 56PF	C1206C560J2GAC	KEMET	1500-85-6001	1
1	DRILL DRWG, PCA, MOTHER BOARD	1700-00-1808	WVTK	1700-00-1808	1
L1	CHOKE, TORROIDAL, 1MH	4294	CASYS	1800-00-0025	1
J6	CONN, HEADER 4 PIN	102202-1	AMP	2100-02-0131	1
J1 J2 J4	CONN, HEADER 26 PIN/2 ROW, .1 CTR, 15 GLD	929836-01-13	A/P	2100-02-0156	3
J10 J11 J7 J8 J9	CONN, EDGE 36 PIN	ETC18DRXN	SULL	2100-02-0191	5
J5	CONN POWER JACK	16PJ032	MOUSR	2100-02-0192	1
J12 J13 J14 J15	CONN, HEADER, DOUBLE 5 PIN ROWS, 0.1X0.1	929836-01-05	APTRN	2100-02-0212	4
P6	JUMPER, FEMALE, 2 POSITION, 0.1 SPACE	929950-00	APTRN	2100-02-0213	1
J3	CONN, HEADER, 13 PIN, 0.1 SPACE	929834-01-13	APTRN	2100-02-0218	1
5	SKT, IC, 40PIN	DILB40P-108T	BURND	2100-03-0030	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, MOTHER BD-52A	1100-00-3081 PAGE 2	B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
3	SOCKET, IC, 28 PIN	DILB28P-108T	BURND	2100-03-0081	1
TP1 TP2 TP3 TP4	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	4
Y2	CRYSTAL 32.768KHZ	KF380	KYCRA	2300-99-0020	1
Y1	CRYSTAL 4.915MHZ	C1700	MIDRO	2300-99-0021	1
F1	FUSE, 1A, 250V	312001	LITFU	2400-05-0007	1
2	FUSE HOLDER, PCB MOUNT	345101	LITFU	2400-05-0043	1
4	BATTERY HOLDER	BH 2/3A	MPD	3000-00-0137	1
LS1	PIEZO	PKM24-4A0	MURAT	3000-00-0141	1
BT1	BATTERY, 3V LITHIUM	BR-2/3A	PANAS	4000-02-0008	1
R29 R30 R31 R39 R40 R41 R42 R43 R44 R45 R46 R47	RES, SMD GP 1/8 LONG 200PPM 5% 10K OHM	MCR18EZH103JW5%	ROHM	4703-20-1035	12
R27	RES, SMD GP 1/8 LONG 200PPM 5% 150K OHM	MCR18EZH154JW5%	ROHM	4703-20-1545	1
R73 R74	RES, SMD GP 1/8 LONG 200PPM 5% 160 OHM	MCR18EZH161JW5%	ROHM	4703-20-1615	2
R62	RES, SMD GP 1/8 LONG 200PPM 5% 22K OHM	MCR18EZH223JW5%	ROHM	4703-20-2235	1
R11 R24 R25 R26 R3 R5 R58 R65	RES, SMD GP 1/8 LONG 200PPM 5% 220K OHM	9C12063A2203JLR	MEPCO	4703-20-2245	8

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, MOTHER BD-52A	1100-00-3081 PAGE 3	B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R1 R12 R2 R20 R4 R50 R53 R54 R55 R56 R6 R61 R69 R7 R70	RES, SMD GP 1/8 LONG 200PPM 5% 470K OHM	MCR18EZH474JW5%	ROHM	4703-20-4745	15
R10 R8 R9	RES, SMD GP 1/8 LONG 200PPM 5% 6.2K OHM	MCR18EZH622JW5%	ROHM	4703-20-6225	3
R32 R33 R34 R35 R36 R37 R38	RES, SMD GP 1/8 LONG 200PPM 5% 6.8K OHM	MCR18EZH682JW5%	ROHM	4703-20-6825	7
R59	RES, 1/8 LONG, 100PPM, 1%, 100K, 1/8W	9C12063A1003FKR	MEPCO	4703-21-0031	1
R48 R51 R52 R57 R66	RES SMD 1/8 LONG 100PPM 1% 1M OHM	MCR18FXTA1004F	ROHM	4703-21-0041	5
R64	RES, SMD 1/8 LONG 100PPM 1% 14.3K OHM	9C12063A1432FKR	MEPCO	4703-21-4321	1
R49	RES, SMD 1/8 LONG 100PPM 1% 316K OHM	MCR18FXTA3163F	ROHM	4703-23-1631	1
R63	RES, SMD 1/8 LONG 100PPM 1% 51.1K OHM	9C12063A5112FKR	MEPCO	4703-25-1121	1
R60	RES, 1/8 LONG, 100PPM, 1%, 750K, 1/8W	9C12063A7503FKR	MEPCO	4703-27-5031	1
[illegible]	RES, CC, 1/8W 5% 5.6M	BB5655	AB	4704-05-5604	1
CR16	DIODE ZENER, 27V,	MLL4750	MOT	4801-02-0002	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, MOTHER BD-52A	1100-00-3081 PAGE 4	B

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE				DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.
x/x ± 1/64	.xxx ± .005	.xx ± .01	∠ ± 1°	DRAWN / DATE	TITLE PARTS LIST MOTHER BD-52A
MATERIAL:				CHKD	
				ENG APPR.	
FINISH:				MFG APPR.	SIZE D · MODEL NO 52A · DRAWING NO 1100-00-3081 · REV B
				ISSUED	SCALE: · CODE IDENT 23338 · SHEET 1 OF 2

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	10%, 1W, LEAD LESS				
CR20	RECTIFIER, GEN PURP, 400V, 1A	1N4004	MOT	4806-01-4004	1
CR11	DIODE, RECTIFIER, DUAL IN-LINE	VS854	VARO	4806-02-0054	1
CR12 CR13	DIODE, STTKY	SB130	GI	4806-02-0130	2
CR19	DIODE, 3A, 200V, FR	MR852	MOT	4806-02-0852	1
CR1 CR10 CR14 CR15 CR17 CR18 CR2 CR21 CR22 CR3 CR4 CR8 CR9	DIODE, LEADLESS EQUIVALENT IN4148, 500MW, SMD	RLS4148	ROHM	4807-01-4148	13
CR5 CR6 CR7	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	3
DS7	LED	TIL-220	TI	4899-00-0006	1
Q1	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	1
Q2	TRANS, POWER FET, P-CHAN ENHANCMNT MODE	RFP6P08	RCA	4902-00-6081	1
Q3	TRANSISTOR	IRFD9123	IR	4902-09-1230	1
S1	SWITCH, DIP PIANO LEVER	76PSB08	GRAHL	5199-00-0005	1
U12	REGULATOR &	LT1020	LINTE	7000-10-2000	1

WAVETEK PARTS LIST	TITLE PCA, MOTHER BD-52A	ASSEMBLY NO. 1100-00-3081 PAGE 5	REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	COMPARATOR, MICRO PWR				
U16	REGULATOR SWITCHING, VARIABLE	RC4193NB	RAYTH	7000-41-9300	1
U4 U7	RAM, 8X8192, CMOS SMD	SRM2064M15	S-MOS	8000-20-6400	2
U15	FLIP-FLOP, DUAL D, CMOS, SMD	HEF4013BTD	SIG	8000-40-1341	1
U9	MUX/DEMUX 8-CHANNEL ANALOG CMOS SMD	HEF4051BTD	SIG	8000-40-5141	1
U13	GATE, NAND, S/TRIG, QUAD 2-INP, CMOS, SMD	HEF4093BTD	SIG	8000-40-9341	1
U1	MICRO PROCESSING UNIT, CMOS	HD63B03RP	HTACH	8000-63-0301	1
U14 U22	GATE, NOR QUAD 2 INPUT POS HCMOS SMD	74HC02D	SIG	8000-74-0241	2
U19 U28 U29	HEX INVERTER	74HC04D	SIG	8000-74-0442	3
U20	GATE, OR, QUAD 2-INPUT, HCMOS, SMD	74HC32D	SIG	8000-74-3241	1
U23 U24	DECODER/DEMUX, 1 OF 8, HCMOS, SMD	74HC138D	SIG	8007-41-3841	2
U18	DEMUX, DUAL 2-TO-4 DECODER, SMD	74HC139D	SIG	8007-41-3941	1

WAVETEK PARTS LIST	TITLE PCA, MOTHER BD-52A	ASSEMBLY NO. 1100-00-3081 PAGE 6	REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U10 U26	BUF/LN DRIVER, OCTAL, TRISTATE, HCMOS, SMD	74HC241D	SIG	8007-42-4140	2
U11	BUF/LN DRIVER, OCTAL, TRISTATE, HCMOS, SMD	N74HC244D	SIG	8007-42-4441	1
U25	TRANSCEIVER, OCTAL BUSS, TRISTATE, HCMOS, SMD	74HC245D	SIG	8007-42-4541	1
U2	D-TRANSPARENT LATCH, OCTAL, TRISTATE, HCMOS, SMD	74HC373D	SIG	8007-43-7341	1
U3	SO	HD146818FP	HTACH	8014-68-1800	1
U6	RECEIVER/TRANSMITTER, RS-232+5V, 16PIN, SMD	MAX232EWE	MAXIM	8100-00-0012	1
U27	LSI, CUSTOM GATE ARRAY, CMOS, 4 CHAN UNIV	8700-51-5201	WVTK	8700-51-5201	1

WAVETEK PARTS LIST	TITLE PCA, MOTHER BD-52A	ASSEMBLY NO. 1100-00-3081 PAGE 7	REV B

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/x	.xxx	.xx	∠
± 1/64	± .005	± .01	± 1°

MATERIAL:

FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

	DATE
DRAWN	
CHKD	
ENG APPR.	
MFG APPR.	
ISSUED	

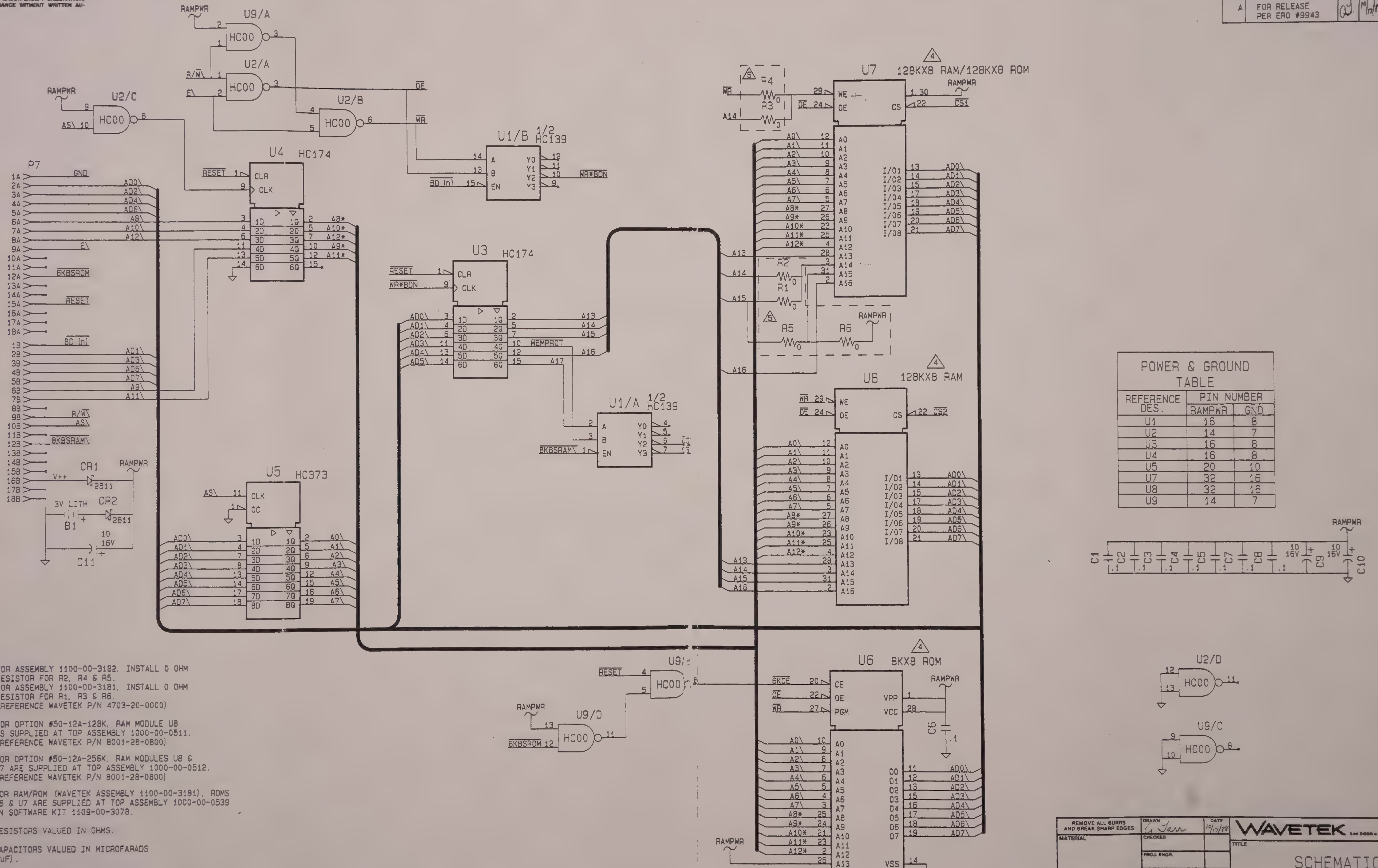
WAVETEK
Wavetek Inc.

TITLE
PARTS LIST
MOTHER BD-52A

SIZE	MODEL NO	DRAWING NO	REV
D	52A	1100-00-3081	B

SCALE: CODE IDENT 23338 SHEET 2 OF 2

REV	ECO	BY	DATE	APP
A	FOR RELEASE PER ERO #9943	QY.	10/17/88	


U9/A HC00
U2/A HC00
U2/B HC00
U2/C HC00
RAMPWR
R/W\
E\
AS\
OE
WR
U1/B 1/2 HC139
BD (n)
WR*BDN
U4 HC174
RESET
CLR
CLK
P7
GND
AD0\ AD1\ AD2\ AD3\ AD4\ AD5\ AD6\ AD7\
A8\ A9\ A10\ A11\ A12\
A8* A9* A10* A11* A12*
6KBSROM
8KBSRAM\
CR1 2811
CR2 2811
3V LITH B1
C11 10 15V
V++
U3 HC174
MEMPROT
A13 A14 A15 A16 A17
U1/A 1/2 HC139
U5 HC373
OC
U7 128KX8 RAM/128KX8 ROM
WE OE CS
CS1
R1 R2 R3 R4 R5 R6
U8 128KX8 RAM
CS2
I/01 I/02 I/03 I/04 I/05 I/06 I/07 I/08
U6 8KX8 ROM
6KCE
CE OE PGM VPP VCC VSS
C6 .1
U9/B HC00
U9/D HC00
U2/D HC00
U9/C HC00
C1 C2 C3 C4 C5 C7 C8 .1
C9 C10 10 16V

POWER & GROUND TABLE		
REFERENCE DES.	PIN NUMBER	
	RAMPWR	GND
U1	16	8
U2	14	7
U3	16	8
U4	16	8
U5	20	10
U7	32	16
U8	32	16
U9	14	7

5 FOR ASSEMBLY 1100-00-3182, INSTALL 0 OHM RESISTOR FOR R2, R4 & R5.
FOR ASSEMBLY 1100-00-3181, INSTALL 0 OHM RESISTOR FOR R1, R3 & R6.
(REFERENCE WAVETEK P/N 4703-20-0000)

4 FOR OPTION #50-12A-128K, RAM MODULE U8 IS SUPPLIED AT TOP ASSEMBLY 1000-00-0511.
(REFERENCE WAVETEK P/N 8001-28-0800)

FOR OPTION #50-12A-256K, RAM MODULES U8 & U7 ARE SUPPLIED AT TOP ASSEMBLY 1000-00-0512.
(REFERENCE WAVETEK P/N 8001-28-0800)

FOR RAM/ROM (WAVETEK ASSEMBLY 1100-00-3181), ROMS U6 & U7 ARE SUPPLIED AT TOP ASSEMBLY 1000-00-0539 IN SOFTWARE KIT 1109-00-3078.

3. RESISTORS VALUED IN OHMS.

2. CAPACITORS VALUED IN MICROFARADS (uF).

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440 (MODEL 51/52) OR 0004-00-0539 (MODEL 52A).

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN G. Tarr DATE 10/17/88
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

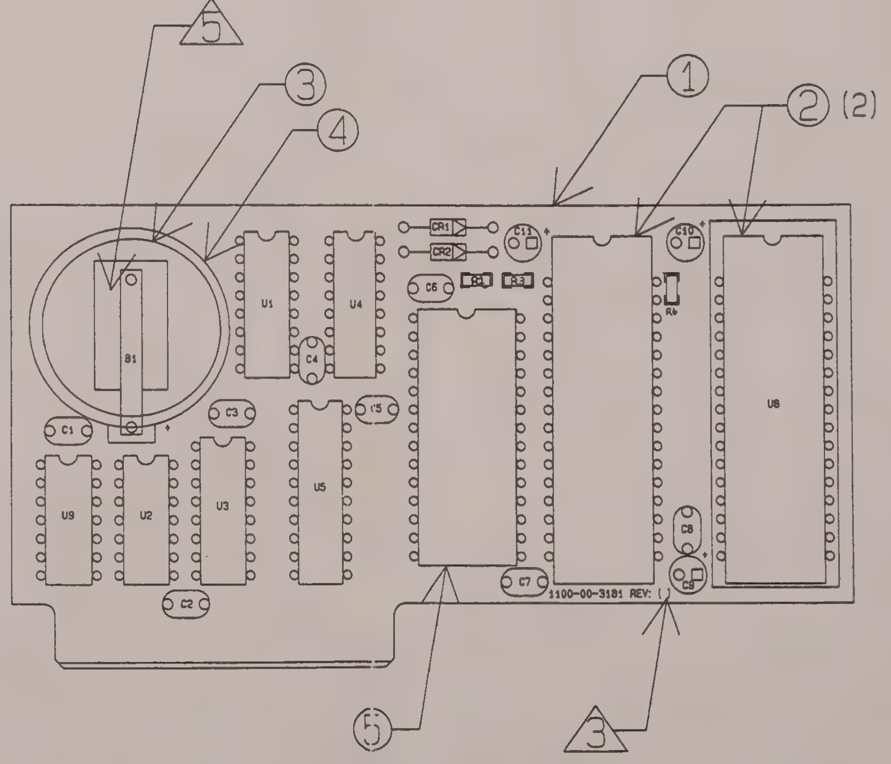
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
RAM/ROM BOARD

SIZE D FSCM NO. 23338 DWG. NO. 0103-00-3181 REV A
SCALE NONE MODEL 52A SHEET 1 OF 1

0103-00-3181 A

REV	ECO	BY	DATE	APP
A	FOR RELEASE PER ERO #9943	QJ	10/17/88	



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, RAM/ROM BD 52A	0103-00-3181	WVTK	0103-00-3181	1
C1 C2 C3 C4 C5 C6 C7 C8	CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2	SR215E104ZAA	AVX	1500-01-0420	8
C10 C11 C9	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	3
NONE	PCB, RAM/ROM BD 52A	1700-00-3181	WVTK	1700-00-3181	1
5	SKT, IC, 28PIN	DILB28P-108T	BURND	2100-03-0055	1
2	SOCKET, DUAL WIPE, 32 PIN, .7 WIDE	ICO-326-S8-T	ROBNU	2100-03-0093	2
NONE	INSULATOR, IC PAD	818-030	BIVAR	2800-11-0035	1
3	BATTERY HOLDER, LITH COIN CELL	BH1000	MEMPD	3000-00-0175	1
4	BATTERY, 3V LITH, COIN CELL, 200 MAHR	DL2430	DURCL	4000-02-0012	1
R1 R3	ZERO OHM JUMPER SMD 1/8 BODY LENGHT 2 AMP	MCR18-JPW	ROHM	4703-20-0000	2
CR1 CR2	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	2
U2 U9	GATE, NAND, QUAD 2 INPUT, 14 PIN DIP	MC74HC00N	MOT	8000-74-0011	2

WAVETEK PARTS LIST	TITLE PCA, RAM/ROM BD 52A	ASSEMBLY NO. 1100-00-3181 PAGE 1	REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U8	RAM-128K X 8 CMOS STATIC 150ns	MH12808SNA-15	MITSU	8001-28-0800	1
U1	DECODER/DEMUX, DUAL 1 OF 4, 16 PIN DIP	MC74HC139N	MOT	8007-41-3911	1
U3 U4	FLIP-FLOP, HEX D, W/RESET	MC74HC174N	MOT	8007-41-7440	2
U5	LATCH, OCTAL TRANSPAR W/3 STATE, CMOS	SN74HC373N	TI	8007-43-7340	1

WAVETEK PARTS LIST	TITLE PCA, RAM/ROM BD 52A	ASSEMBLY NO. 1100-00-3181 PAGE 2	REV A

5. INSTALL BATTERY (B1) USING A THIN PIECE OF MYLAR (OR EQUIV.) TO INSULATE "+" END OF BATTERY FROM IT'S CONTACT (THE CLIP ON ITEM 4) ONLY AFTER ALL SOLDER OPERATIONS ARE COMPLETED.
4. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
3. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0539.
1. SEE 0103-00-3181 FOR SCHEMATIC.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPERATE PARTS LIST PL 1100-00-3181

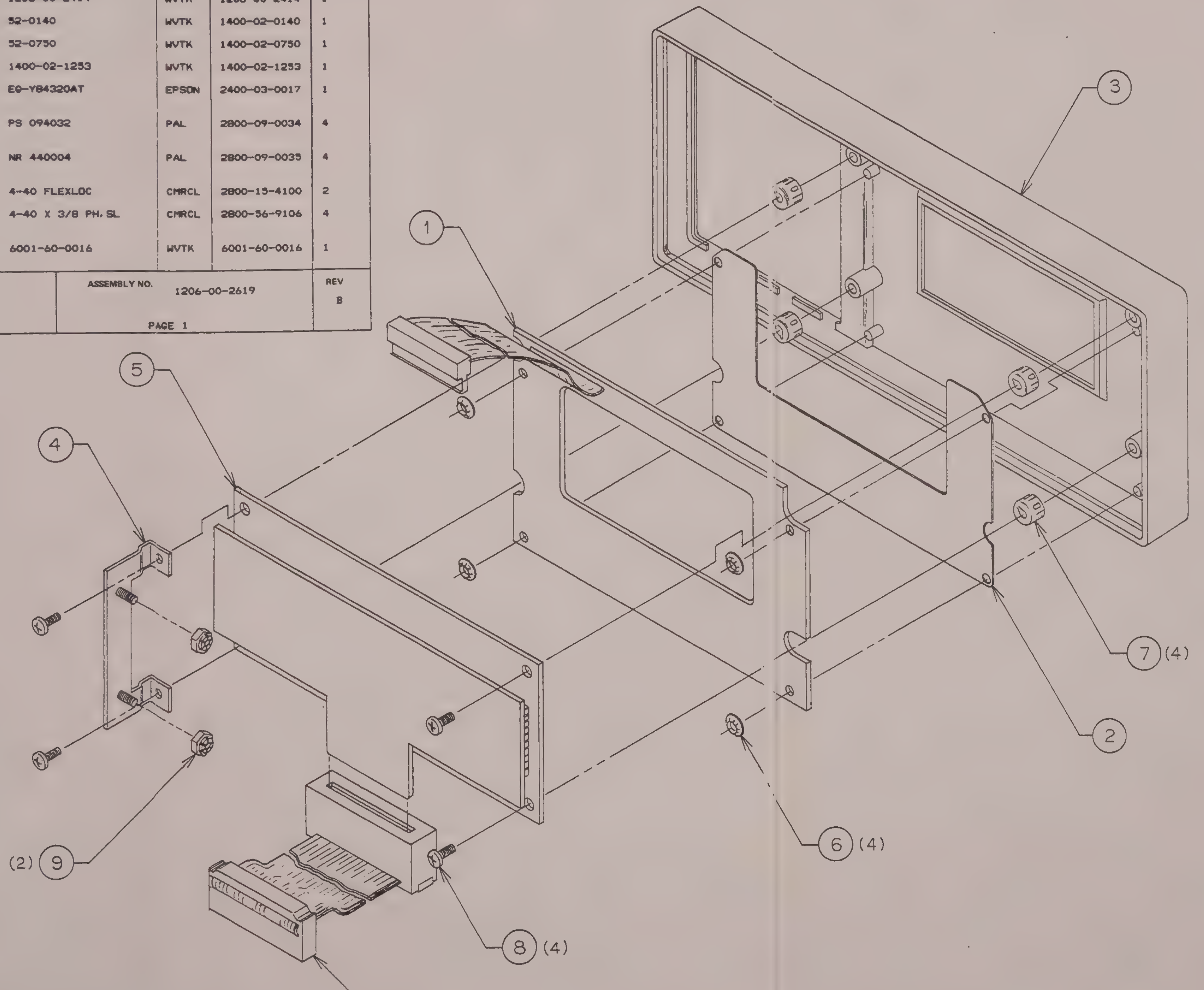
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Q. Tarr	DATE 10/17/88	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE PCA, RAM/ROM BOARD
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3181 · REV A
DO NOT SCALE DRAWING			SCALE · MODEL · Sheet OF

1100-00-3181 A

REV	ECN	BY	DATE	APP
A	FOR RELEASE	AT	3/5/86	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCA, KEYBOARD-52	1208-00-2414	WVTK	1208-00-2414	1
2	KEYPAD	52-0140	WVTK	1400-02-0140	1
3	PANEL, FRONT	52-0750	WVTK	1400-02-0750	1
4	BRACKET, FRONT PANEL	1400-02-1253	WVTK	1400-02-1253	1
5	DISPLAY, DOT MATRIX, LCD, W/RAM 3X1.25	EG-Y84320AT	EPSON	2400-03-0017	1
6	NUT, PUSH, FASTENER, ROUND, 3/32 ID	PS 094032	PAL	2800-09-0034	4
7	ON-SERT FASTENER, 4-40	NR 440004	PAL	2800-09-0035	4
9	NUT, FLEXLOC, 4-40, Z	4-40 FLEXLOC	CMRCL	2800-15-4100	2
8	SCREW, 4-40X3/8 PHP, NYLOK PATCH, Z	4-40 X 3/8 PH, SL	CMRCL	2800-56-9106	4
W4	RIBBON CABLE 26 PIN 28AWG	6001-60-0016	WVTK	6001-60-0016	1

WAVETEK PARTS LIST	TITLE ASSY, FRONT PANEL-52	ASSEMBLY NO. 1206-00-2619 PAGE 1	REV B



W4
ATTACH W4 TO DISPLAY (ITEM 5)
BEFORE INSTALLING DISPLAY INTO
ASSEMBLY.

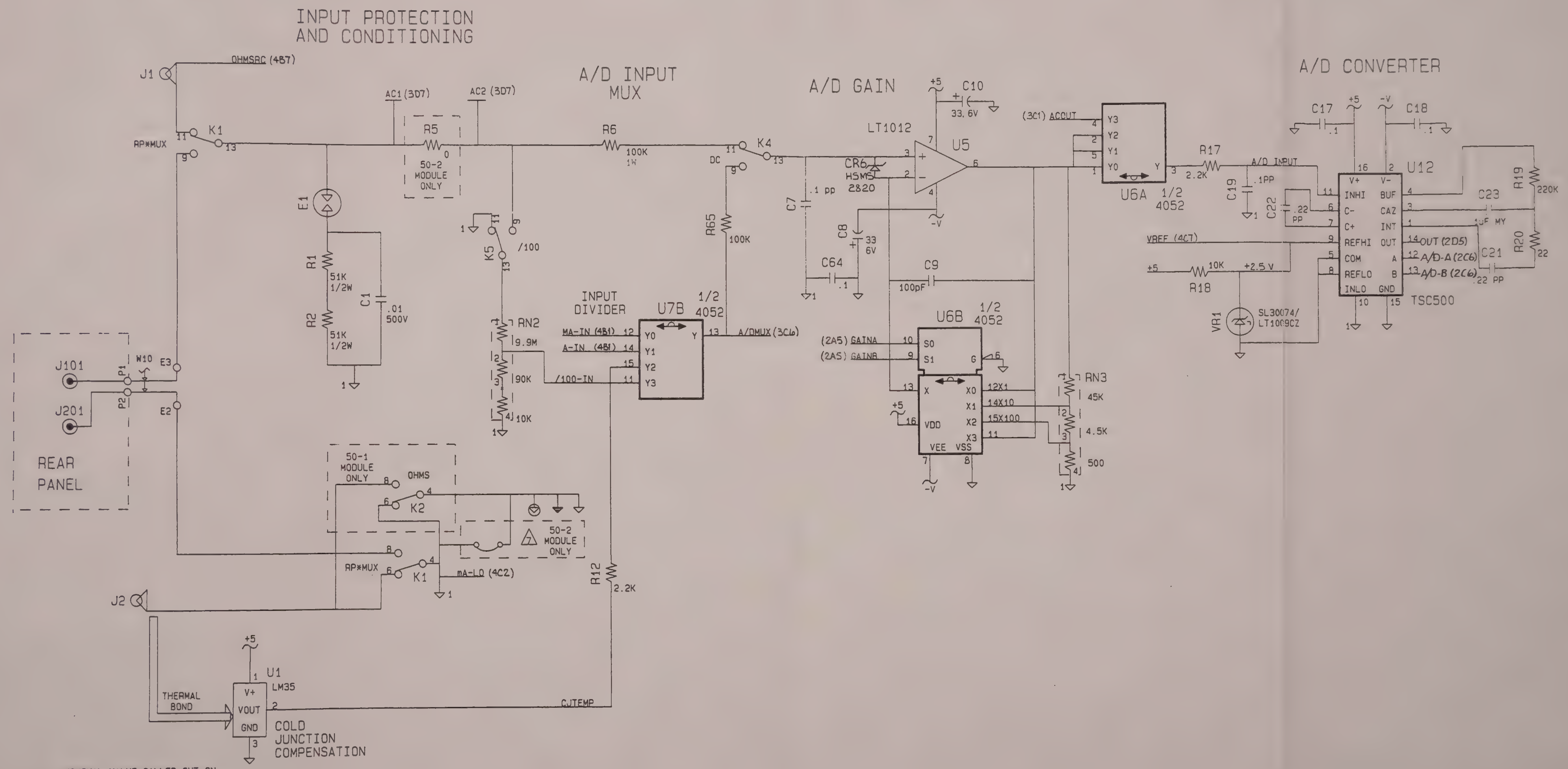
SEE SEPARATE PARTS LIST 1206-00-2619

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 9/9/85	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	PROJ ENGR	3/7/86	TITLE ASSEMBLY, FRONT PANEL
	RELEASE APPROV 3/10/86		
FINISH WAVETEK PROCESS —//—	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 52 / DWG NO 1206-00-2619 / REV A
	SCALE NONE		CODE IDENT 23338 / SHEET 1 OF 1

1206-00-2619 A

NOTE. UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
A	ECO # 9898	MS	10/27/88	


INPUT PROTECTION
AND CONDITIONING
A/D INPUT
MUX
A/D GAIN
A/D CONVERTER
J1
OHMSRC (4B7)
AC1 (3D7)
AC2 (3D7)
K1
RP*MUX
R5
50-2
MODULE
ONLY
R6
100K
1W
K4
DC
E1
R1
51K
1/2W
R2
51K
1/2W
C1
.01
500V
K5
/100
RN2
9.9M
90K
10K
R65
100K
INPUT
DIVIDER
U7B
1/2
4052
MA-IN (4B1)
A-IN (4B1)
/100-IN
Y0
Y1
Y2
Y3
Y
A/DMUX (3C6)
LT1012
U5
CR6
HSMS
2820
C7
.1 PP
C8
33
6V
C64
.1
C9
100pF
C10
33, 6V
+5
-V
(3C1) ACOUT
U6A
1/2
4052
R17
2.2K
A/D INPUT
U6B
1/2
4052
(2A5) GAINA
(2A5) GAINB
S0
S1
G
X
X0
X1
X2
X3
VDD
VEE
VSS
12X1
14X10
15X100
RN3
45K
4.5K
500
C17
.1
C18
.1
C19
.1PP
C22
.22
PP
U12
TSC500
V+
V-
INHI
BUF
C-
CAZ
C+
INT
REFHI
OUT
COM
A
REFLO
B
INLO
GND
VREF (4C7)
+5
10K
+2.5 V
R18
VR1
SL30074/
LT1009CZ
C23
.1UF MY
C21
.22 PP
R19
220K
R20
22
OUT (2D5)
A/D-A (2C6)
A/D-B (2C6)
J101
J201
W10
P1
P2
E3
E2
REAR
PANEL
50-1
MODULE
ONLY
OHMS
K2
50-2
MODULE
ONLY
RP*MUX
K1
mA-LO (4C2)
R12
2.2K
J2
THERMAL
BOND
U1
LM35
V+
VOUT
GND
CJTEMP
COLD
JUNCTION
COMPENSATION

8. * = NOMINAL VALUE CALLED OUT ON PARTS LIST.

△7 FOR 50-2 MODULE: INSTALL JUMPER BETWEEN PIN 4 & 6 OF K2.

△6 FOR 50-2 MODULE: INSTALL JUMPER BETWEEN PIN 2 & 3 OF VR3.

△5 (n) INDICATES CHANNEL NUMBER; E.G., IF J5 IS CONNECTED TO J13 THAN +LATCH (n) = +LATCH2 = +LATCH SIGNAL FOR CHANNEL 2 MODULE.

4. DIODES ARE RLS4148.

3. CAPACITORS VALUED IN MICROFARADS (uF).

2. RESISTORS VALUED IN OHMS, 1/8W, 5%.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440 FOR MODEL 51/52 OR 0004-00-0539 FOR MODEL 52A.

NOTE: UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27088

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN ANN TARR
DATE
PROJ ENGR C. SEAGRAVE
RELEASE APPROV D.R. TAYLOR
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
XX ±.030
DO NOT SCALE DWG
SCALE NONE

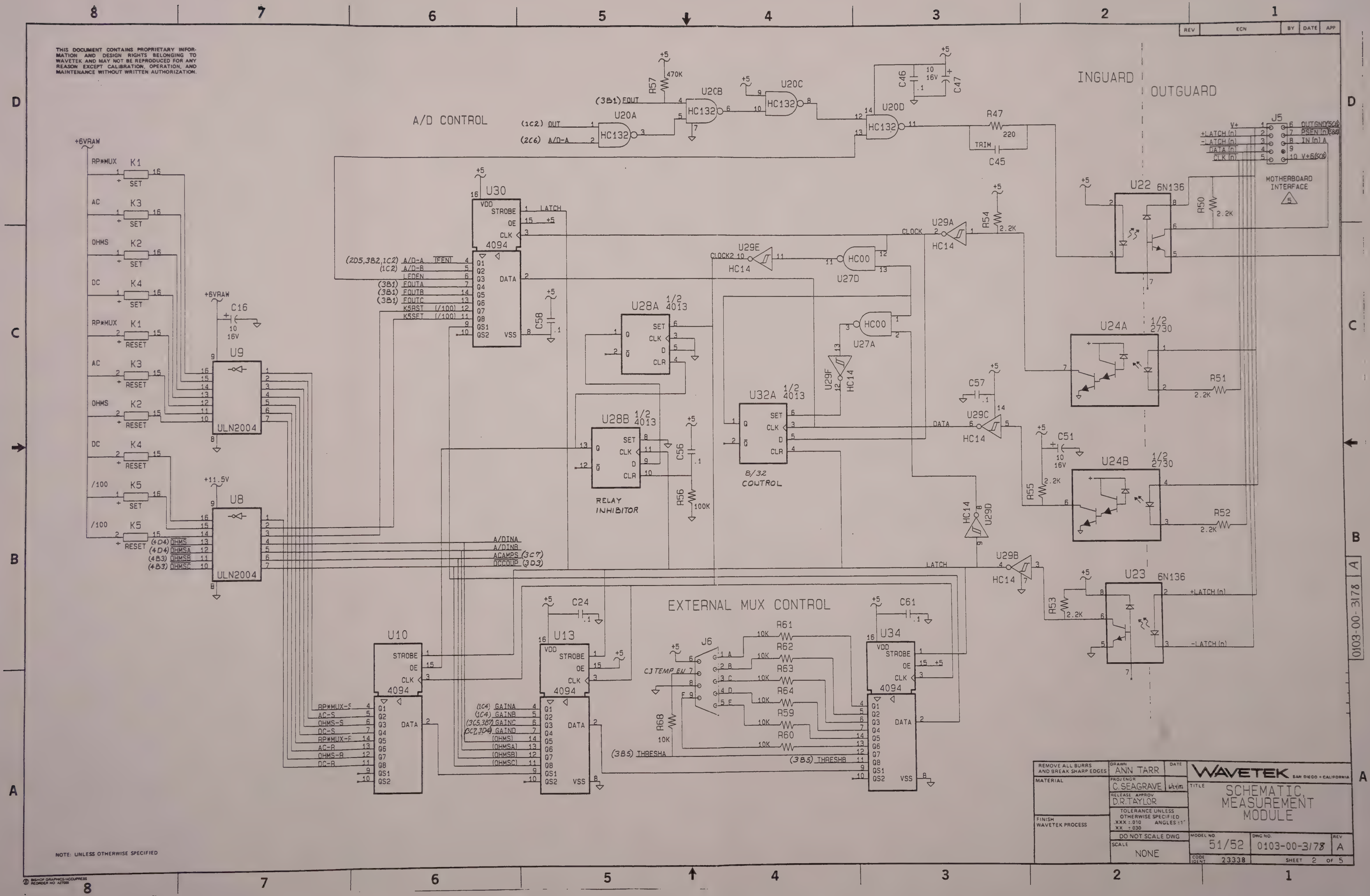
WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC, MEASUREMENT MODULE

MODEL NO. 51/52
DWG NO. 0103-00-3178
REV A
CODE IDENT 23338
SHEET 1 OF 5

0103-00-3178 A

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.


A/D CONTROL
INGUARD
OUTGUARD
EXTERNAL MUX CONTROL
RELAY INHIBITOR
B/32 CONTROL
MOTHERBOARD INTERFACE
U20A HC132
U20B HC132
U20C HC132
U20D HC132
U22 6N136
U23 6N136
U24A 1/2 2730
U24B 1/2 2730
U29A HC14
U29B HC14
U29C HC14
U29D HC14
U29E HC14
U29F HC14
U27A HC00
U27D HC00
U28A 1/2 4013
U28B 1/2 4013
U32A 1/2 4013
U30 4094
U10 4094
U13 4094
U34 4094
U8 ULN2004
U9 ULN2004
K1 K2 K3 K4 K5
J5
J6
+6VRAW
+11.5V
+5
CLOCK
DATA
LATCH
+LATCH (n)
-LATCH (n)
OUTGND(5C8)
PSEN (n)
IN (n) A
V+6(5C8)
CJ TEMP EN
(3B5) THRESHA
(3B5) THRESHB
A/DINA
A/DINB
ACAMPS (3C7)
DCCOUP (3D3)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN ANN TARR

PROJ ENGR C. SEAGRAVE

RELEASE APPROV D.R.TAYLOR

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
MEASUREMENT
MODULE

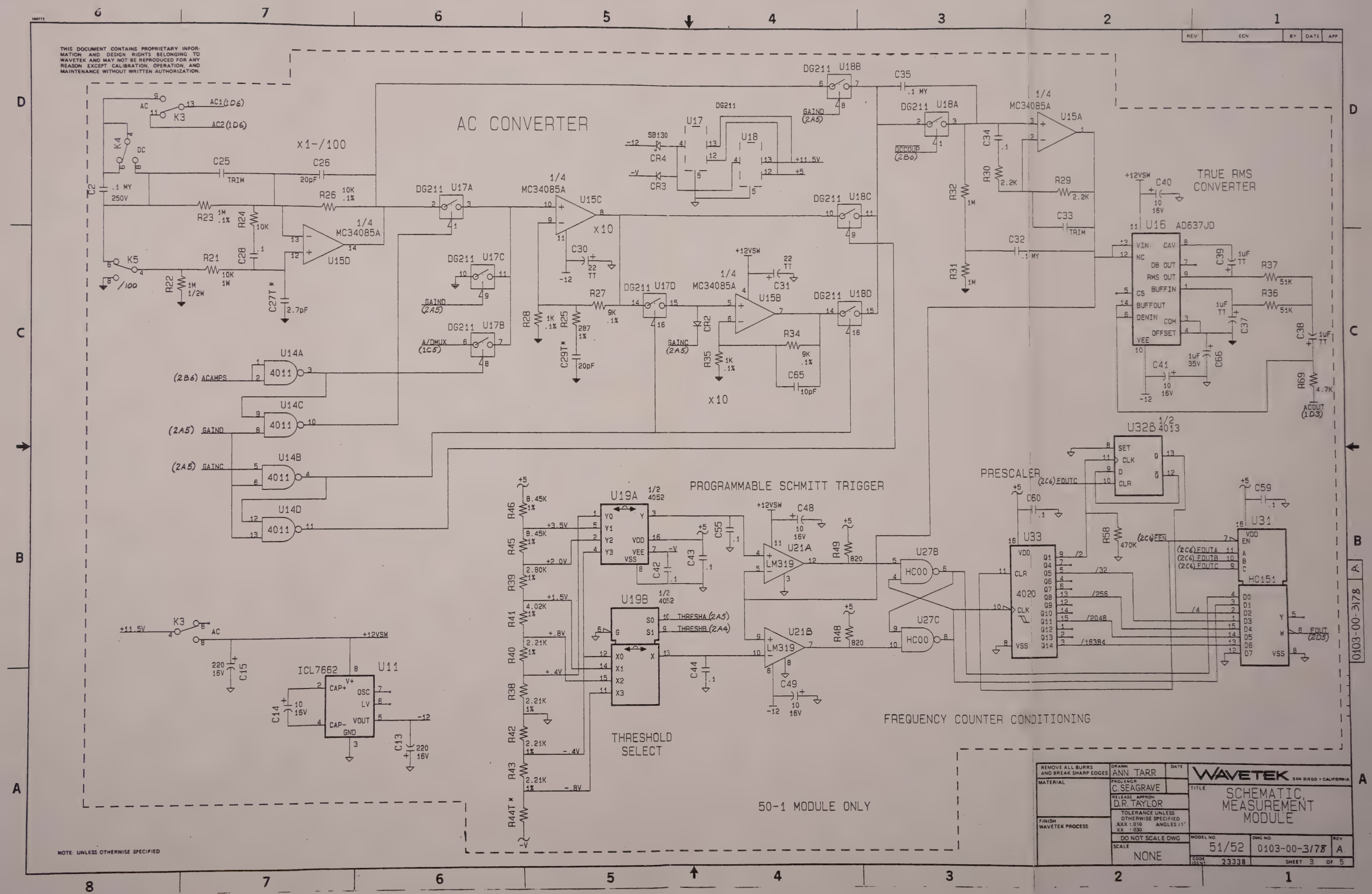
MODEL NO 51/52

DWG NO. 0103-00-3178

REV A

CODE IDENT 23338

SHEET 2 OF 5


AC CONVERTER
x1-/100
K3
AC1(1D6)
AC2(1D6)
K4
DC
C25 TRIM
C26 20pF
C2 .1 MY 250V
R23 1M .1%
R24 10K
R26 10K .1%
C28 .1
1/4 MC34085A U15D
K5
/100
R21 10K 1W
R22 1M 1/2W
C27T* 2.7pF
DG211 U17A
1/4 MC34085A U15C
x10
C30 22 TT
DG211 U17C
GAIND (2A5)
DG211 U17B
A/DMUX (1C5)
R28 1K .1%
R25 287 1%
C29T* 20pF
R27 9K .1%
DG211 U17D
GAINC (2A5)
CR2
1/4 MC34085A U15B
C31 22 TT
+12VSW
R35 1K .1%
R34 9K .1%
C65 10pF
x10
DG211 U17
SB130 CR4
CR3
U18
+11.5V
+5
DG211 U18B
C35 .1 MY
DG211 U18A
DCCOUP (2B6)
DG211 U18C
DG211 U18D
1/4 MC34085A U15A
C34 .1
R30 2.2K
R29 2.2K
C33 TRIM
R32 1M
R31 1M
C32 .1 MY
TRUE RMS CONVERTER
C40 10 16V
U16 AD637JD
VIN CAV NC DB OUT RMS OUT BUFFIN CS BUFFOUT DENIN COM OFFSET VEE
C39 1uF TT
R37 51K
R36 51K
C37 1uF TT
C38 1uF TT
C41 10 16V
C66 1uF 35V
R69 4.7K
ACOUT (1D3)
U14A 4011
(2B6) ACAMPS
U14C 4011
(2A5) GAIND
U14B 4011
(2A5) GAINC
U14D 4011
K3
+11.5V
AC
+12VSW
C15 220 16V
ICL7662 U11
CAP+ V+ OSC LV CAP- VOUT GND
C14 10 16V
C13 220 16V
-12
PROGRAMMABLE SCHMITT TRIGGER
R46 8.45K 1%
R45 8.45K 1%
R39 2.80K 1%
R41 4.02K 1%
R40 2.21K 1%
R38 2.21K 1%
R42 2.21K 1%
R43 2.21K 1%
R44T*
+3.5V +2.0V +1.5V +.8V +.4V -.4V -.8V
U19A 1/2 4052
Y0 Y1 Y2 Y3 Y VDD VEE VSS
C42 .1
C43 .1
C55 .1
U19B 1/2 4052
S0 S1 G
THRESHA (2A5)
THRESHB (2A4)
X0 X1 X2 X3 X
THRESHOLD SELECT
C44 .1
C48 10 16V
U21A LM319
U21B LM319
C49 10 16V
R49 820
R48 820
U27B HC00
U27C HC00
PRESCALER
(2C6) FOUTC
U32B 1/2 4013
SET CLK D CLR Q
C60 .1
U33 4020
VDD CLR CLK VSS Q1 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14
/2 /32 /256 /2048 /16384 /4
R58 470K
(2C6) FEN
(2C6) FOUTA
(2C6) FOUTB
(2C6) FOUTC
C59
U31 HC151
VDD EN A B C D0 D1 D2 D3 D4 D5 D6 D7 Y W VSS
FOUT (2D5)
FREQUENCY COUNTER CONDITIONING
50-1 MODULE ONLY
0103-00-3178
A

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

DRAWN ANN TARR

PROJ ENGR C. SEAGRAVE

RELEASE APPROV D.R. TAYLOR

TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 .XX ±.030 ANGLES ±1°

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC, MEASUREMENT MODULE

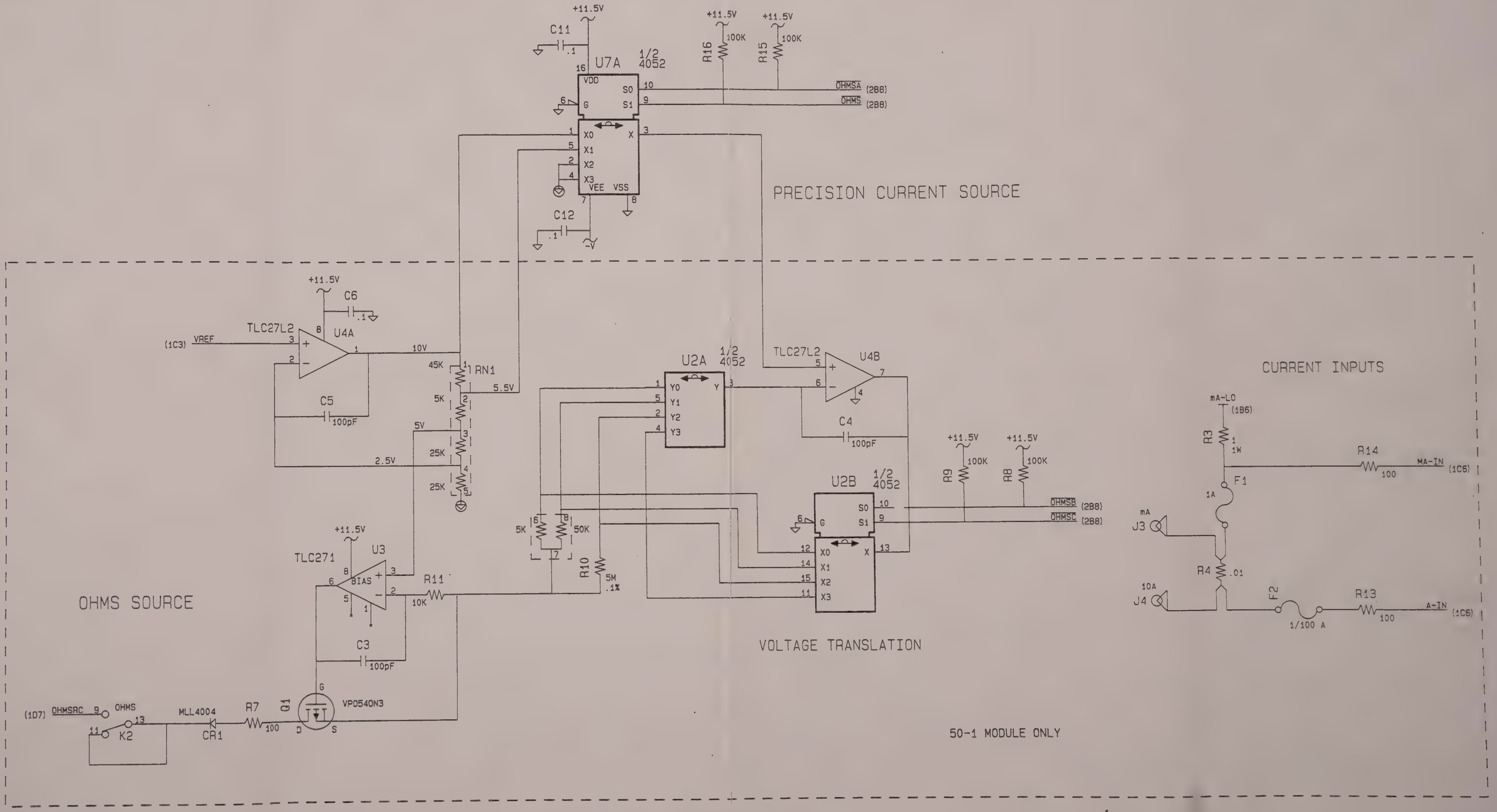
MODEL NO. 51/52

DWG NO. 0103-00-3178

REV A

CODE IDENT 23338

SHEET 3 OF 5


PRECISION CURRENT SOURCE
+11.5V
C11
.1
U7A
1/2
4052
VDD
S0
S1
G
X0
X1
X2
X3
X
VEE
VSS
C12
.1
-V
R16
100K
R15
100K
OHMSA (2B8)
OHMS (2B8)
OHMS SOURCE
TLC27L2
U4A
C6
.1
(1C3) VREF
10V
45K
RN1
5.5V
5K
5V
25K
2.5V
25K
C5
100pF
TLC271
U3
BIAS
R11
10K
C3
100pF
(1D7) OHMSRC
OHMS
K2
MLL4004
CR1
R7
100
Q1
VP0540N3
G
D
S
VOLTAGE TRANSLATION
U2A
1/2
4052
Y0
Y1
Y2
Y3
Y
TLC27L2
U4B
C4
100pF
5K
50K
R10
5M
.1%
U2B
1/2
4052
S0
S1
G
X0
X1
X2
X3
X
R9
100K
R8
100K
OHMSB (2B8)
OHMSC (2B8)
CURRENT INPUTS
mA-LO
(1B6)
R3
1
1W
R14
100
MA-IN
(1C6)
F1
1A
mA
J3
R4
.01
10A
J4
F2
1/100 A
R13
100
A-IN
(1C6)
50-1 MODULE ONLY

NOTE: UNLESS OTHERWISE SPECIFIED

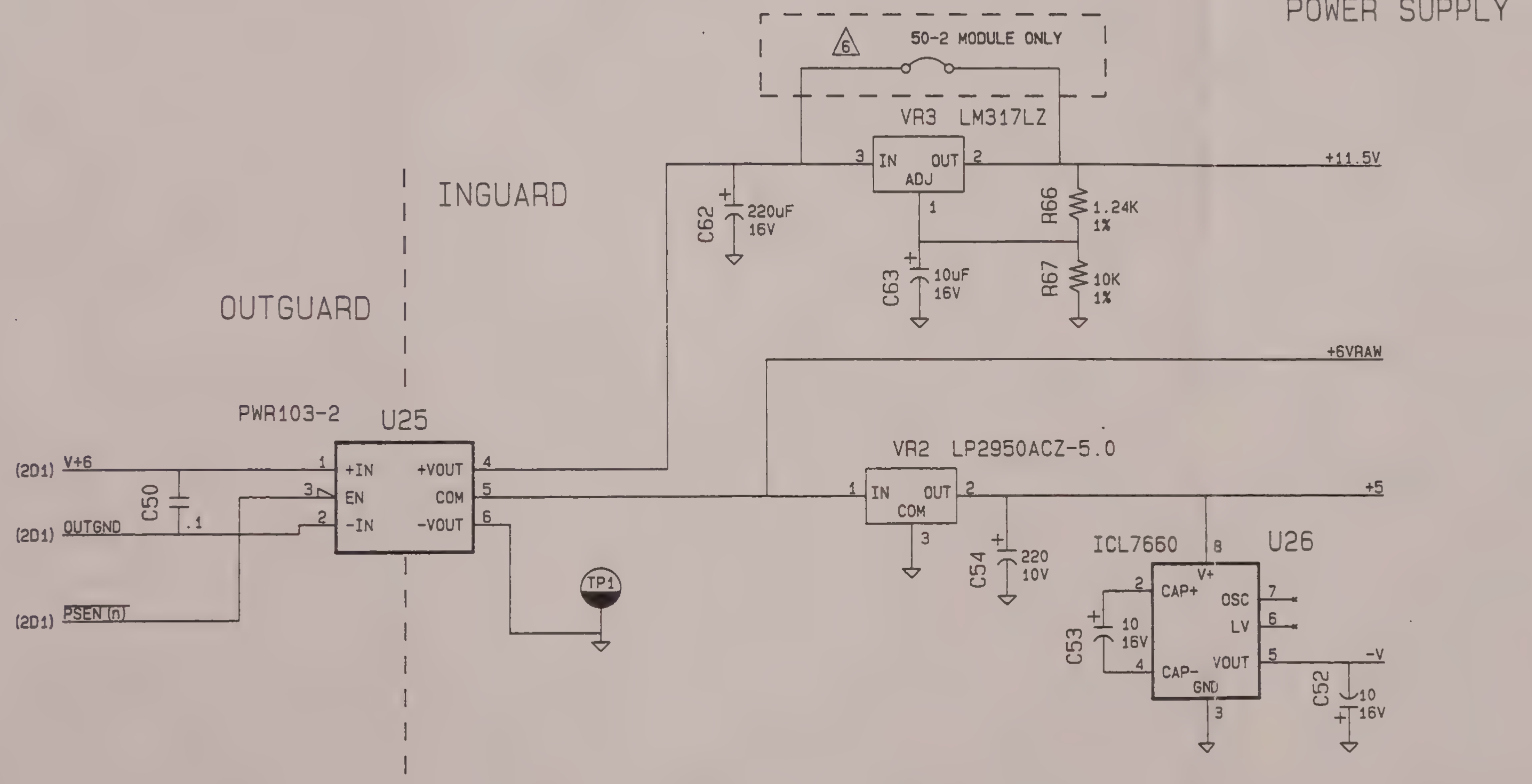
REV	ECO	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TARR	DATE 2/86	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL —//—	CHECKED C.SEAGRAVE	2/86	TITLE SCHEMATIC, MEASUREMENT MODULE	
	PROJ. ENGR. C.SEAGRAVE	2/86		
FINISH WAVETEK PROCESS —//—	RELEASE APPROV. D.R.TAYLOR	2/86		
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D FSCM NO. 23338 DWG. NO. 0103-00-3178	REV A
DO NOT SCALE DRAWING			SCALE NONE MODEL 51/52	SHEET 4 OF 5

0103-00-3178 A

REV	ECO	BY	DATE	APP

POWER SUPPLY



50-2 MODULE ONLY
6
VR3 LM317LZ
IN
OUT
ADJ
3
2
1
+11.5V
C62
220uF
16V
C63
10uF
16V
R66
1.24K
1%
R67
10K
1%
INGUARD
OUTGUARD
+6VRAW
PWR103-2
U25
(2D1) V+6
(2D1) OUTGND
(2D1) PSEN (n)
C50
.1
+IN
EN
-IN
+VOUT
COM
-VOUT
1
3
2
4
5
6
TP1
VR2 LP2950ACZ-5.0
IN
OUT
COM
1
2
3
+5
C54
220
10V
ICL7660
U26
8
V+
CAP+
CAP-
OSC
LV
VOUT
GND
2
4
7
6
5
3
C53
10
16V
-V
C52
10
16V

POWER & GROUND TABLE

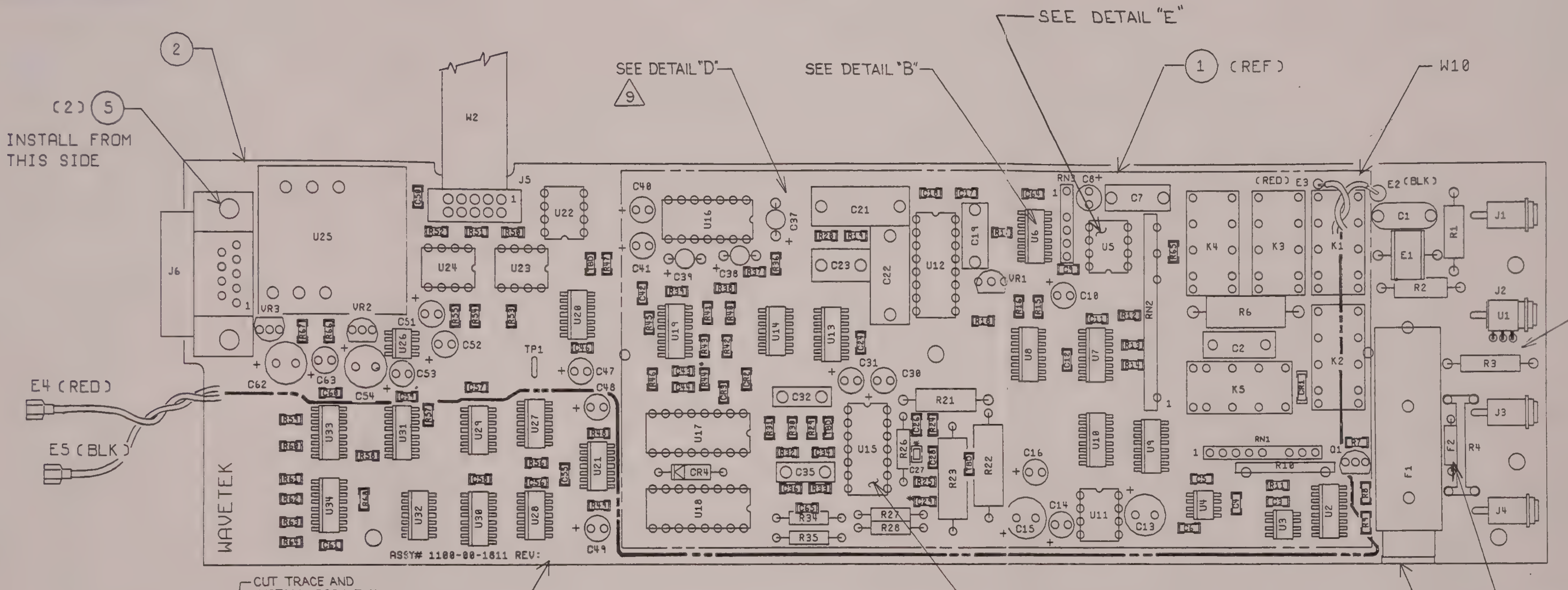
REFERENCE DES.	PIN NUMBER		
	+11.5V	+5	GND
U2	16		7.8
U3	7		4
U10		16	8
U14		14	7
U24		8	5
U27		14	7
U28		14	7
U32		14	7

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TARR	DATE 2/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	CHECKED C.SEAGRAVE	2/86	TITLE SCHEMATIC, MEASUREMENT MODULE
	PROJ. ENGR. C.SEAGRAVE	2/86	
FINISH WAVETEK PROCESS —//—	RELEASE APPROV. D.R.TAYLOR	2/86	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 0103-00-3178 · REV A
DO NOT SCALE DRAWING			SCALE NONE · MODEL 51/52 · SHEET 5 OF 5

0103-00-3178 A

REV	ECN	BY	DATE	APP
A	ECO #9898	MS	10/27/86	[illegible]


SEE DETAIL "E"
SEE DETAIL "D"
9
SEE DETAIL "B"
1 (REF)
W10
2
(2) 5
INSTALL FROM THIS SIDE
W2
J5
J6
U25
U22
U24
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U21
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R6
R1
R2
R3
R4
R10
RN1
RN2
RN3
K1
K2
K3
K4
K5
E1
E2 (BLK)
(RED) E3
E4 (RED)
E5 (BLK)
F1
F2
Q1
J1
J2
J3
J4
U1
WAVETEK
ASSY# 1100-00-1811 REV:
SEE DETAIL "A"

CUT TRACE AND INSTALL R69 (4.7K). RTV TO P.C. BOARD

SOLDER TO FEEDTHRU

SOLDER TO TRACE

4

SEE DETAIL "C"

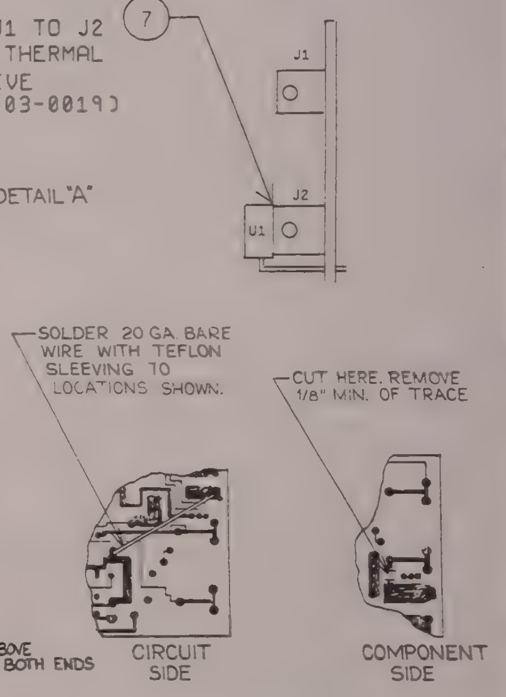
8

INSTALL F2 APPROX. 1/4" ABOVE BOARD AND TEFLON SLEEVE BOTH ENDS

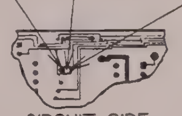
3

BOND U1 TO J2 USING THERMAL ADHESIVE (1600-03-0019)

7

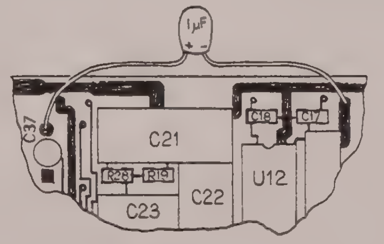

J1
J2
U1
SOLDER 20 GA BARE WIRE WITH TEFLON SLEEVING TO LOCATIONS SHOWN.
CUT HERE. REMOVE 1/8" MIN. OF TRACE
CIRCUIT SIDE
COMPONENT SIDE

DETAIL "A"

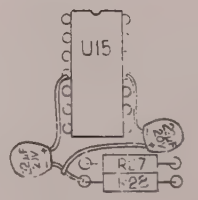


CIRCUIT SIDE

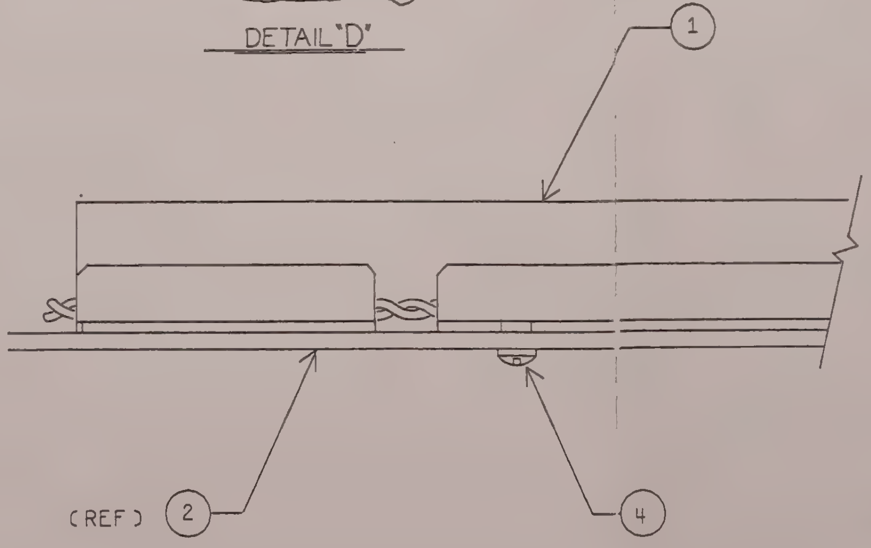
DETAIL "B"

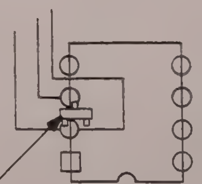

1µF
C37
C21
C22
C23
U12

DETAIL "D"



DETAIL "C"



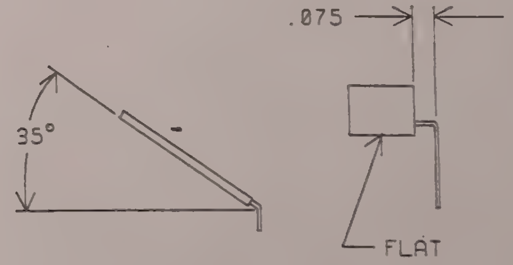


DETAIL "E"

CIRCUIT SIDE

SCALE: NONE

10 RTV TO PC BOARD



RN2

U1

SPECIAL COMPONENT PREP

SCALE: NONE

10 ADD CR6 BETWEEN PINS 2&3 OF U5 ON CIRCUIT SIDE OF BOARD.

9 ADD A 22GA BARE WIRE WITH TEFLON SLEEVING TO (+) LEAD OF 1UF CAP, SOLDER TO (-) LEAD OF C37 TOPSIDE; SOLDER (-) LEAD OF 1UF CAP TO GROUND HOLE NEAR C19. RTV THE BODY OF 1UF CAP TO P.C. BOARD. (SEE DETAIL "D".)

8 BEND LEADS OF 2 CAPS ABOUT 1/4" HIGH, SOLDER (+) LEAD TO PIN 4, (-) LEAD TO PIN 11 OF U15. SOLDER 2 REMAINING LEADS TOGETHER, BEND 1/4" HIGH, SOLDER TO R28. (SEE DETAIL "C".)

7. * = NOMINAL VALUE CALLED OUT ON PARTS LIST.

6. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.

5. TRIM COMPONENT LEADS TO A MAXIMUM HEIGHT OF .045 FROM BOARD SURFACE.

4 MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.

3. SEE INSTRUMENT SCHEMATIC 0004-00-0440 FOR ASSEMBLY INTERCONNECTION FOR 51/52 OR 0004-00-0539 FOR 52A

2. SEE 0103-00-3178 FOR CIRCUIT SCHEMATIC.

1. SEE PARTS LIST 1100-00-3178.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1101-00-3178

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL —//—
FINISH WAVETEK PROCESS —//—
DRAWN B. REDMAN
DATE
PROJ ENGR C.SEAGRAVE 4/23/86
RELEASE APPROV D.R.TAYLOR
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 .XX ±.030 ANGLES ±1°
DO NOT SCALE DWG
SCALE 2/1
WAVETEK SAN DIEGO • CALIFORNIA
TITLE PCA, MEASUREMENT MODULE (50-1)
MODEL NO 51/52
DWG NO. 1100-00-3178
REV A
CODE IDENT 23338
SHEET 1 OF 1

1100-00-3178 R

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, MEASUREMENT MODULE 50-1	0103-00-3178	WVTK	0103-00-3178	1
W10	ASSY, CABLE (W-10)	1207-00-2806	WVTK	1207-00-2806	1
NONE	KIT, SMD LOAD (52-1811)	1208-00-2864	WVTK	1208-00-2864	1
NONE	FRONT PANEL, 4-CHANNEL	1400-02-0840	WVTK	1400-02-0840	1
NONE	LABEL, CHANNEL, 4 POSITION	52-1090	WVTK	1400-02-1090	1
C1	CAP, CER, .01/500V	ECK-D2H103ZEE	PANAS	1500-01-0306	1
C14 C16 C40 C41 C47 C48 C49 C51 C52 C53 C63	CAP, ELECT, 10MF, 20%, 16V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	11
C54	CAP, ELECT, 220MF/10V	ECEA1AU221	PANAS	1500-32-2001	1
C13 C15 C62	CAP, ELECT, 220MF, 20%, 16V, RADIAL	SSM220M16S	ITT	1500-32-2104	3
C2	CAP, MET, POLY, .1MF, 250V	160-.1-J250D	WEST	1500-41-0405	1
C19 C7	CAP, MET POLY, .1PP, 160V	171-.1-J160D	WEST	1500-41-0434	2
C23	CAP, MET POLY, 1MF/63V	167-1-J63D	WEST	1500-41-0503	1
C21 C22	CAP, MET POLY, 022PP, 160V	171-.22-J160H	WEST	1500-42-2025	2
C32 C35	CAP, MET, POLY, .1MF, 63V, .5% RAD LEAD SP .3	167/.1/J/63/A	WEST	1500-43-0413	2
C37 C38 C39 C66	CAP, TANT, 1MF, 35V	196D105X0035HA1	SPRAG	1500-71-0512	4
C30 C31	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	2
C10 C8	CAP, TANT, 33MFD, 6V, RADIAL, LS .125	199033696R3CA1	SPRAG	1500-73-3602	2
7	ADHESIVE, THERMAL, EPOXY	00241	LKTIT	1600-03-0019	1
J1 J2 J3 J4	PC JACK	09-9094-1-04	CONCD	2100-02-0190	4
J6	CONN, RT ANGLE PC MOUNT, 9 PIN	745394-2	AMP	2100-02-0200	1
TP1	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	1
F1	FUSE, 1A, 250V	312001	LITFU	2400-05-0007	1
3	FUSE HOLDER, PCB MOUNT	345101	LITFU	2400-05-0043	1
E1	SPARK GAP	BZ-B600	SIEM	2400-05-0046	1
F2	FUSE, AXIAL LEAD MOUNT, 10MA	GFA1/100A	BUSS	2400-05-0054	1
4	SCREW, 4-40X3/16, PHP, NYLOK PATCH	4-40 X 3/16	CMRCL	2800-23-4103	1
NONE	WASHER, FLAT, NYLON, 0.245 OD, 0.128 ID	5610-55-20	SESTM	2800-26-0026	2
NONE	SNAP RIVIT SHOULDER, RELEASABLE, NYLON	SR 3065 B	RICH	2800-60-0002	2
5	PIN SNAPLOCK, NYLON, PERMANENT, 1/8 HOLE	SLP-125.01	RICH	2800-60-0003	2
K1 K2 K3 K4 K5	RELAY, 2 FORMC	DS2E-SL2-DC5V	AROMT	4500-00-0028	5
R22	RES, C, 1/2W, 2%, 1M	DCS-1/2	DALE	4700-24-1004	1
R28 R35	RES, MF, 1/8W, .1%, 1K	RN55E-1001B	MEPCO	4701-02-1001	2
R26	RES, MF, 1/8W, .1%, 10K	RN55E-1002B	MEPCO	4701-02-1002	1
R27 R34	RES, MF, 1/8W, .1%, 9K	5023ZE9K00B	MEPCO	4701-02-9001	2
R23	RES, MFLM 1 MEG 0.1%	CMF-65 1004 B T-9	DALE	4701-32-1004	1
R21	RES, MF, 1W, 5%, 10K	RSF1B	MICRO	4701-35-1002	1
R10	RES, MF, .33W, .1%, 5M	TF626R	CADD	4701-82-5004	1
R3	RES, WW, 1W, 1%, 1	RS1A 1 OHM 1%	DALE	4702-33-1009	1
R4	RES, WW, 10W, .5%, .01	SPR-676	DALE	4702-79-0107	1
R69	RES, SMD GP 1/8 LONG 200PPM 5% 4.7K OHM	MCR18EZH472JW5%	ROHM	4703-20-4725	1
RN2	RES NETWORK	1776-8	CADDO	4770-00-0040	1
RN3	RES NETWORK	T1794-180-2	CADDO	4770-00-0041	1
RN1	RES NETWORK	T1794-181	CADDO	4770-00-0042	1
R6	RES, CC, 1W, 10%, 100K	GB1041	AB	4799-00-0092	1
R1 R2	RES, CC, 1/2W, 5%, 51K	EB5131	AB	4799-00-0093	2
CR4	DIODE, STTKY	SB130	GI	4806-02-0130	1
CR6	DIODE, SCHOTTKY BARRIER, SMT	HSMS 2820	HP	4899-00-0061	1
G1	TRANS, FET, P-CHANNEL	VP0540N3	SUPER	4902-05-4000	1
W2	RIBBON CABLE ASSEMBLY, 10 PIN, 10"	6002-00-0043	WVTK	6002-00-0043	1
U1	CENTIGRADE TEMP SENSOR	LM35DZ	NAT	7000-00-3500	1
VR3	VOLT REGULATOR	LM317LZ	MOT	7000-03-1701	1
U12	ANALOG PROCESSOR	TSC500L	TELE	7000-05-0000	1
U16	RMS TO DC	AD637JD	ANDEV	7000-06-3700	1
U5	PICOAMP INPUT MIC VOLT OFFSET LOW NOISE	LT1012CN8	LINTE	7000-10-1200	1
U25	POWER SUPPLY	PWR103-2	BUR	7000-10-3201	1
VR2	REGULATOR, MICROPOWER VOLTAGE, 3 PIN	LP2950ACZ-5.0V	NSC	7000-29-5000	1
U11	CONVERTER, DC TO DC, 500MW, 8 PIN DIP, CMOS	ICL7662CPA	INTSL	7000-76-6201	1
VR1	VOLTAGE REFERENCE	7003-00-7400	WVTK	7003-00-7400	1
U15	OP AMP QUAD HIGH SPEED	MC34085AP	MOT	7003-40-8500	1
U22 U23	OPTO CPLP, FAST	6N136	SPECT	7100-00-0001	2
U17 U18	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	2
U24	OPTOCOUPL, DUAL, LOW INPUT, HIGH GAIN	HCLP2730	HP	8000-27-3000	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/x	.xxx	.xx	∠
± 1/64	± .005	± .01	± 1°

MATERIAL:
FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

	DATE
DRAWN	
CHKD	
ENG APPR.	
MFG APPR.	
ISSUED	

WAVETEK
Wavetek Inc.

TITLE
PARTS LIST
PCA, MEASUREMENT MODULE

SIZE D
MODEL NO 50-1
DRAWING NO 1100-00-3178
REV A
SCALE:
CODE IDENT 23338
SHEET 1 OF 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C65	CAP, SMD CER 5% 50V NPO 10PF	C1206C100D2GAC	KEMET	1500-81-0001	1
C3 C4 C5 C9	CAP, SMD CER 5% 50V NPO 100PF	C1206C101J2GAC	KEMET	1500-81-0101	4
C11 C12 C17 C18 C24 C28 C34 C42 C43 C44 C46 C50 C55 C56 C57 C58 C59 C6 C60 C61 C64	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	21
C26	CAP, SMD CER 2% 50V 20PF	C1206C200G5GAC	KEMET	1500-82-0001	1
C27T	CAP, SMD CER NPO 0805 STD SIZE 2.7PF+-0.5	C0805C279D2GAC	KEMET	1500-82-7901	1
C29T	CAP, SMD CER 5% 50V 33PF	C1206C330J2GAC	KEMET	1500-83-3001	1
2	DRILL DRWG, PCA, CHANNEL BOARD	1700-1811	WVTK	1700-00-1811	1
R13 R14 R7	RES, SMD GP 1/8 LONG 200PPM 5% 100 OHM	9C12063A1000JLR	MEPCO	4703-20-1015	3
R11 R18 R24 R59 R60 R61 R62 R63 R64 R68	RES, SMD GP 1/8 LONG 200PPM 5% 10K OHM	MCR18EZH103JW5%	ROHM	4703-20-1035	10
R15 R16 R56 R65 R8 R9	RES, SMD GP 1/8 LONG 200PPM 5% 100K OHM	MCR18EZH104JW5%	ROHM	4703-20-1045	6
R31 R32	RES, SMD GP 1/8 LONG 200PPM 5% 1M OHM	MCR18EZH105JW5%	ROHM	4703-20-1055	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	KIT, SMD LOAD (52-1811)	1208-00-2864 PAGE 1	B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R20	RES, SMD GP 1/8 LONG 200PPM 5% 22 OHM	MCR18EZH220JW5%	ROHM	4703-20-2205	1
R12 R17 R29 R30 R50 R51 R52 R53 R54 R55	RES, SMD GP 1/8 LONG 200PPM 5% 2.2K OHM	MCR18EZH222JW5%	ROHM	4703-20-2225	10
R19	RES, SMD GP 1/8 LONG 200PPM 5% 220K OHM	9C12063A2203JLR	MEPCO	4703-20-2245	1
R47	RES, SMD, GP, 1/8 LONG, 200PPM, 5%, 470	0108-00-2766	WVTK	4703-20-4715	1
R57 R58	RES, SMD GP 1/8 LONG 200PPM 5% 470K OHM	MCR18EZH474JW5%	ROHM	4703-20-4745	2
R36 R37	RES, SMD GP 1/8 LONG 200PPM 5% 51K OHM	MCR18EZH513JW5%	ROHM	4703-20-5135	2
R48 R49	RES, SMD GP 1/8 LONG 200PPM 5% 820 OHM	MCR18EZH821JW5%	ROHM	4703-20-8215	2
R67	RES, SMD 1/8 LONG 100PPM 1% 10K OHM	9C12063A1002FKR	MEPCO	4703-21-0021	1
R66	RES, SMD 1/8 LONG 100PPM 1% 1.24K OHM	MCR18FXTA1241F	ROHM	4703-21-2411	1
R38 R40 R42 R43	RES, SMD 1/8 LONG 100PPM 1% 2.21K OHM	9C12063A2211FKR	MEPCO	4703-22-2111	4
R44T	RES, SMD 1/8 LONG 100PPM 1% 23.7K OHM	9C12063A2372FKR	MEPCO	4703-22-3721	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	KIT, SMD LOAD (52-1811)	1208-00-2864 PAGE 2	B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R39	RES, SMD 1/8 LONG 100PPM 1% 2.80K OHM	9C12063A2801FKR	MEPCO	4703-22-8011	1
R25	RES, SMD 1/8 LONG 100PPM 1% 287 OHM	MCR18FXTA2870F	ROHM	4703-22-8701	1
R41	RES, SMD 1/8 LONG 100PPM 1% 4.02K OHM	MCR18FXTA4021F	ROHM	4703-24-0211	1
R45 R46	RES, SMD 1/8 LONG 100PPM 1% 8.45K OHM	9C12063A8451FKR	MEPCO	4703-28-4511	2
CR1	G.P. RECTIFIER 400V, 1A LEADLESS IN4004, SMD	MLL4004	MOT	4806-03-4004	1
CR2 CR3	DIODE, LEADLESS EQUIVALENT IN4148, 500MW, SMD	RLS4148	ROHM	4807-01-4148	2
U3	OP AMP, PROGRAM, SMD	TLC271ACD	TI	7000-02-7101	1
U4	OPERATIONAL AMPLIFIER, DUAL, SMD	TLC27L2ACD	TI	7000-02-7210	1
U21	COMPARATOR, DUAL DIFFERENTIAL, SMD	LM319D	SIG	7000-03-1900	1
U8 U9	DARLINGTON TRANSISTOR ARRAY, SMD	ULN2004D	SIG	7000-20-0001	2
U19 U2 U6 U7	MUL/DEMUL, DUAL 4	HEF4052BTD	SIG	7000-40-5200	4

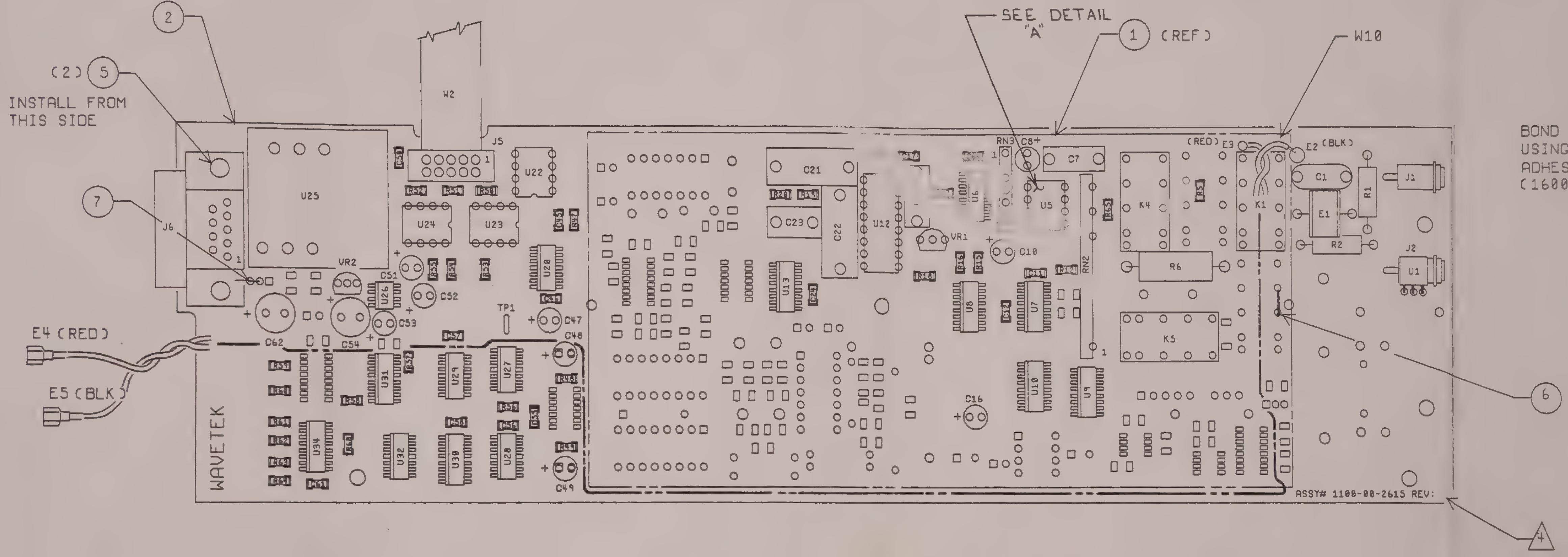
WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	KIT, SMD LOAD (52-1811)	1208-00-2864 PAGE 3	B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	CHANNEL ANALOG, SMD				
U26	CONVERTER, DC TO DC, CMOS, 300MW, SMD	ICL7660CBA	INTSL	7000-76-6041	1
U14	GATE, NAND, SO, QUAD 2-INPUT, SMD	HEF 4011BTD	SIG	8000-40-1102	1
U28 U32	FLIP-FLOP, DUAL D, CMOS, SMD	HEF4013BTD	SIG	8000-40-1341	2
U33	COUNTER, CMOS, BINARY, 14-STAGE, RIPPLE-CARRY, SMD	HEF4020BTD	SIG	8000-40-2041	1
U10 U13 U30 U34	REG/LATCH 8-BIT SHIFT CMOS, SMD	HEF4094BTD	SIG	8000-40-9441	4
U27	GATE, NAND, QUAD, 2INP POS, SMD	74HC00D	SIG	8000-74-0041	1
U20	SCHMITT TRIG, NAND, QUAD 2-INP, SMD	74HC132D	SIG	8000-74-1320	1
U29	HEX SCHMITT TRIGGER/INVERTER, HCMOS, SMD	74HC14D	SIG	8000-74-1441	1
U31	MUX, 8 INP, CMOS	74HC151D	SIG	8007-41-5141	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	KIT, SMD LOAD (52-1811)	1208-00-2864 PAGE 4	B

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES		WAVETEK Wavetek Inc.
x/x ± 1/64 .xxx ± .005 .xx ± .01 ∠ ± 1°	DRAWN	DATE	TITLE PARTS LIST KIT, SMD LOAD (52-1811)
MATERIAL:	CHKD		
	ENG APPR.		
FINISH:	MFG APPR.		SIZE D MODEL NO. 50-1 DRAWING NO 1208-00-2864 REV B
	ISSUED		SCALE: CODE IDENT 23338 SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	ECO # 9898	MS	10/27 88	[illegible]


2
(2) 5
INSTALL FROM
THIS SIDE
7
J6
U25
W2
J5
U22
U24
U23
VR2
C51
C52
U26
TP1
C47
C48
C53
C54
C62
E4 (RED)
E5 (BLK)
WAVETEK
U31
U29
U27
U20
U34
U32
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U28
C49
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C22
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U12
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VR1
C10
U6
U8
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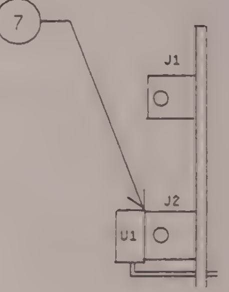
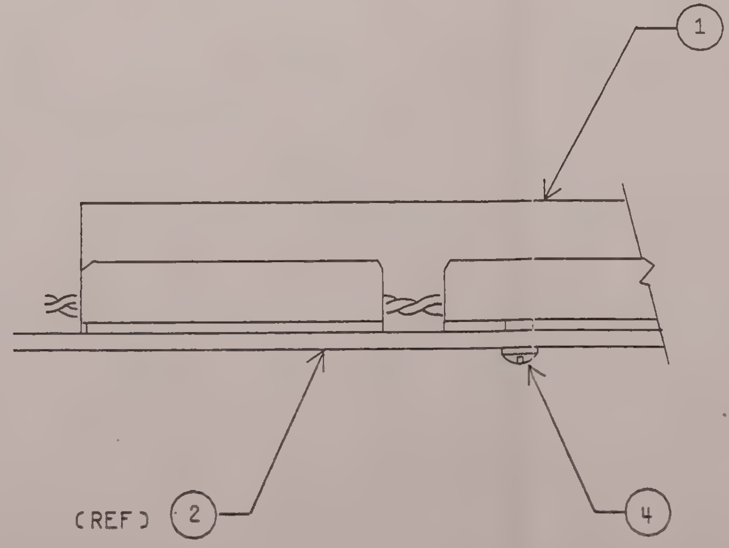
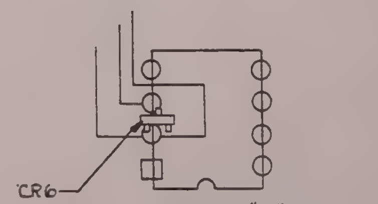
U10
U9
C16
SEE DETAIL
"A"
1 (REF)
RN3
C8
C7
U5
RN2
K4
K3
K1
R6
K5
(RED) E3
E2 (BLK)
W10
C1
E1
R1
R2
J1
J2
U1
6
ASSY# 1100-00-2615 REV:
4

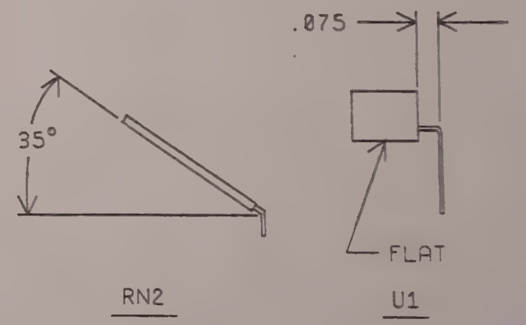
BOND U1 TO J2
USING THERMAL
ADHESIVE
(1600-03-0019)







DETAIL "A"
CIRCUIT SIDE
SCALE: NONE
△7 RTV TO PC BOARD


.075
35°
FLAT
RN2
U1

SPECIAL COMPONENT PREP
SCALE: NONE

SEE SEPARATE PARTS LIST 1101-00-2615

7. ADD CR6 BETWEEN PINS 2 & 3 OF U5 ON CIRCUIT SIDE OF BD.
6. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
5. TRIM COMPONENT LEADS TO A MAXIMUM HEIGHT OF .045 FROM BOARD SURFACE.
4. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
3. SEE INSTRUMENT SCHEMATIC 0004-00-0040 FOR ASSEMBLY INTERCONNECTION *FOR 51/52 OR 0004-00-0539 FOR 52A.*
2. SEE 0103-00-3178 FOR SCHEMATIC.
1. SEE PARTS LIST 1100-00-3177 .

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR SEAGRAVE		TITLE PCA, MEASUREMENT MODULE (50-2)
	RELEASE APPROV D.R.TAY_OR		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51/52 · DWG NO. 1100-00-3177 · REV A
	SCALE 2/1		CODE IDENT 23338 · SHEET 1 OF 1

1100-00-3177 A

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A3708

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, MEASUREMENT MODULE 50-1	0103-00-3178	WVTK	0103-00-3178	1
W10	ASSY, CABLE (W-10)	1207-00-2306	WVTK	1207-00-2806	1
NONE	KIT, SMD LOAD (52-2615)	1208-00-2365	WVTK	1208-00-2865	1
NONE	FRONT PANEL, 2-CHANNEL	52-0850	WVTK	1400-02-0850	1
NONE	LABEL, CHANNEL, 2 POSITION	52-1100	WVTK	1400-02-1100	1
C1	CAP, CER, .01/500V	ECK-D2H103ZEE	PANAS	1500-01-0306	1
C16 C47 C51 C52 C53	CAP, ELECT, 10MF, 20%, 16V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	5
C54	CAP, ELECT, 220MF/10V	ECEA1AU22:	PANAS	1500-32-2001	1
C62	CAP, ELECT, 220MF, 20%, 16V, RADIAL	SSM220M169	ITT	1500-32-2104	1
C19 C7	CAP, MET POLY, .1PP, 160V	171-.1-J160D	WEST	1500-41-0434	2
C23	CAP, MET POLY, 1MF/63V	167-1-J63D	WEST	1500-41-0503	1
C21 C22	CAP, MET POLY, 022PP, 160V	171-.22-J160H	WEST	1500-42-2025	2
C10 C8	CAP, TANT, 33MFD, 6V, RAD	199033696+3CA1	SPRAG	1500-73-3602	2

WAVETEK PARTS LIST | TITLE: PCA, MEASUERMENT MODULE 50-2 | ASSEMBLY NO. 1100-00-3177 | REV A | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	IAL, LS .125				
7	ADHESIVE, THERMAL, EPOXY	00241	LKTIT	1600-03-0019	1
J1 J2	PC JACK	09-9094-1-04	CONCD	2100-02-0190	2
J6	CONN, RT ANGLE PC MOUNT, 9 PIN	745394-2	AMP	2100-02-0200	1
TP1	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	1
E1	SPARK GAP	BZ-B600	SIEM	2400-05-0046	1
6	JUMPER, .100	J 0.100X0.125 B22	SGIRS	2800-12-0049	1
7	JUMPER, .200	J 0.200X0.125 B22	SGIRS	2800-12-0050	1
4	SCREW, 4-40X3/16, PHP, NYLOK PATCH	4-40 X 3/15	CMRCL	2800-23-4103	1
NONE	WASHER, FLAT, NYLON, 0.245 OD, 0.128 ID	5610-55-20	SESTM	2800-26-0026	2
NONE	SNAP RIVIT SHOULDER, RELEASABLE, NYLON	SR 3065 B	RICH	2800-60-0002	2
5	PIN SNAPLOCK, NYLON, PERMANENT, 1/8 HOLE	SLP-125.01	RICH	2800-60-0003	2
K1 K4 K5	RELAY, 2 FORMC	DS2E-SL2-D:5V	AROMT	4500-00-0028	3

WAVETEK PARTS LIST | TITLE: PCA, MEASUERMENT MODULE 50-2 | ASSEMBLY NO. 1100-00-3177 | REV A | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RN2	RES NETWORK	1776-8	CADDO	4770-00-0040	1
RN3	RES NETWORK	T1794-180-2	CADDO	4770-00-0041	1
R6	RES, CC, 1W, 10%, 100K	GB1041	AB	4799-00-0092	1
R1 R2	RES, CC, 1/2W, 5%, 51K	EB5131	AB	4799-00-0093	2
CR6	DIODE, SCHOTTKY BARRIER, SMT	HSMS 2820	HP	4899-00-0061	1
W2	RIBBON CABLE ASSEMBLY, 10 PIN, 10"	6002-00-0043	WVTK	6002-00-0043	1
U1	CENTIGRADE TEMP SENSOR	LM35DZ	NAT	7000-00-3500	1
U12	ANALOG PROCESSOR	TSC500L	TELE	7000-05-0000	1
U5	PICOAMP INPUT MIC VOLT OFFSET LOW NOISE	LT1012CN8	LINTE	7000-10-1200	1
U25	POWER SUPPLY	PWR103-1	BUR	7000-10-3100	1
VR2	REGULATOR, MICROPOWER VOLTAGE, 3 PIN	LP2950ACZ-5.0V	NSC	7000-29-5000	1
VR1	VOLTAGE REFERENCE	7003-00-7400	WVTK	7003-00-7400	1
U22 U23	OPTO CPLP, FAST	6N136	SPECT	7100-00-0001	2
U24	OPTOCOUPL, DUAL, LOW INPUT, HIGH GAIN	HCLP2730	HP	8000-27-3000	1

WAVETEK PARTS LIST | TITLE: PCA, MEASUERMENT MODULE 50-2 | ASSEMBLY NO. 1100-00-3177 | REV A | PAGE 3

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/x	.xxx	.xx	∠
± 1/64	± .005	± .01	± 1°

MATERIAL:

FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

	DATE
DRAWN	
CHKD	
ENG APPR.	
MFG APPR.	
ISSUED	

WAVETEK
Wavetek Inc.

TITLE
PARTS LIST
PCA, MEASUREMENT MODULE

SIZE	MODEL NO.	DRAWING NO	REV
D	50-2	1100-00-3177	A

SCALE: | CODE IDENT 23338 | SHEET 1 OF 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C9	CAP, SMD CER 5% 50V NPO 100PF	C1206C101J2GAC	KEMET	1500-81-0101	1
C11 C12 C17 C18 C20 C24 C46 C50 C56 C57 C58 C61 C64	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	13
2	DRILL DRWG, PCA, CHANNEL BOARD	1700-1811	WVTK	1700-00-1811	1
R5	ZERO OHM JUMPER SMD 1/8 BODY LENGHT 2 AMP	MCR18-JPW	ROHM	4703-20-0000	1
R18 R59 R60 R61 R62 R63 R64 R68	RES, SMD GP 1/8 LONG 200PPM 5% 10K OHM	MCR18EZH103JW5%	ROHM	4703-20-1035	8
R15 R16 R56 R65	RES, SMD GP 1/8 LONG 200PPM 5% 100K OHM	MCR18EZH104JW5%	ROHM	4703-20-1045	4
R20	RES, SMD GP 1/8 LONG 200PPM 5% 22 OHM	MCR18EZH220JW5%	ROHM	4703-20-2205	1
R12 R17 R50 R51 R52 R53 R54 R55	RES, SMD GP 1/8 LONG 200PPM 5% 2.2K OHM	MCR18EZH222JW5%	ROHM	4703-20-2225	8
R19	RES, SMD GP 1/8 LONG 200PPM 5% 220K OHM	9C12063A2203JLR	MEPCO	4703-20-2245	1
R47	RES, SMD, GP, 1/8 LONG, 200PPM, 5%, 470	0108-00-2766	WVTK	4703-20-4715	1
R57 R58	RES, SMD GP 1/8 LONG 200PPM 5% 470K OHM	MCR18EZH474JW5%	ROHM	4703-20-4745	2

WAVETEK PARTS LIST	TITLE KIT, SMD LOAD (52-2615)	ASSEMBLY NO. 1208-00-2865 PAGE 1	REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R48 R49	RES, SMD GP 1/8 LONG 200PPM 5% 820 OHM	MCR18EZH821JW5%	ROHM	4703-20-8215	2
U8 U9	DARLINGTON TRANSISTOR ARRAY, SMD	ULN2004D	SIG	7000-20-0001	2
U6 U7	MUL/DEMUL, DUAL 4 CHANNEL ANALOG, SMD	HEF4052BTD	SIG	7000-40-5200	2
U26	CONVERTER, DC TO DC, CMOS, 300MW, SMD	ICL7660CBA	INTSL	7000-76-6041	1
U28 U32	FLIP-FLOP, DUAL D, CMOS, SMD	HEF4013BTD	SIG	8000-40-1341	2
U10 U13 U30 U34	REG/LATCH 8-BIT SHIFT CMOS, SMD	HEF4094BTD	SIG	8000-40-9441	4
U27	GATE, NAND, QUAD, 2INP POS, SMD	74HC00D	SIG	8000-74-0041	1
U20	SCHMITT TRIG, NAND, QUAD 2-INP, SMD	74HC132D	SIG	8000-74-1320	1
U29	HEX SCHMITT TRIGGER/INVERTER, HCMOS, SMD	74HC14D	SIG	8000-74-1441	1

WAVETEK PARTS LIST	TITLE KIT, SMD LOAD (52-2615)	ASSEMBLY NO. 1208-00-2865 PAGE 2	REV B

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE			
x/x ± 1/64	.xxx ± .005	.xx ± .01	∠ ± 1°
MATERIAL:			
FINISH:			

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

	DATE
DRAWN	
CHKD	
ENG APPR.	
MFG APPR.	
ISSUED	

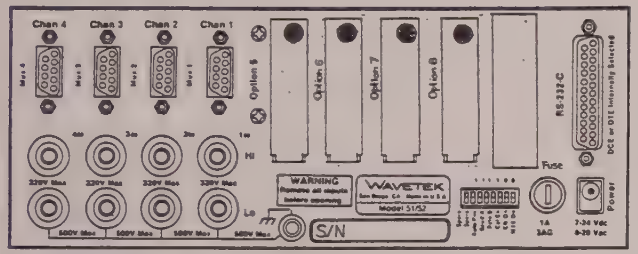
WAVETEK
Wavetek Inc.

TITLE
PARTS LIST
KIT, SMD LOAD
(52-2615)

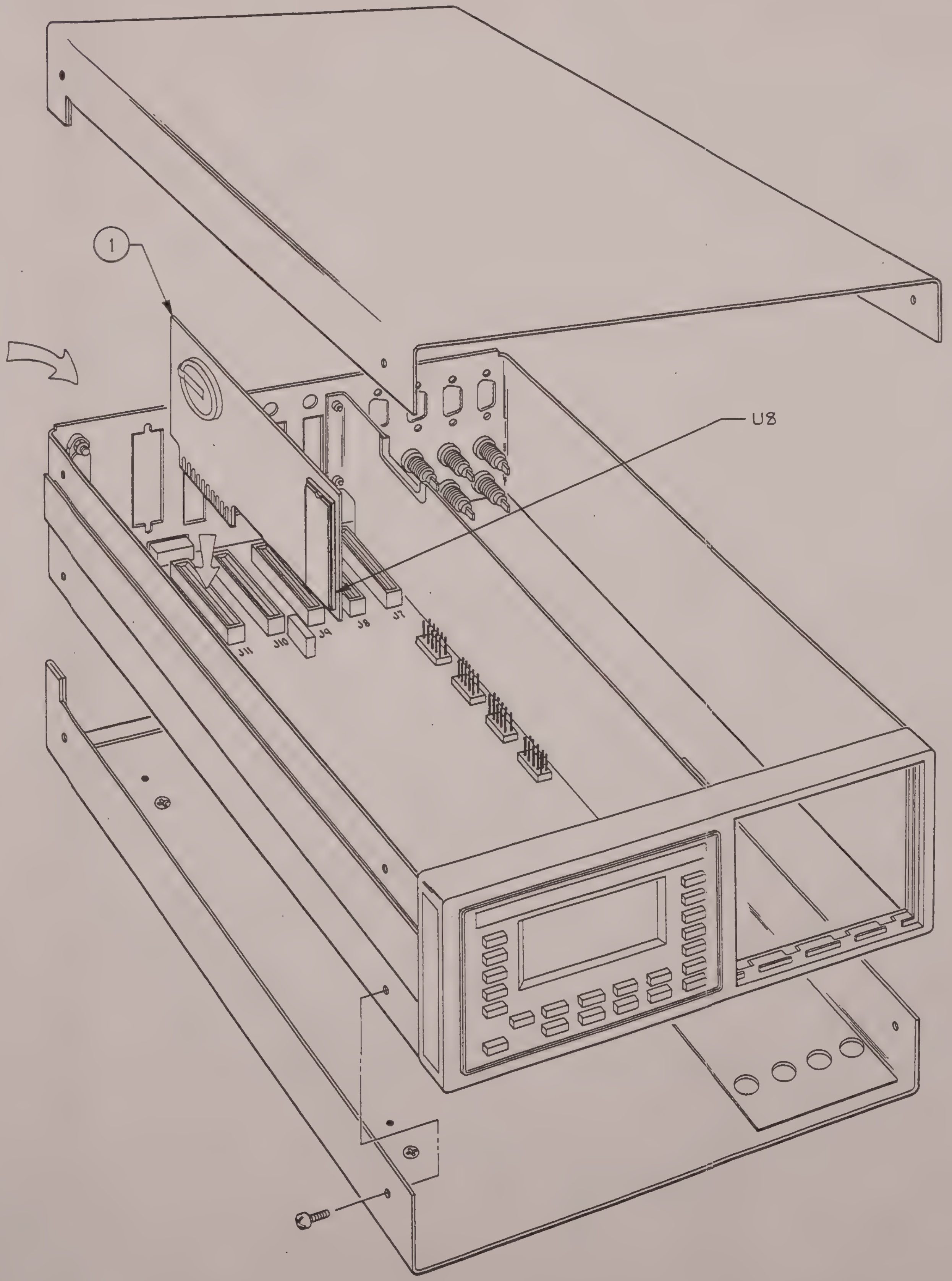
SIZE	MODEL NO.	DRAWING NO.	REV
D	50-2	1208-00-2865	B

SCALE: CODE IDENT 23338 SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE PER ERO#8287	AT	5/13/87	
B	ECO #89-026	HS	3/14/89	TM


Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS-232-C
DCE or DTE Internally Selected
Hi
Lo
320V Max
500V Max
WARNING
WAVETEK
Model 51/52
S/N
Fuse
1A 3AG
Power
7-34 Vdc
8-20 Vac

SAMPLE REAR PANEL CONFIGURATION


1
U8
J11
J10
J9
J8
J7

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	PCA, RAM BD 52A	1100-00-3182	WVTK	1100-00-3182	1
U8	RAM-128K X 8 CMOS STATIC 150ns	MH12808SNA-15	MITSU	8001-28-0800	1

WAVETEK PARTS LIST	TITLE OPTION 50-12A-128K, RAM EXPANSION BD	ASSEMBLY NO. 1000-00-0511 PAGE 1	REV B

3. RAM EXPANSION BOARD ASSEMBLY (OPTION 50-12A-128K) MAY BE INSTALLED IN EITHER J7 (REAR PANEL OPTION 5), J8, (REAR PANEL OPTION 6), J9 (REAR PANEL OPTION 7), J10 (REAR PANEL OPTION 8), OR J11. SPECIFIC SLOT IS DEPENDENT UPON TOTAL INSTRUMENT CONFIGURATION.

2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1000-00-0511

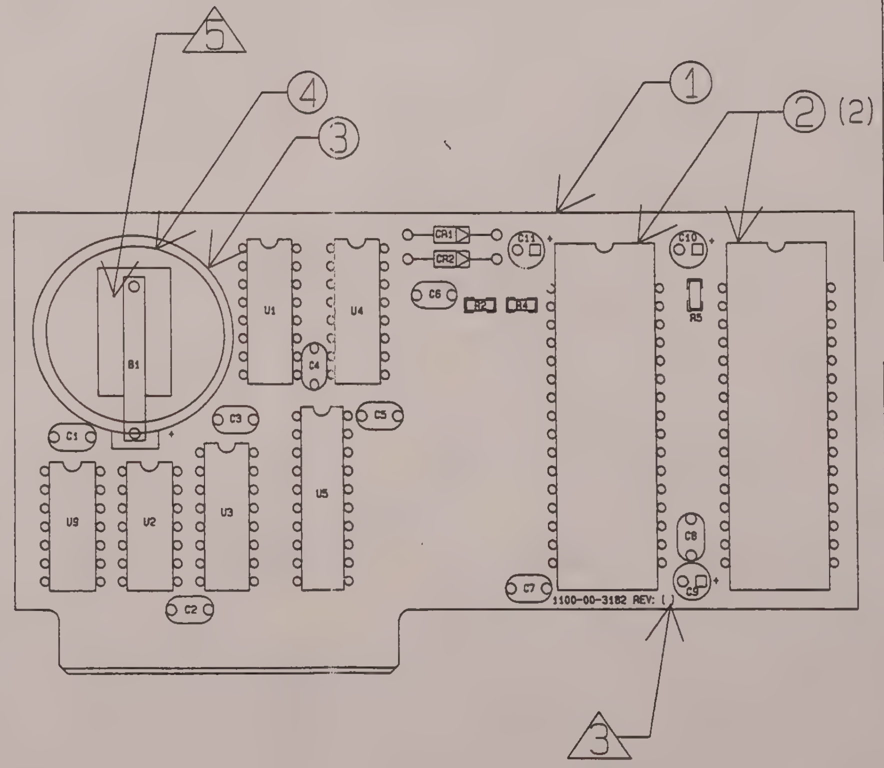
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3/13/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —/—	PROJ ENGR DR Taylor	5/19/87	TITLE ASSEMBLY, RAM EXPANSION BOARD OPTION 50-12A-128K
	RELEASE APPROV DL Taylor		
FINISH WAVETEK PROCESS —/—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO 51/52
	SCALE NONE		DWG NO. 1000-00-0511. REV B
			CODE IDENT 23338 SHEET 1 OF 1

1000-00-0511 B

REV	ECO	BY	DATE	APP
A	FOR RELEASE PER ERO #9943	OJ	10/17/88	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	SCHEMATIC, RAM/ROM BD 52A	0103-00-3181	WVTK	0103-00-3181	1
C1 C2 C3 C4 C5 C6 C7 C8	CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2	SR215E104ZAA	AVX	1500-01-0420	8
C10 C11 C9	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	3
NONE	PCB, RAM/ROM BD 52A	1700-00-3181	WVTK	1700-00-3181	1
2	SOCKET, DUAL WIPE, 32 PIN, .7 WIDE	ICO-326-S8-T	ROBNU	2100-03-0093	2
NONE	INSULATOR, IC PAD	818-030	BIVAR	2800-11-0035	1
3	BATTERY HOLDER, LITH COIN CELL	BH1000	MEMPD	3000-00-0175	1
4	BATTERY, 3V LITH, COIN CELL, 200 MAHR	DL2430	DURCL	4000-02-0012	1
R2 R4	ZERO OHM JUMPER SMD 1/8 BODY LENGHT 2 AMP	MCR18-JPW	ROHM	4703-20-0000	2
CR1 CR2	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	2
U2 U9	GATE, NAND, QUAD 2 INPUT, 14 PIN DIP	MC74HC00N	MOT	8000-74-0011 -	2
U1	DECODER/DEMUX, DUAL 1	MC74HC139N	MOT	8007-41-3911	1

WAVETEK PARTS LIST
TITLE PCA, RAM BD 52A
ASSEMBLY NO. 1100-00-3182
REV A
PAGE 1



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	OF 4, 16 PIN DIP				
U3 U4	FLIP-FLOP, HEX D, W/RESET	MC74HC174N	MOT	8007-41-7440	2
U5	LATCH, OCTAL TRANSPAR W/3 STATE, CMOS	SN74HC373N	TI	8007-43-7340	1

WAVETEK PARTS LIST
TITLE PCA, RAM BD 52A
ASSEMBLY NO. 1100-00-3182
REV A
PAGE 2

1100 00 3182 A

△5 INSTALL BATTERY (B1) USING A THIN PIECE OF MYLAR (OR EQUIV.) TO INSULATE "+" END OF BATTERY FROM IT'S CONTACT (THE CLIP ON ITEM 4) ONLY AFTER ALL SOLDER OPERATIONS ARE COMPLETED.

4. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

△3 MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.

2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440 (MODEL 51/52) OR 0004-00-0539 (MODEL 52A).

1. SEE 0103-00-3181 FOR SCHEMATIC.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPERATE PARTS LIST PL1100-00-3182

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

DRAWN O. Farr DATE 10/17/88
CHECKED
PROJ. ENGR.
RELEASE APPROV.

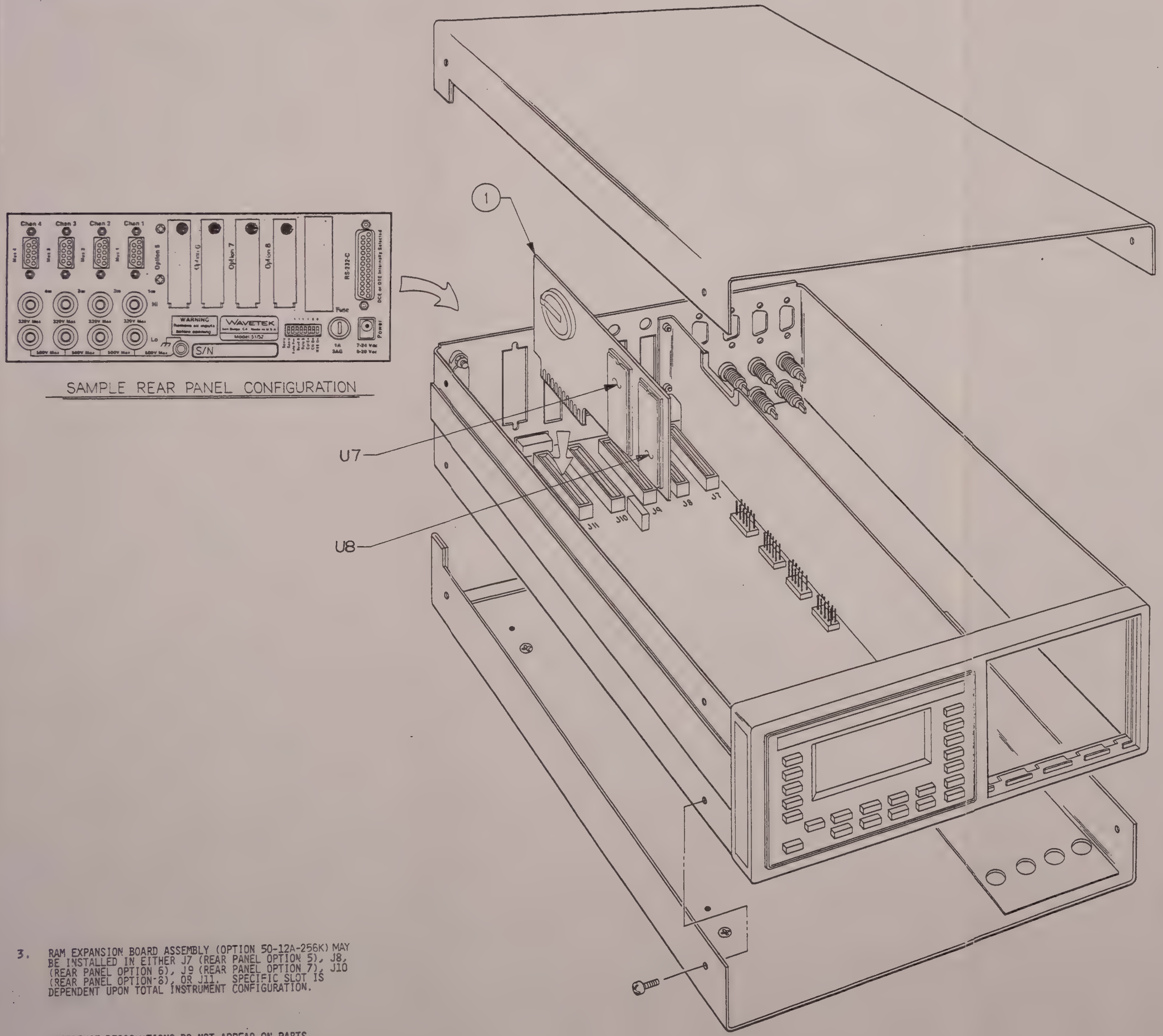
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PCA,
RAM BOARD

SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-3182
REV A
SCALE 2:1
MODEL 51/52/52A
SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	FOR RELEASE PER ERO#8287	JT	5/13/87	CL
B	ECO#89-026	BG	3 13 89	NM


Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS-232-C
DCE or DTE Internally Selected
Hi
Lo
320V Max
500V Max
WARNING
WAVETEK
Model 51/52
S/N
Fuse
1A
3AG
Power
7-24 Vac
9-30 Vac
1
U7
U8
J11
J10
J9
J8
J7

SAMPLE REAR PANEL CONFIGURATION

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	PCA, RAM BD 52A	1100-00-3182	WVTK	1100-00-3182	1
U7 U8	RAM-128K X 8 CMOS STATIC 150ns	MH12808SNA-15	MITSU	8001-28-0800	2

WAVETEK PARTS LIST
TITLE OPTION 50-12A-256K, RAM EXPANSION BD
ASSEMBLY NO. 1000-00-0512
REV B
PAGE 1

3. RAM EXPANSION BOARD ASSEMBLY (OPTION 50-12A-256K) MAY BE INSTALLED IN EITHER J7 (REAR PANEL OPTION 5), J8, (REAR PANEL OPTION 6), J9 (REAR PANEL OPTION 7), J10 (REAR PANEL OPTION 8), OR J11. SPECIFIC SLOT IS DEPENDENT UPON TOTAL INSTRUMENT CONFIGURATION.

2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440.

NOTE: UNLESS OTHERWISE SPECIFIED

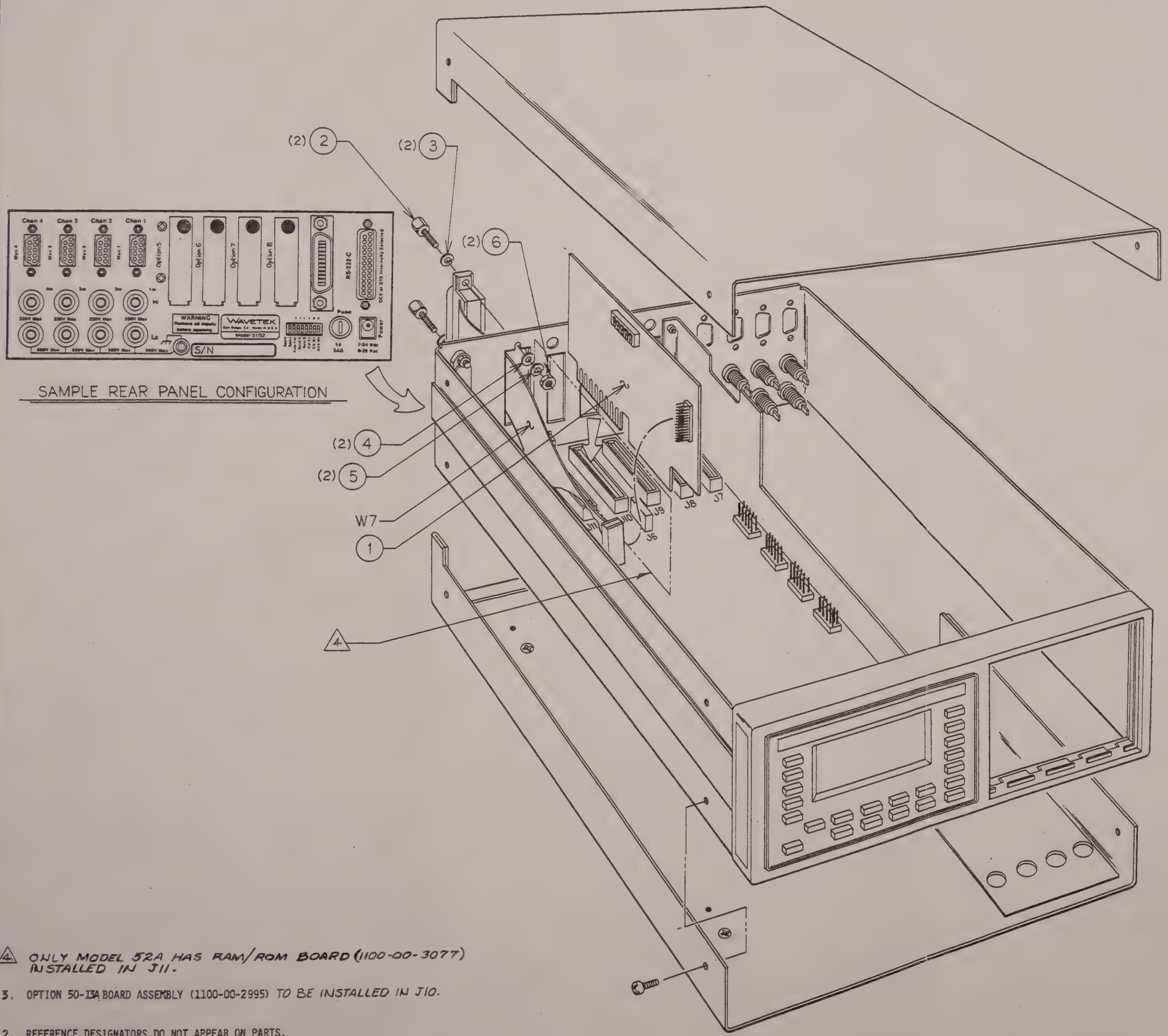
SEE SEPARATE PARTS LIST 1000-00-0512

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL —
FINISH WAVETEK PROCESS —
DRAWN D. COOPER
DATE
PROJ ENGR D R Taylor 5/19/87
RELEASE APPROV D R Taylor
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE ASSEMBLY, RAM EXPANSION BOARD OPTION 50-12A-256K
MODEL NO 51/52
DWG NO. 1000-00-0512
REV B
CODE IDENT 23338
SHEET 1 OF 1

1000-00-0512 B

BISHOP GRAPHICS/ACCUPRESS REORDER NO A2706

REV	ECN	BY	DATE	APP
A	FOR RELEASE PER ERO # 9008	MAG	8-7-87	A.R.T.
B	ECO # 9749	D.B.	6/21/88	


Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
RS-232-C
DCE or DTE Internally Selected
WARNING
WAVETEK
Model 51/52
Fuse
Power
S/N
(2) 2
(2) 3
(2) 6
(2) 4
(2) 5
W7
1
4
J11
J10
J9
J8
J7
J6

SAMPLE REAR PANEL CONFIGURATION

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT-52	0004-00-0440	WVTK	0004-00-0440	1
NONE	SCHEMATIC, INSTRUMENT-52A	0004-00-0539	WVTK	0004-00-0539	1
NONE	PCA, GPIB BD 50-13A	1100-00-3176	WVTK	1100-00-3176	1
2	JACK SCREW	859-0530	WVTK	1400-01-0530	2
6	NUT, HEX, 6-32, Z	MS35649-264	COML	2800-14-6100	2
4	WASHER, FLAT, #6 BIN 495	#6FLAT WASHER	CMRCL	2800-26-6001	2
5	#6 LOCKWASHER, PLATED	#6SRLW	CMRCL	2800-42-6000	2
3	LOCKWASHER, #8 SPLIT RING BIN 540	#8SRLW	CMRCL	2800-42-8000	2
W7	RIBBON CABLE ASSEMBLY, 24 PIN, 6.75"	6002-00-0044	WVTK	6002-00-0044	1

WAVETEK PARTS LIST	TITLE OPTION 50-13A IEEE-488 BOARD	ASSEMBLY NO. 1000-00-0525 PAGE 1	REV B

4. ONLY MODEL 52A HAS RAM/ROM BOARD (1100-00-3077) INSTALLED IN J11.
3. OPTION 50-13A BOARD ASSEMBLY (1100-00-2995) TO BE INSTALLED IN J10.
2. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440 FOR MODEL 51/52 OR 0004-00-0539 FOR MODEL 52A.

NOTE: UNLESS OTHERWISE SPECIFIED

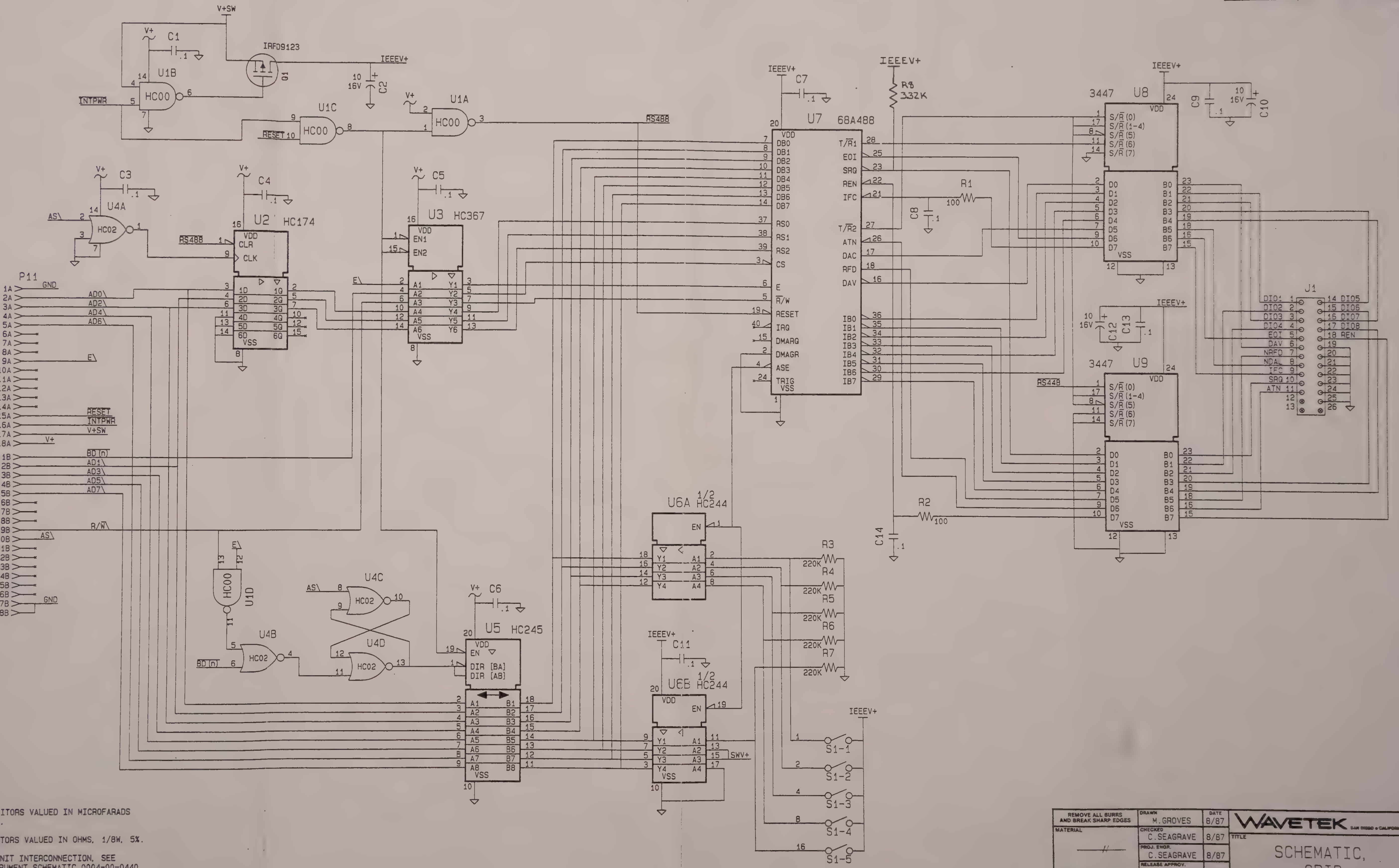
SEE SEPARATE PARTS LIST 1000-00-0525

REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN MOGraves DATE 8-7-87
PROJ ENGR Cotagove 8-10-87
RELEASE APPROV
MATERIAL —
FINISH WAVETEK PROCESS —
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
ASSEMBLY, IEEE-488
BOARD OPTION
(OPTION 50-13A)

MODEL NO. 51/52
DWG NO. 1000-00-0525
REV B
CODE IDENT 23338
SHEET 1 OF 1

REV	ECO	BY	DATE	APP
A	ECO # 9898	MS	10 27 88	


V+SW
C1
.1
U1B
HC00
INTPWR
IRFD9123
Q1
IEEEV+
10 16V
C2
U1C
U1A
RESET
RS488
V+
C3
U4A
HC02
AS\
C4
U2 HC174
CLR
CLK
C5
U3 HC367
EN1
EN2
P11
GND
AD0\
AD2\
AD4\
AD6\
E\
INTPWR
V+SW
BD(n)
AD1\
AD3\
AD5\
AD7\
R/W\
C7
U7 68A488
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
RS0
RS1
RS2
CS
RESET
IRQ
DMAGR
ASE
TRIG
T/R1
EOI
SRQ
REN
IFC
T/R2
ATN
DAC
RFD
DAV
IB0
IB1
IB2
IB3
IB4
IB5
IB6
IB7
R8
332K
R1
100
C8
3447 U8
C9
C10
S/R(0)
S/R(1-4)
S/R(5)
S/R(6)
S/R(7)
3447 U9
RS448
C12
C13
J1
DIO1
DIO2
DIO3
DIO4
EOI
DAV
NRFD
NDAC
IFC
SRQ
ATN
DIO5
DIO6
DIO7
DIO8
REN
R2
100
C14
U6A 1/2 HC244
R3
R4
R5
R6
R7
220K
U1D
U4C
U4B
U4D
C6
U5 HC245
DIR [BA]
DIR [AB]
C11
U6B 1/2 HC244
SWV+
S1-1
S1-2
S1-3
S1-4
S1-5

3. CAPACITORS VALUED IN MICROFARADS (uF).

2. RESISTORS VALUED IN OHMS, 1/8W, 5%.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440 (MODEL 51/52) OR 0004-00-0539 (MODEL 52A).

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL —//—

FINISH WAVETEK PROCESS —//—

DO NOT SCALE DRAWING

DRAWN M.GROVES DATE 8/87
CHECKED C.SEAGRAVE 8/87
PROJ. ENGR. C.SEAGRAVE 8/87
RELEASE APPROV. D.R.TAYLOR 8/87

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

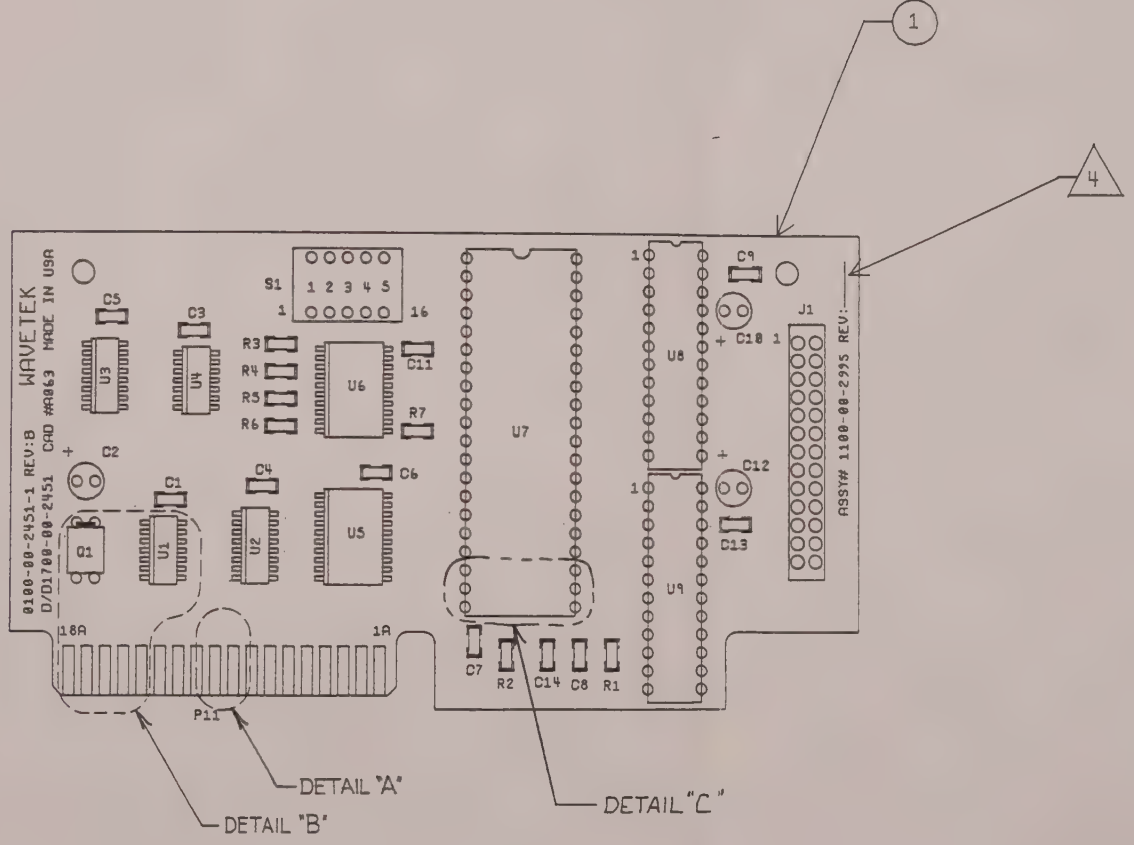
TITLE

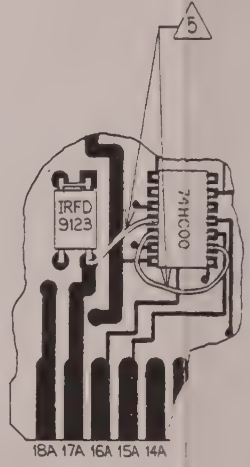
SCHEMATIC, GPIB

SIZE D FSCM NO. 23338 DWG. NO. 0103-00-3176 REV A
SCALE NONE MODEL 51/52 SHEET 1 OF 1

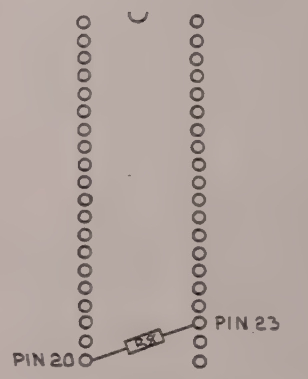
0103-00-3176 A

REV	ECN	BY	DATE	APP
A	ECO # 9898	MS	10/27/88	

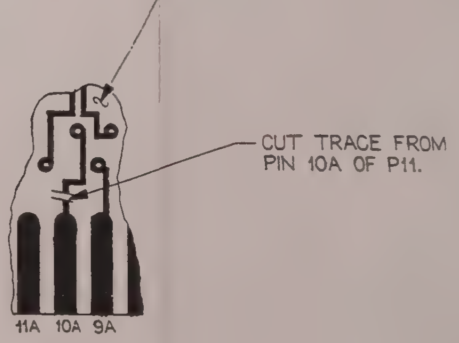

1
4
WAVETEK
0100-00-2451-1 REV:B
D/D1700-00-2451 CAD #A063 MADE IN USA
ASSY# 1100-00-2995 REV:
S1
1 2 3 4 5
1
16
C5
C3
R3
R4
R5
R6
U3
U4
U6
C11
R7
C2
C4
C1
C6
Q1
U1
U2
U5
U7
U8
U9
C9
C18
C12
C13
J1
18A
1A
P11
C7
R2
C14
C8
R1
DETAIL "A"
DETAIL "B"
DETAIL "C"


5
IRFD 9123
74HC00
18A 17A 16A 15A 14A

DETAIL "B"
(SCALE: NONE)


PIN 20
PIN 23
R8

DETAIL "C"
CIRCUIT SIDE
SCALE : NONE △6


COMPONENT SIDE
CUT TRACE FROM PIN 10A OF P11.
11A 10A 9A

DETAIL "A"
(SCALE: NONE)

△6 JUMPER U7 FROM PIN 20 TO PIN 23 WITH R8 ON CIRCUIT SIDE.

△5 LIFT UP PIN 4 AND PIN 9 OF U1 FROM PADS.
ADD JUMPER FROM U1, PIN 5 TO U1, PIN 9.
ADD JUMPER FROM U1, PIN 4 TO Q1, SOURCE.

△4 MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.

3 SEE INSTRUMENT SCHEMATIC 0004-00-0040 *(MODEL 51/52) OR 0004-00-0539 (MODEL 52A)* FOR ASSEMBLY INTERCONNECTION.

2. SEE 0103-00-3176 FOR SCHEMATIC.

1. SEE PARTS LIST 1100-00-3176.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL —//—
FINISH WAVETEK PROCESS —//—
DRAWN M.O. Graves DATE 8-6-87
PROJ ENGR C. Seagone 8-14-87
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE 2/1

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PCA,
GPIB OPTION

MODEL NO. 51/52
DWG NO. 1100-00-3176
REV A
CODE IDENT 23338
SHEET 1 OF 1

1100-00-3176 A

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, GPIB BD 50-13A	0103-00-3176	WVTK	0103-00-3176	1
NONE	KIT, SMD LOAD (52-2451)	1208-00-2866	WVTK	1208-00-2866	1
C10 C12 C2	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	3
J1	CONN, HEADER 26 PIN/2 ROW, .1 CTR, 15 GLD	929836-01-13	A/P	2100-02-0156	1
NONE	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
Q1	TRANSISTOR	IRFD9123	IR	4902-09-1230	1
S1	SWITCH PC	500-105	DUNCN	5199-00-0001	1
U8 U9	BUS XCVR, BIDIR, Q, TTL	MC3447P3	MOT	8000-34-4700	2
U7	IEEE 488 INTERFACE ADAPTER	MC68A488P	MOT	8006-84-8801	1

WAVETEK PARTS LIST	TITLE PCA, GPIB BD 50-13A	ASSEMBLY NO. 1100-00-3176 PAGE 1	REV A

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE x/x ± 1/64 · .xxx ± .005 · .xx ± .01 · ∠ ± 1°	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.
MATERIAL:	DRAWN · DATE	TITLE PARTS LIST PCA, GPIB BD 50-13A
	CHKD	
	ENG APPR.	
FINISH:	MFG APPR.	SIZE D · MODEL NO. 50-13A · DRAWING NO 1100-00-3176 · REV A
	ISSUED	SCALE: · CODE IDENT 23338 · SHEET 1 OF 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C1 C11 C13 C14 C3 C4 C5 C6 C7 C8 C9	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	11
1	DRILL DRWG, GPIB OPT BD	1700-00-2451	WVTK	1700-00-2451	1
R1 R2	RES, SMD GP 1/8 LONG 200PPM 5% 100 OHM	9C12063A1000JLR	MEPCO	4703-20-1015	2
R3 R4 R5 R6 R7	RES, SMD GP 1/8 LONG 200PPM 5% 220K OHM	9C12063A2203JLR	MEPCO	4703-20-2245	5
U1	GATE, NAND, QUAD, 2INP POS, SMD	74HC00D	SIG	8000-74-0041	1
U4	GATE, NOR QUAD 2 INPUT POS HCMOS SMD	74HC02D	SIG	8000-74-0241	1
U2	FLIP-FLOP, HEX, RESET, HCMOS, SMD	74HC174D	SIG	8007-41-7441	1
U6	BUF/LN DRIVER, OCTAL, TRISTATE, HCMOS, SMD	N74HC244D	SIG	8007-42-4441	1
U5	TRANSCEIVER, OCTAL BUSS, TRISTATE, HCMOS, SMD	74HC245D	SIG	8007-42-4541	1
U3	HEX BUFFER\LINE DRIVER, TRI-STATE, HCMOS, SMD	74HC367D	SIG	8007-43-6741	1

WAVETEK PARTS LIST	TITLE KIT, SMD LOAD (52-2451)	ASSEMBLY NO. 1208-00-2866 PAGE 1	REV

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/x	.xxx	.xx	∠
± 1/64	± .005	± .01	± 1°

MATERIAL:

FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

	DATE
DRAWN	
CHKD	
ENG APPR.	
MFG APPR.	
ISSUED	

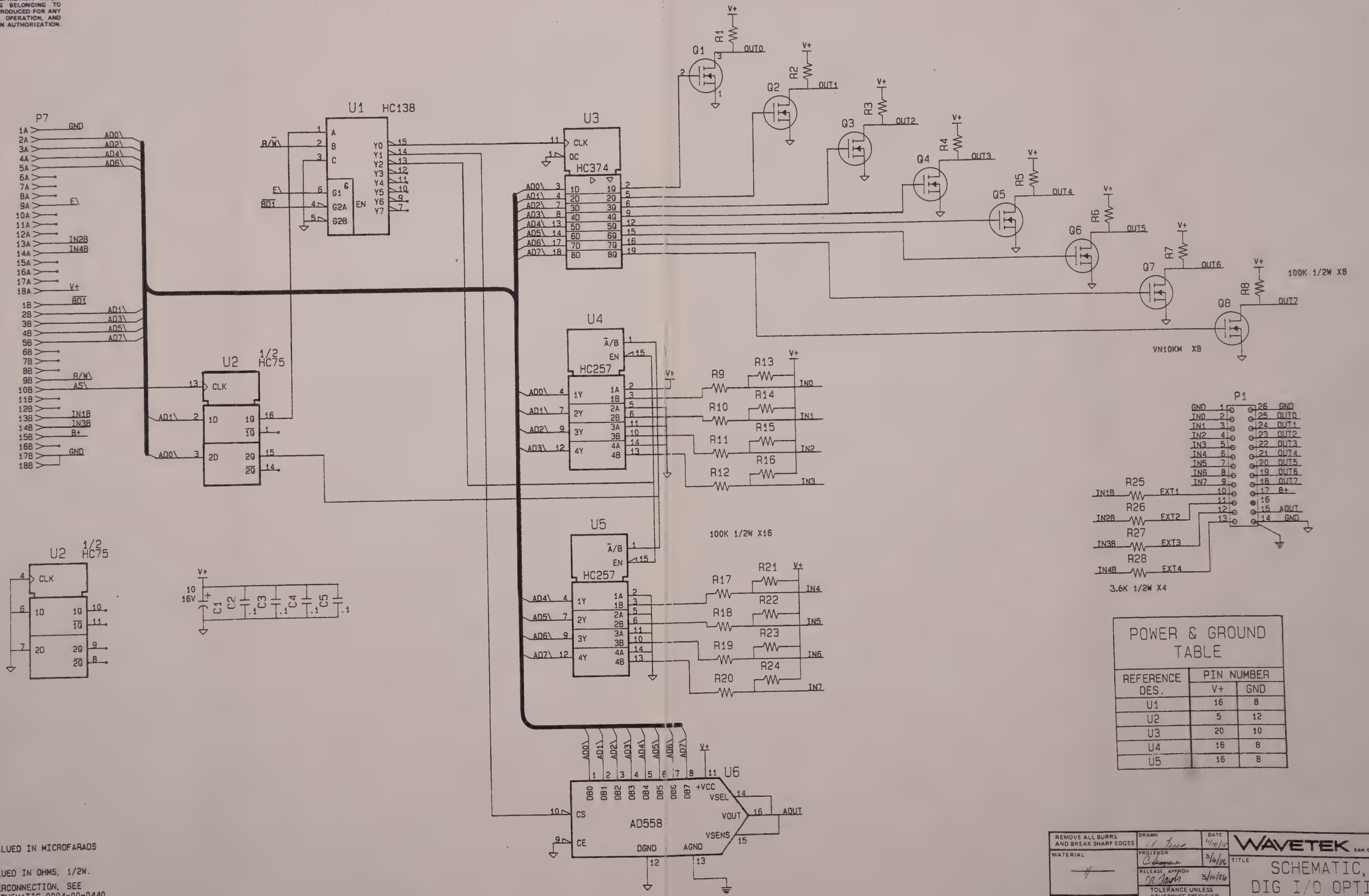
WAVETEK
Wavetek Inc.

TITLE
PARTS LIST
KIT, SMD LOAD
(52-2451)

SIZE	MODEL NO.	DRAWING NO	REV
D	50-13A	1208-00-2866	

SCALE: CODE IDENT 23338 SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	RELEASE ECO#9816	M.S.	5/4/89	YM


P7
1A GND
2A AD0\
3A AD2\
4A AD4\
5A AD6\
9A E\
13A IN2B
14A IN4B
18A V+
1B BD1
2B AD1\
3B AD3\
4B AD5\
5B AD7\
9B R/W\
10B AS\
13B IN1B
14B IN3B
15B B+
17B GND
U1 HC138
A
B
C
G1
G2A
G2B
EN
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
R/W\
E\
BD1
U2 1/2 HC75
CLK
1D
1Q
2D
2Q
U3
HC374
CLK
OC
1D
1Q
2D
2Q
3D
3Q
4D
4Q
5D
5Q
6D
6Q
7D
7Q
8D
8Q
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
R1
R2
R3
R4
R5
R6
R7
R8
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
100K 1/2W X8
VN10KM X8
U4
HC257
Ā/B
EN
1Y
2Y
3Y
4Y
1A
1B
2A
2B
3A
3B
4A
4B
R9
R10
R11
R12
R13
R14
R15
R16
IN0
IN1
IN2
IN3
100K 1/2W X16
U5
HC257
R17
R18
R19
R20
R21
R22
R23
R24
IN4
IN5
IN6
IN7
U2 1/2 HC75
C1
C2
C3
C4
C5
10 16V
.1
U6
AD558
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
+VCC
VSEL
VOUT
VSENS
CS
CE
DGND
AGND
AOUT
P1
GND
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
EXT1
EXT2
EXT3
EXT4
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
B+
AOUT
GND
R25
R26
R27
R28
IN1B
IN2B
IN3B
IN4B
3.6K 1/2W X4

POWER & GROUND TABLE

REFERENCE DES.	PIN NUMBER V+	PIN NUMBER GND
U1	16	8
U2	5	12
U3	20	10
U4	16	8
U5	16	8

3. CAPACITORS VALUED IN MICROFARADS (uF).
2. RESISTORS VALUED IN OHMS, 1/2W.
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0440 FOR MODEL 51/52 OR 0004-00-0539 FOR MODEL 51A.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

DRAWN C.L. [illegible] DATE 11/15/85

PROJ ENGR C. [illegible] 3/6/86

RELEASE APPROV M. [illegible] 3/10/86

MATERIAL —//—

FINISH WAVETEK PROCESS —//—

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC, DIG I/O OPTION

MODEL NO. 51/52

DWG NO. 0103-00-3147

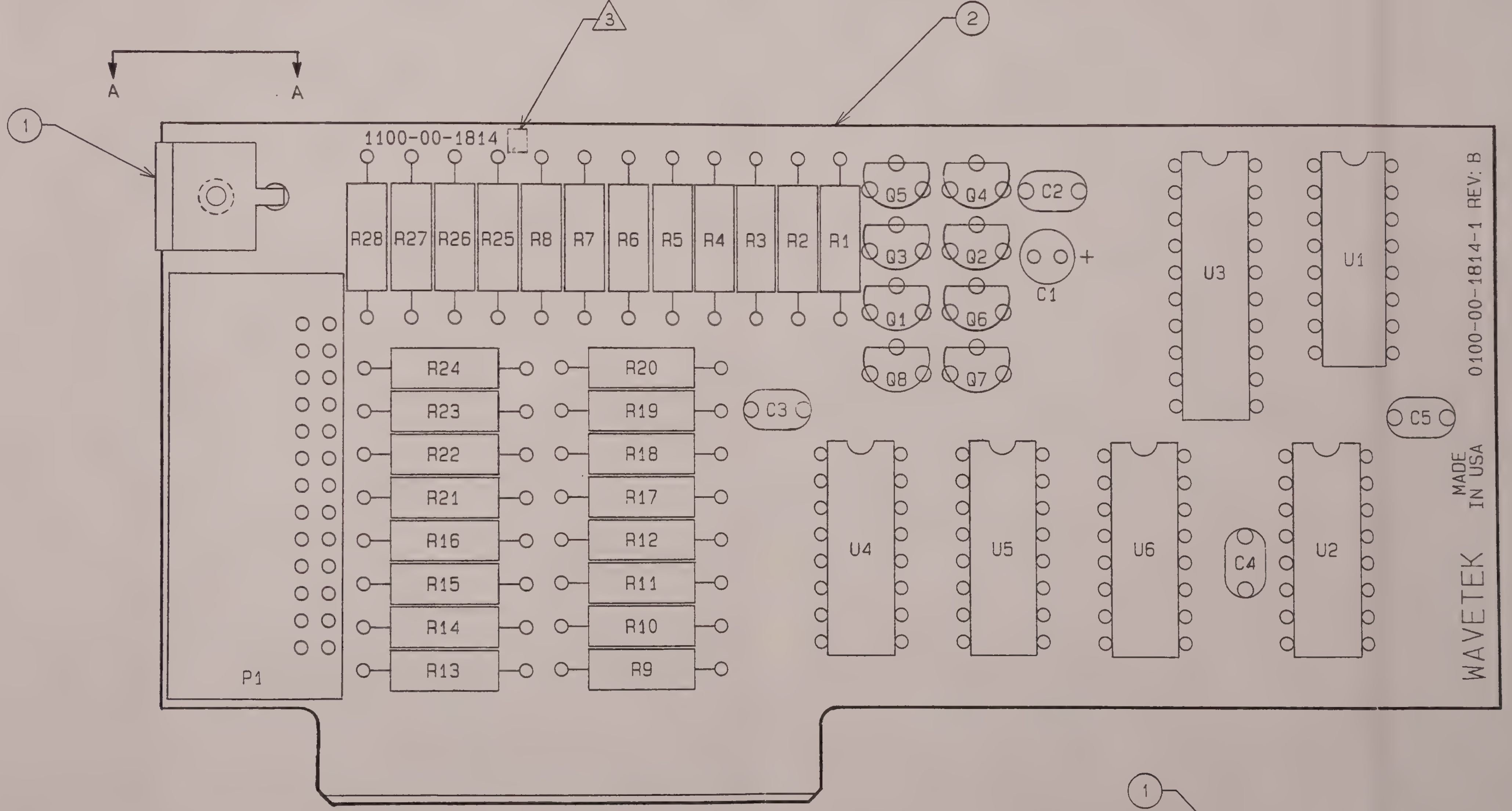
REV A

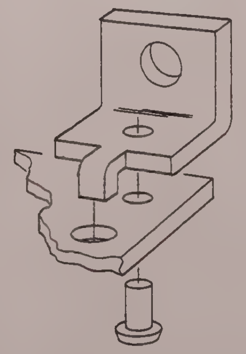
CODE IDENT 23338

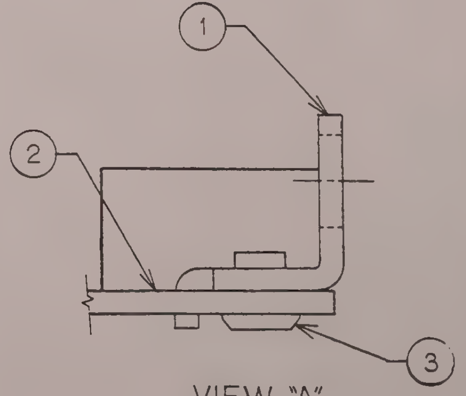
SHEET 1 OF 1

0103-00-3147 A

REV	ECN	BY	DATE	APP
A	RELEASE ECO#9816	M.S.	8/4/88	


A
A
①
③
②
1100-00-1814
R28
R27
R26
R25
R8
R7
R6
R5
R4
R3
R2
R1
Q5
Q4
C2
Q3
Q2
C1
+
Q1
Q6
Q8
Q7
U3
U1
0100-00-1814-1 REV: B
R24
R23
R22
R21
R16
R15
R14
R13
R20
R19
R18
R17
R12
R11
R10
R9
C3
C5
U4
U5
U6
C4
U2
MADE IN USA
WAVETEK
P1





VIEW "A"

③ MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.

2. SEE INSTRUMENT SCHEMATIC 0004-00-0440 FOR 51/52 OR 0004-00-0539 FOR 52A FOR ASSEMBLY INTERCONNECTION.

1. SEE 0103-00-1814 FOR SCHEMATIC.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1100-00-3147

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN P. Tan	DATE 1/14/86	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —‖—	PROJ ENGR N. S. Muller	1/14/96	TITLE PCA, DIGITAL 1/0
	RELEASE APPROV	3/6/86	
FINISH WAVETEK PROCESS —‖—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 51, 52
	SCALE 4/1		DWG NO. 1100-00-3147
			REV A
			CODE IDENT 23338
			SHEET 1 OF 1

1100-00-3147 A

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, DIGITAL I/O BD	0103-00-3147	WVTK	0103-00-3147	1
1	BRKT, RETAINING	52-1213	WVTK	1400-02-1213	1
C2 C3 C4 C5	CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2	SR215E104ZAA	AVX	1500-01-0420	4
C1	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	1
2	DRILL DRWG, PCA, DIGITAL I/O BOARD	1700-1814	WVTK	1700-00-1814	1
P1	CONN, HEADER, 26 PIN, 0.1 SPACE DOUBLE	1-103167-0	AMP	2100-02-0201	1
3	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	1
R25 R26 R27 R28	RES, C, 1/2W, 5%, 3.6K	RC-1/2-362J	STKPL	4700-25-3601	4
R1 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R3 R4 R5 R6 R7 R8 R9	RES, METAL OXIDE 1/2W 100K 5%	RSF1/2BJ100K	M-OHM	4705-25-1003	24
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8	TRANS	VN10KM	SLCON	4902-00-0100	8
U6	DAC, 8-BIT, INTERNAL REF, 16 PIN DIP	AD558JN	ANDEV	7000-05-5801	1
U2	LATCH QUAD,	N74HC75N	SIG	8000-74-7501	1

WAVETEK PARTS LIST

TITLE PCA, DIGITAL I/O BD

ASSEMBLY NO. 1100-00-3147

REV A

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	TRANSPARENT, HCMOS, 16 PIN DIP				
U1	DECODER, 3-8 LINE, CMOS	MC74HC138N	MOT	8007-41-3840	1
U4 U5	MUX, QUAD 2-INPUT, TRI-STATE, HCMOS, 16 PIN	N74HC257N	SIG	8007-42-5701	2
U3	FLIP-FLOP, OCT D, TRI-S, CMOS	74HC374	TI	8007-43-7440	1

WAVETEK PARTS LIST

TITLE PCA, DIGITAL I/O BD

ASSEMBLY NO. 1100-00-3147

REV A

PAGE 2

50-15.
473.00
1100-3095

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/x	.xxx	.xx	∠
± 1/64	± .005	± .01	± 1°

MATERIAL:

FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

	DATE
DRAWN	
CHKD	
ENG APPR.	
MFG APPR.	
ISSUED	

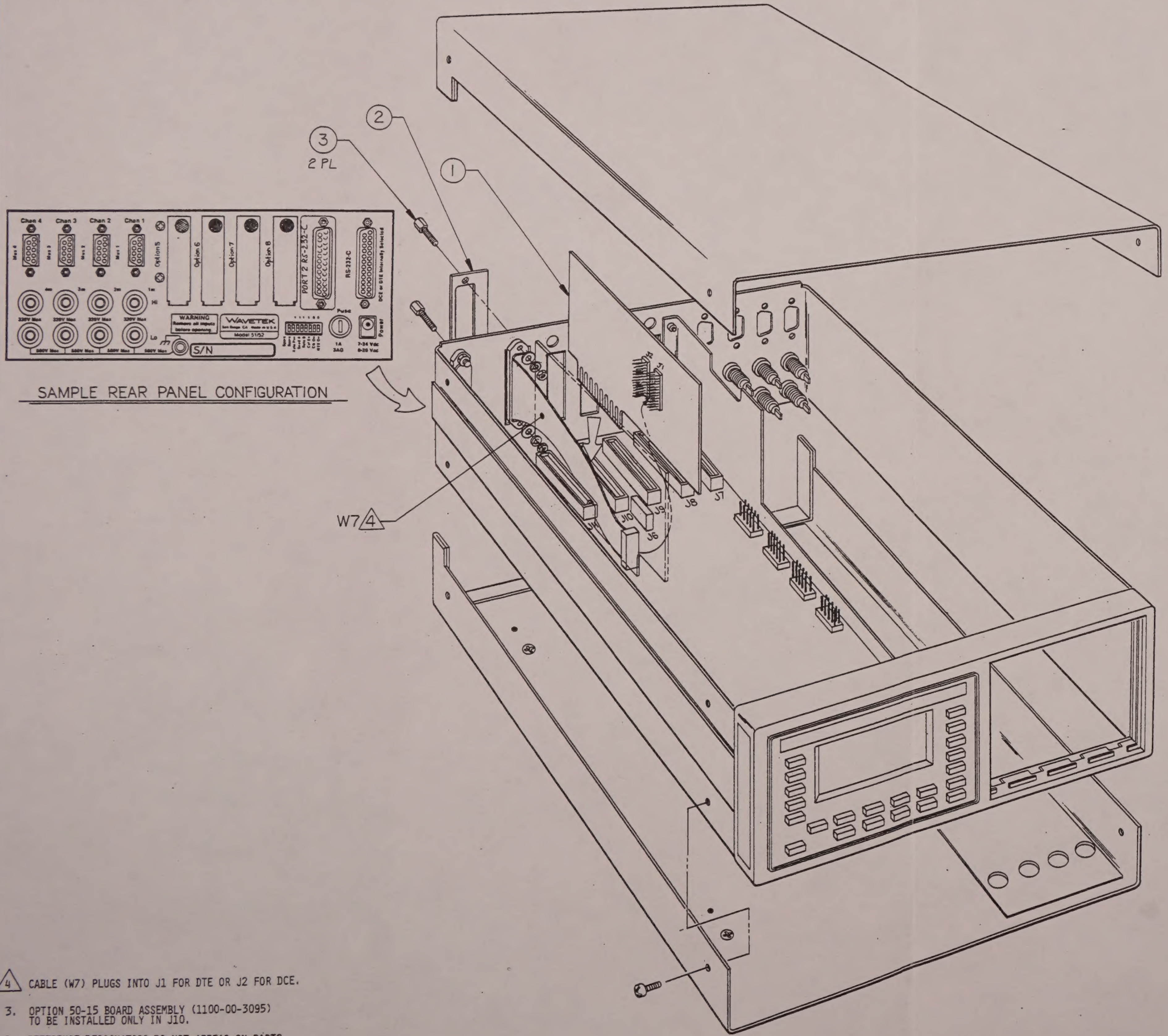
WAVETEK
Wavetek Inc.

TITLE
PARTS LIST
PCA, DIGITAL I/O BD

SIZE	MODEL NO.	DRAWING NO	REV
D	50-14	1100-00-3147	A

SCALE:
CODE IDENT 23338
SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	RELEASE PER ERO NO. 9797	MAG	3-25-88	nm



Chan 4
Chan 3
Chan 2
Chan 1
Option 5
Option 6
Option 7
Option 8
PORT 2 RS-232-C
RS-232-C
DCE or DTE Internally Selected
Hi
Lo
320V Max
500V Max
WARNING Remove all inputs before opening
WAVETEK
Model 51/52
Fuse
1A 3AG
Power
7-24 Vdc 6-20 Vac
S/N
3
2 PL
2
1
W7 4
J7
J8
J9
J10
J5

SAMPLE REAR PANEL CONFIGURATION

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT-52A	0004-00-0539	WVTK	0004-00-0539	1
1	ASSY, 50-15 SERIAL CARD	1100-00-3095	WVTK	1100-00-3095	1
3	MODIFICATION, JACK SCREW	23/75-9669	WVTK	1400-01-9669	1
2	PLATE, ADAPTER	1400-02-4470	WVTK	1400-02-4470	1
W7	ASSY, RIBBON CABLE	6002-00-0029	WVTK	6002-00-0029	1

WAVETEK PARTS LIST	TITLE OPTION 50-15 SERIAL CARD	ASSEMBLY NO. 1000-00-0540 PAGE 1	REV A

4 CABLE (W7) PLUGS INTO J1 FOR DTE OR J2 FOR DCE.

3. OPTION 50-15 BOARD ASSEMBLY (1100-00-3095) TO BE INSTALLED ONLY IN J10.

2. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0539

NOTE: UNLESS OTHERWISE SPECIFIED

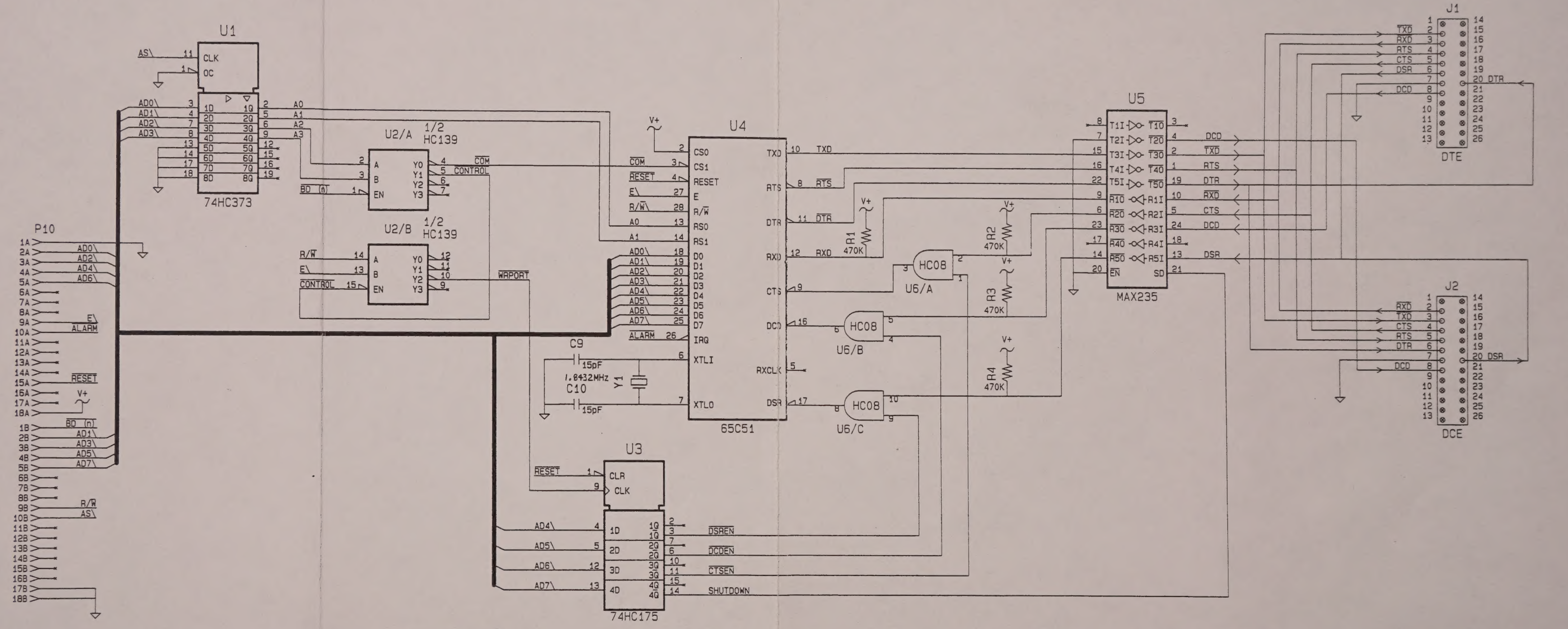
SEE SEPARATE PARTS LIST 1000-00-0540

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN MIKE GROVES	DATE 3-25-88	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	PROJ ENGR C. Scagnone	6-21-88	TITLE ASSEMBLY, SERIAL CARD OPTION (OPTION 50-15)
	RELEASE APPROV JR Taylor		
FINISH WAVETEK PROCESS —//—	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 52A
	SCALE NONE		DWG NO. 1000-00-0540 REV A
			CODE IDENT 23338 SHEET 1 OF 1

1000-00-0540 A

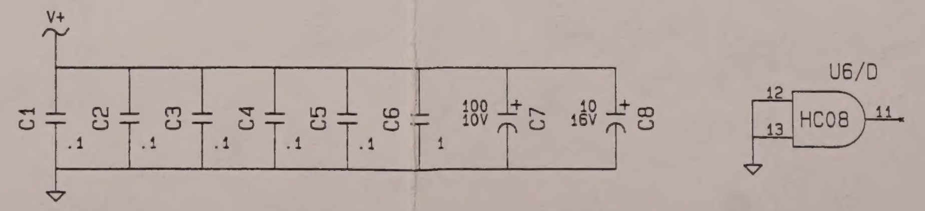
BISHOP GRAPHICS/ACCUPRESS

REV	ECO	BY	DATE	APP
A	FOR RELEASE ERD9797	nm	6/10/88	


U1
74HC373
CLK
OC
AS\
AD0\
AD1\
AD2\
AD3\
A0
A1
A2
A3
U2/A 1/2 HC139
U2/B 1/2 HC139
COM
CONTROL
BD (n)
R/W
E\
WRPORT
U4
65C51
CS0
CS1
RESET
E
R/W
RS0
RS1
D0
D1
D2
D3
D4
D5
D6
D7
IRQ
XTLI
XTLO
TXD
RTS
DTR
RXD
CTS
DCD
RXCLK
DSR
ALARM
C9
15pF
1.8432MHz
Y1
C10
15pF
V+
R1 470K
R2 470K
R3 470K
R4 470K
U6/A
U6/B
U6/C
HC08
U5
MAX235
T1I
T2I
T3I
T4I
T5I
R1O
R2O
R3O
R4O
R5O
EN
T1O
T2O
T3O
T4O
T5O
R1I
R2I
R3I
R4I
R5I
SD
J1
DTE
J2
DCE
TXD
RXD
RTS
CTS
DSR
DCD
DTR
20 DTR
20 DSR
U3
74HC175
CLR
CLK
AD4\
AD5\
AD6\
AD7\
DSREN
DCDEN
CTSEN
SHUTDOWN
P10
1A
2A
3A
4A
5A
6A
7A
8A
9A
10A
11A
12A
13A
14A
15A
16A
17A
18A
1B
2B
3B
4B
5B
6B
7B
8B
9B
10B
11B
12B
13B
14B
15B
16B
17B
18B
AS\

POWER & GROUND TABLE

REFERENCE DES.	PIN NUMBER	
	V+	GND
U1	20	10
U2	16	8
U3	16	8
U4	15	1
U5	12	11
U6	14	7


V+
C1
.1
C2
.1
C3
.1
C4
.1
C5
.1
C6
1
100 10V
C7
10 16V
C8
U6/D
HC08
12
13
11

3. CAPACITOR VALUES ARE IN MICROFARADS (µF).

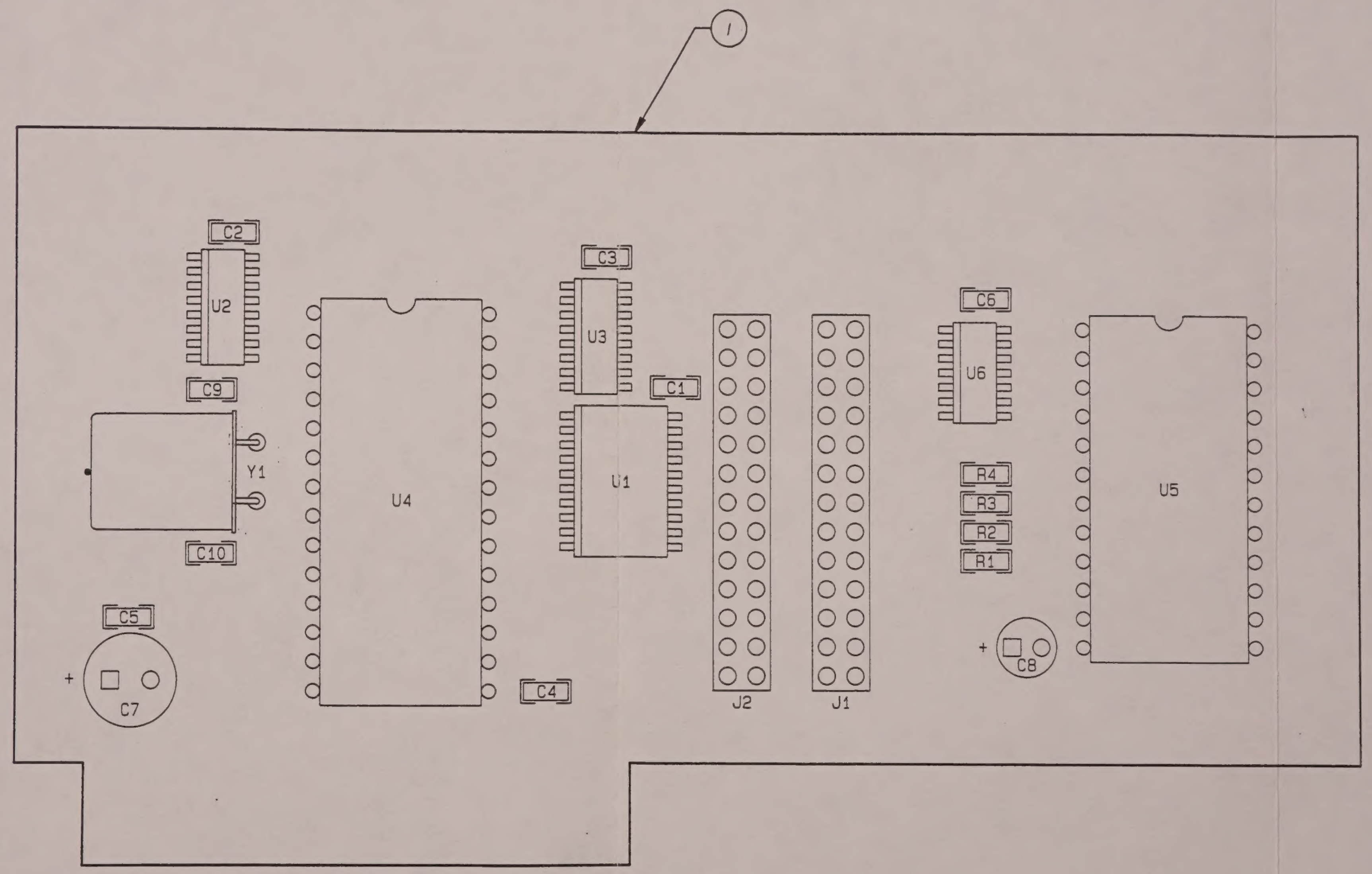
2. RESISTOR VALUES ARE IN OHMS (Ω), 1/8W.

1. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-0539.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ANN TARR	DATE 6-16-88	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	CHECKED N. S. Nath	6/10/88	TITLE SCHEMATIC, SERIAL CARD
	PROJ. ENGR. C. Leayne	6-21-88	
FINISH WAVETEK PROCESS —//—	RELEASE APPROV. DL Taylor	6/22/88	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D FSCM NO. 23338 DWG. NO. 0103-00-3095 REV A
DO NOT SCALE DRAWING			SCALE NONE MODEL 52A SHEET 1 OF 1

REV	ECO	BY	DATE	APP
A	FOR RELEASE ERO 9797	hm	6/16/98	



SEE SEPARATE PARTS LIST 1100-00-3095

2. SEE 0103-00-3095 FOR SCHEMATIC.
1. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-0539.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ANN TARR	DATE 6/14/98	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	CHECKED	6/16/98	TITLE PCA, SERIAL CARD
	PROJ. ENGR.	6-21-98	
FINISH WAVETEK PROCESS —//—	RELEASE APPROV.	6/22/98	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3095 · REV A
DO NOT SCALE DRAWING			SCALE 4/1 · MODEL 52A · SHEET 1 OF 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, 50-15 SERIAL CARD	0103-00-3095	WVTK	0103-00-3095	1
C8	CAP, ELECT, 10MF, 20%, 16 V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	1
C7	CAP, ELECT, 100MF/10V	SXE10VB101MC	UNCON	1500-31-0121	1
C1 C2 C3 C4 C5 C6	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	6
C10 C9	CAP, SMD CER 5% 50V 15PF	C1206C150J2GAC	KEMET	1500-81-5001	2
1	DRILL DRWG, PCB, 50-15 SERIAL CARD	1700-00-3095	WVTK	1700-00-3095	1
J1 J2	CONN, HEADER 26 PIN/2 ROW, .1 CTR, 15 GLD	929836-01-13	A/P	2100-02-0156	2
Y1	CRYSTAL, HC18 1.8432 MHZ 3RD LEAD	FOX018SX	FOX	2300-99-0032	1
R1 R2 R3 R4	RES, SMD GP 1/8 LONG 200PPM 5% 470K OHM	MCR18EZH474JW5%	ROHM	4703-20-4745	4
U5	DRIVER/RECEIVER, RS232	MAX235CPG	MAXIM	8000-02-3200	1
U4	ADAPTER, ASYNC, COMM INTERFACE, CMOS	R65C51P2	ROCKW	8000-65-5100	1
U6	GATE, QUAD 2 IN, AND, CMOS, SMD	CD74HC08M	RCA	8007-40-8000	1

WAVETEK PARTS LIST	TITLE ASSY, 50-15 SERIAL CARD	ASSEMBLY NO. 1100-00-3095 PAGE 1	REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U2	DEMUX, DUAL 2-TO-4 DECODER, SMD	74HC139D	SIG	8007-41-3941	1
U3	FLIP FLOP, D, HEX QUAD, W/CIR, SMD, CMOS	74HC175D	SIG	8007-41-7520	1
U1	D-TRANSPARENT LATCH, OCTAL, TRISTATE, HCMOS, SMD	74HC373D	SIG	8007-43-7341	1

WAVETEK PARTS LIST	TITLE ASSY, 50-15 SERIAL CARD	ASSEMBLY NO. 1100-00-3095 PAGE 2	REV A

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE				DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES		WAVETEK Wavetek Inc.
x/x ± 1/64	.xxx ± .005	.xx ± .01	∠ ± 1°	DRAWN	DATE	TITLE PARTS LIST ASSY, 50-15 SERIAL CARD
MATERIAL:				CHKD		
				ENG APPR.		
FINISH:				MFG APPR.		SIZE D · MODEL NO. 50-15 · DRAWING NO. 1100-00-3095 · REV A
				ISSUED		SCALE: · CODE IDENT 23338 · SHEET 1 OF 1